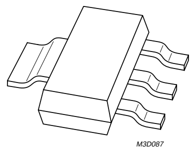


PHT4NQ10T

TrenchMOS™ standard level FET

Rev. 02 — 2 May 2002 **Product data**

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHT4NQ10T in SOT223.

2. Features

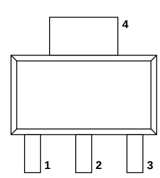
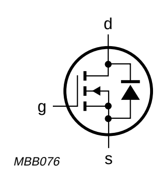
- TrenchMOS™ technology
- Very fast switching
- Surface mount package.

3. Applications

- Primary side switch in DC to DC converters
- High speed line driver
- Fast general purpose switch.

4. Pinning information

Table 1: Pinning - SOT223, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 SOT223	
2	drain (d)		
3	source (g)		
4	drain (d)		

5. Quick reference data

Table 2: Quick reference data

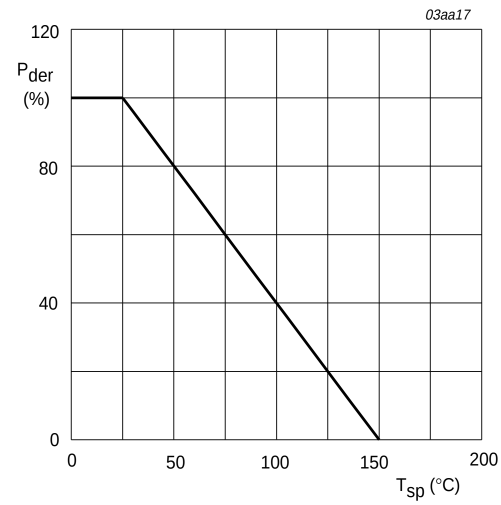
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	100	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 10 V	-	3.5	A
P_{tot}	total power dissipation	T_{sp} = 25 °C	-	6.9	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.75 A			
		T_j = 25 °C	200	250	mΩ
		T_j = 150 °C	-	575	mΩ

6. Limiting values

Table 3: Limiting values

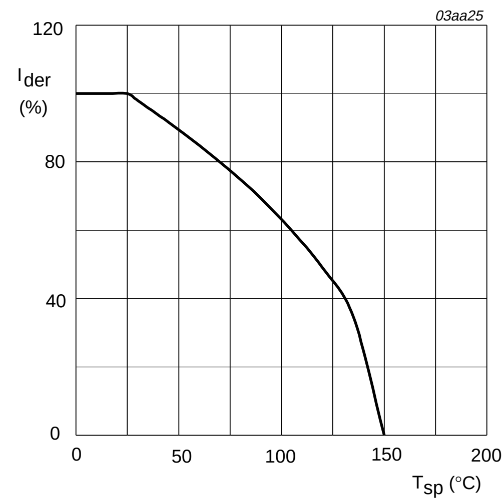
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	100	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	3.5	A
		T_{sp} = 100 °C; V_{GS} = 10 V; Figure 2	-	2.2	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	14	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1	-	6.9	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{sp} = 25 °C	-	3.5	A
I_{SM}	peak source (diode forward) current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	-	14	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 3.5 A; t_p = 0.2 ms; V_{DD} ≤ 15 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C; Figure 4	-	45	mJ
$I_{DS(AL)SM}$	peak non-repetitive drain-source avalanche current		-	3.5	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

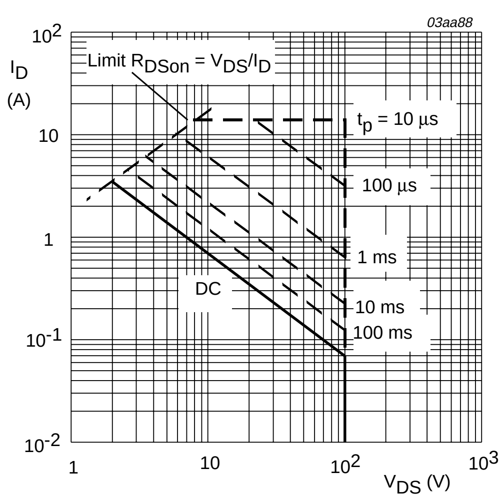
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 10$ V

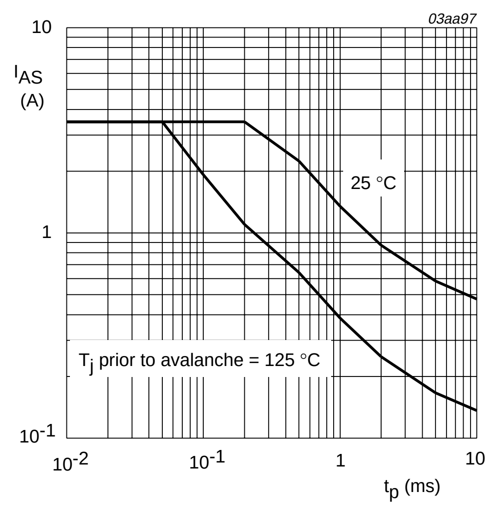
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25$ °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; $V_{DD} \leq 15$ V; $R_{GS} = 50\ \Omega$;
$V_{GS} = 10$ V; starting $T_j = 25$ °C and 125 °C.

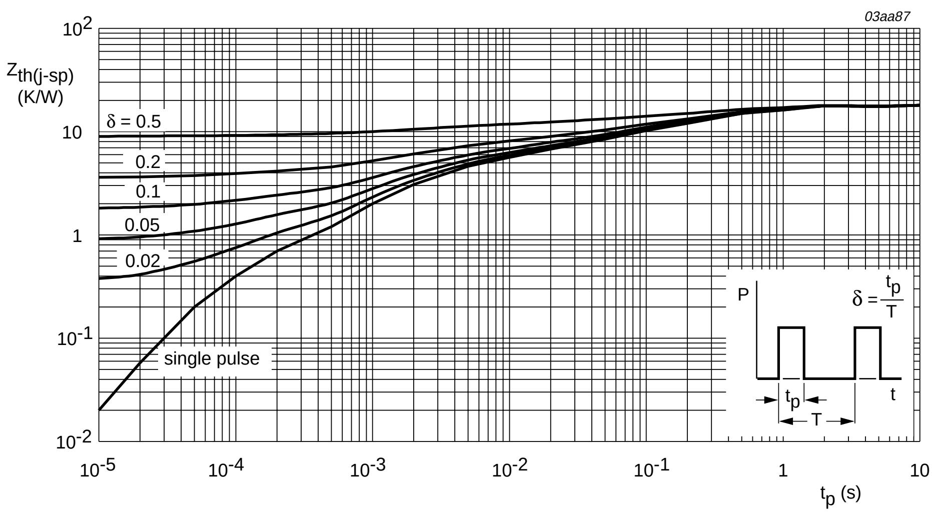
Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; Figure 5	-	-	18	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	-	150	-	K/W

7.1 Transient thermal impedance



Mounted on a metal clad substrate.

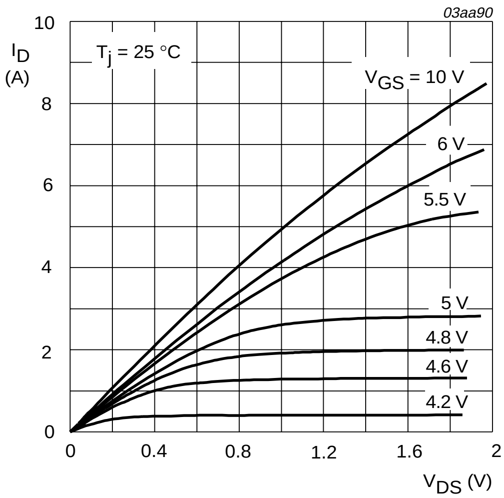
Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

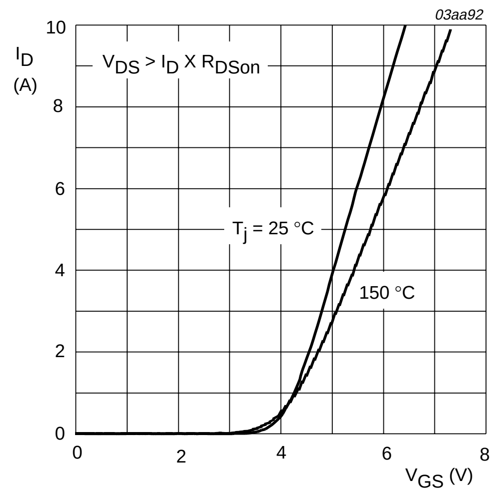
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	100	130	-	V
		T_j = –55 °C	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}				
		T_j = 25 °C; Figure 10	2	3	4	V
		T_j = 150 °C; Figure 10	1.2	-	-	V
		T_j = –55 °C; Figure 10	-	-	6	V
I_{DSS}	drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V				
		T_j = 25 °C	-	1	25	µA
		T_j = 150 °C	-	4	250	µA
		V_{DS} = 60 V; V_{GS} = 0 V				
		T_j = 85 °C	-	-	1	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.75 A				
		T_j = 25 °C; Figure 8 and 9	-	200	250	mΩ
		T_j = 150 °C; Figure 9	-	-	575	mΩ
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 5 V; I_D = 3.5 A; Figure 12	-	4.2		S
$Q_{g(tot)}$	total gate charge	I_D = 3.5 A; V_{DS} = 80 V; V_{GS} = 10 V; Figure 15	-	7.4	-	nC
Q_{gs}	gate-source charge		-	1.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.3	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 13	-	300	-	pF
C_{oss}	output capacitance		-	44	-	pF
C_{rss}	reverse transfer capacitance		-	21	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 50 V; R_D = 15 Ω; V_{GS} = 10 V; R_G = 6 Ω	-	8	-	ns
t_r	rise time		-	13	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
t_f	fall time		-	11	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 3.5 A; V_{GS} = 0 V; Figure 14	-	0.87	1.5	V
t_{rr}	reverse recovery time	I_S = 3.5 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	50	-	ns
Q_r	recovered charge		-	100	-	nC



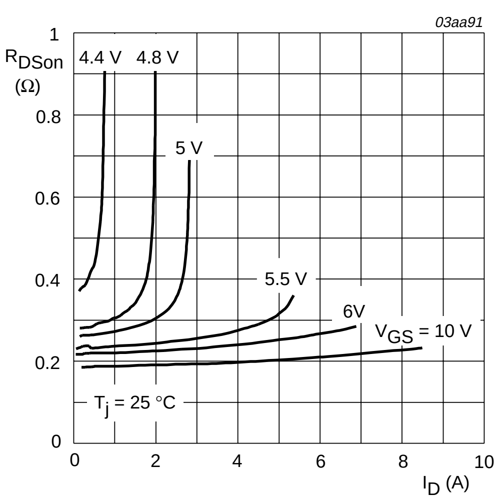
T_j = 25 °C

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



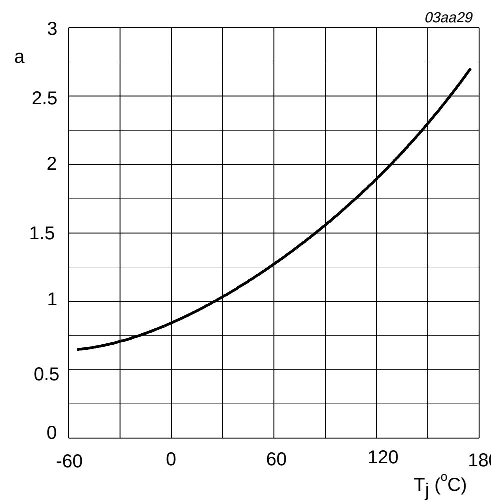
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



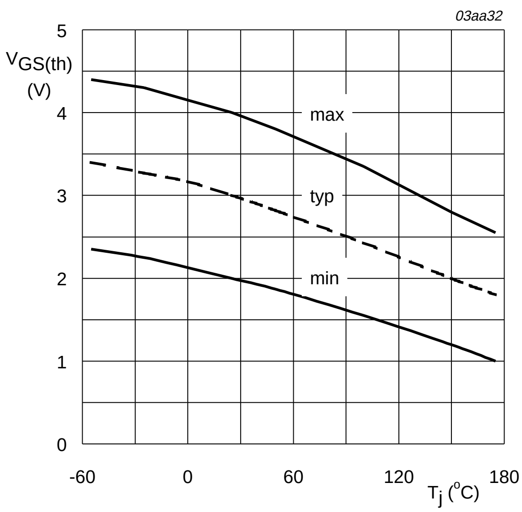
T_j = 25 °C

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



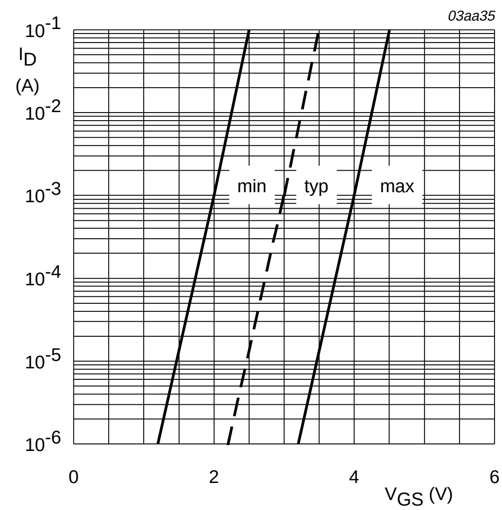
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.



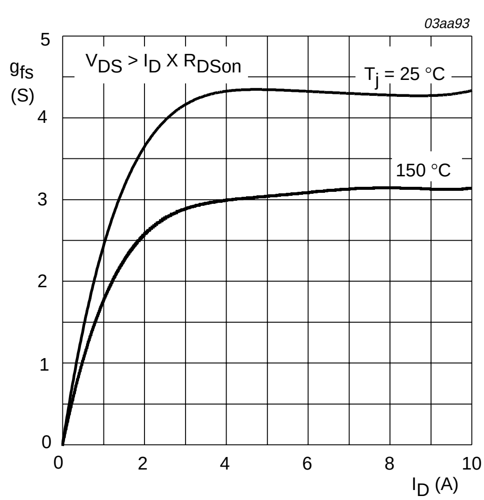
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature.



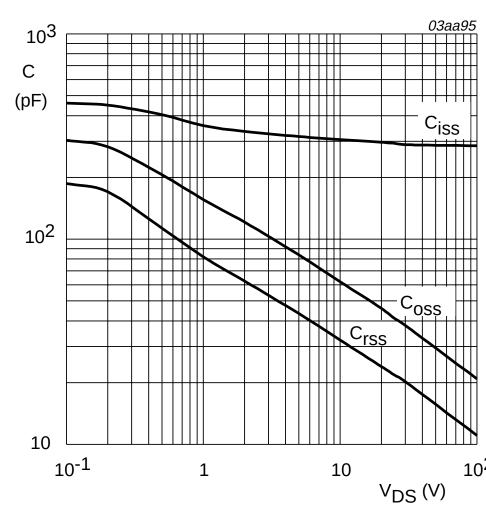
T_j = 25 °C; V_{DS} = 5 V

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



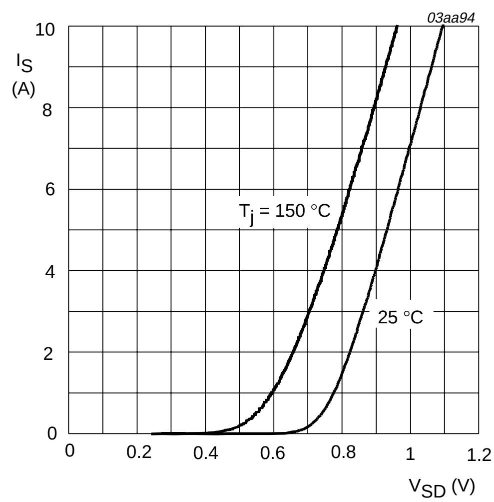
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 12. Forward transconductance as a function of drain current; typical values.



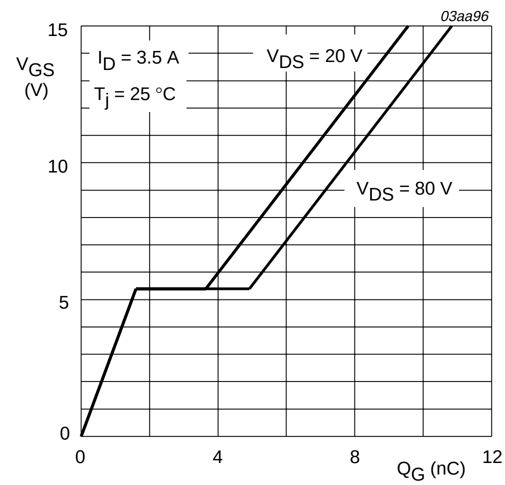
V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

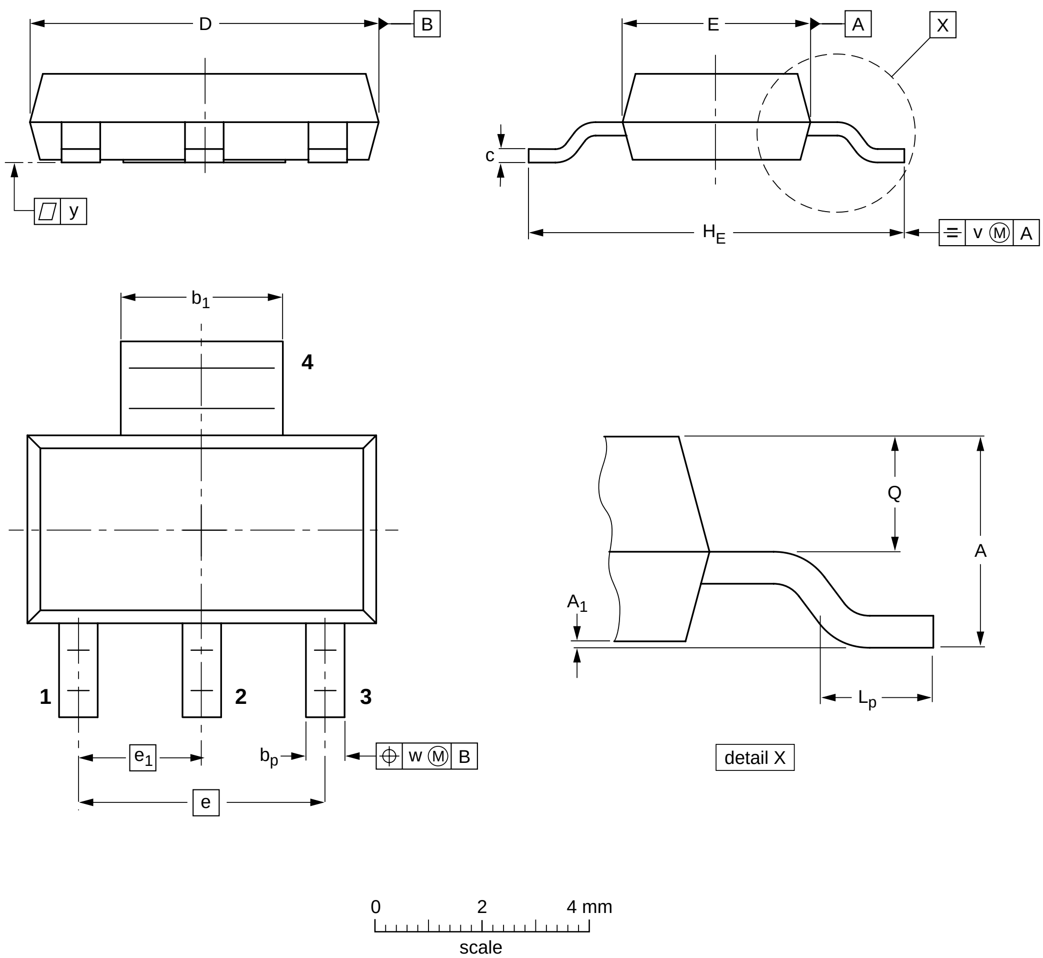


I_D = 3.5 A; V_{DS} = 80 V

Fig 15. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223			SC-73			~~97-02-28~~ 99-09-13

Fig 16. SOT223.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20020502	-	**Product data (9397 750 09581)** Modifications: • Additional I_{DSS} data added.
01	20000731	-	**Product specification; initial version.**

11. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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