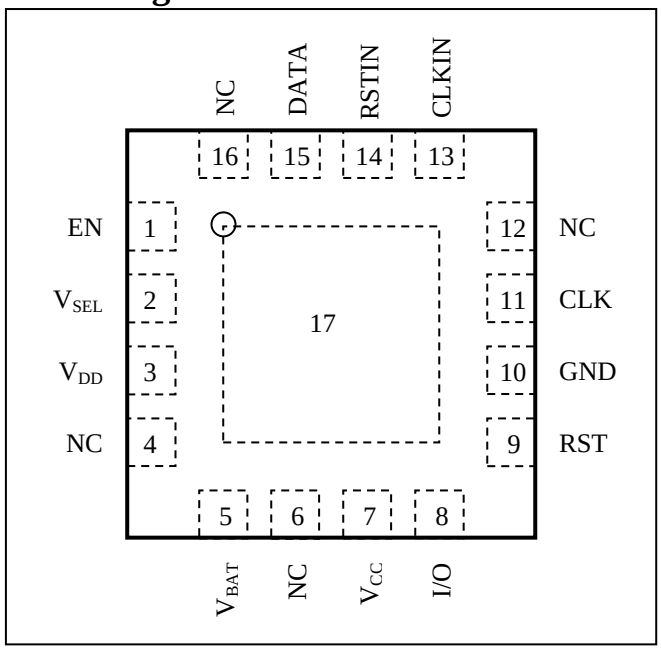
Single SIM/Smart Card Power Supply and Level Translation

Features

- Power Management and Control for two SIM Cards or Smart Cards
- SIM Power Supply 1.8V/3V at 50mA
- Input Voltage Range: 3V to 6V
- Controller Voltage Range: 1.4V to 3.6V
- Automatic Level Translation
- Built-In Fault Protection Circuitry
- Meets all ETSI, IMT-2000 and ISO7816 SIM/Smart Card Interface Requirements
- 40μA Operating Current
- Low Operating/Shutdown Current
- >8kV ESD on SIM Card Pins
- Meets EMV Fault Tolerance Requirements
- Packaging (Pb-free & Green): 16-Lead QFN3x3

Pin Assignment



Note: 16-Lead (3mmx3mm) Plastic QFN Exposed Pad (pin 17) is GND, Must Be Soldered to PCB.

Description

The PI4ULS5V4555 provides the power conversion and signal level translation needed for advanced (2.5G and 3G) cellular telephones to interface with 1.8V and 3V subscriber identity modules (SIMs). The device meets all requirements for 1.8V or 3V SIMs and contains LDO regulators to power 1.8V or 3V SIM cards from a 3V and 6V input. The output voltages can be set using a single selection pin and up to 50mA of load current can be supplied. Internal level translators allow controller operating with supplier as low as 1.4V to interface with 1.8V or 3V Smart Cards. Battery life is maximized by a low operating current of 40μA and a shutdown current of less than 1μA.

Applications

- GSM, TD-SCDMA and other 3G+ Cellular Phones
- Wireless Point-to-Sale Terminals
- Multiple SIM Card Interfaces

Pin Description

Pin	Name	Type	Description
3	V_{DD}	P	Power Input. Control logic power supply voltage input of devices.
5	V_{BAT}	P	Power Input. Analog section power supply voltage input of devices.
7	V_{CC}	O	Power Output. 1.8V or 3V voltage output for respective SIM /Smart cards' power supply V_{CC} pin.
11	CLK	O	Clock Output. Connect CLK pin to SIM/Smart card's CLK pin. CLK signal is derived from the CLKIN pin.
9	RST	O	Reset Output. Connect RST pin to SIM/Smart card's RST pin. RST signal is derived from the RSTIN pin.
8	I/O	I/O	Data Port. Connect I/O pin to SIM/Smart card's I/O pin. Communication path can be set from DATA to I/O.
15	DATA	I/O	Data Port. I/O pin transmits/receives data to/from the DATA pin.
13	RSTIN	I	Reset Input. Reset signal is transmitted from RSTIN to RST.
14	CLKIN	I	Clock Input. Clock signal is transmitted from CLKIN to CLK.
1	EN	I	V_{CC} Enable Control Inputs. EN=HIGH output active, EN=LOW shutdown the device.
2	V_{SEL}	I	Voltage Selection Input. V_{SEL}=LOW, V_{CC}=1.8V and V_{SEL}=HIGH, V_{CC}=3V
4, 6, 12, 16	NC	-	No Connection.
10	GND	P	Ground.
17	GND	P	Ground. Exposed pad of the package bottom.

V_{SEL} Truth Table

V_{SEL}	Selected Voltage
0	1.8V (V_{CC}=1.8V)
1	3V (V_{CC}=3V)

Maximum Ratings

Storage Temperature	-65℃ to +150℃
Ambient Temperature	-40℃ to +85℃
ESD(HBM) for all pins	8KV
V_{BAT}, V_{DD}, V_{CC} to GND	-0.5V to +6.0V
I/O, CLK, RST	-0.5V to V_{CC} +0.5V
I_{CC}	50mA
V_{CC} Short Circuit Duration	Indefinite

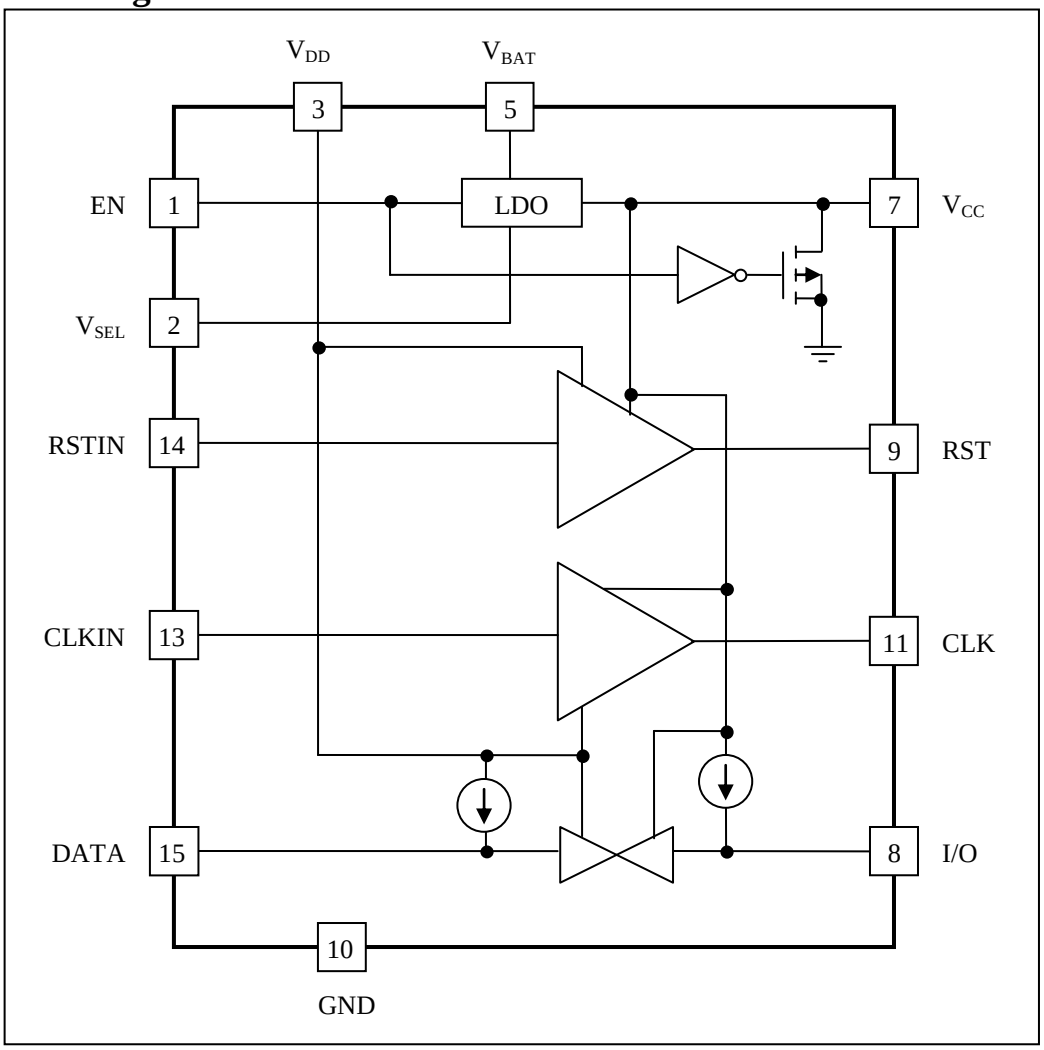
Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The device is guaranteed to meet performance specifications from 0 ℃ to 85 ℃. Specification over the -40 ℃ to 85 ℃ operating temperature range are assured by design, characterization and correlation with statistical controls.
3. I_{CC} based on long-term current density limitation.

DC Electrical Characteristics

(V_{BAT} =3.3V, V_{DD}=1.8V, C_3= 1µF, T_A = –40℃ to 85℃, unless otherwise noted.)

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
Input Power Supply						
V_{BAT}	V_{BAT} Operating Voltage	-	3.0	-	6.0	V
I_{BAT}	V_{BAT} Operating Current	V_{CC}=3V, I_{CC}=0A	-	40	60	µA
		V_{CC}=1.8V, I_{CC} =0A				
V_{DD}	V_{DD} Operating Voltage	-	1.4	-	3.6	V
I_{DD}	V_{DD} Operating Current	-	-	5	10	µA
I_{DDS}	V_{DD} Shutdown Current	-	-	0.1	1	
I_{BATS}	V_{BAT} Shutdown Current	V_{DD} =0V	-	0.1	1	
SIM Card Supplies						
V_{CC}	Output Voltage	3V Mode. 0mA<I_{CC}<50mA	2.85	3.00	3.15	V
		1.8V Mode. 0mA<I_{CC}<30mA	1.71	1.8	1.89	
	Turn on time of V_{CC}	I_{CC}=0mA, EN active to V_{CC} at 90% Selected Voltage	-	0.3	1.5	ms
	Turn off time of V_{CC}	I_{CC}=0mA, EN shutdown to V_{CC} at 1V	-	0.5	-	ms
I_{SHORT}	V_{CC} Short Circuit Current	V_{CC} short to GND	60	90	120	mA
CLK						
V_{OL}	Low Level Output Voltage	Sink current =-200µA	-	-	0.2x V_{CC}	V
V_{OH}	High Level Output Voltage	Source current =20µA	0.9x V_{CC}	-	-	V
	Rise/Fall Time	Loaded with 50pF (10% to 90%)	-	-	16	ns
	CLK Frequency	-	5	-	-	MHz
RST						
V_{OL}	Low Level Output Voltage	Sink current =-200µA	-	-	0.2x V_{CC}	V
V_{OH}	High Level Output Voltage	Source current =20µA	0.9x V_{CC}	-	-	V
	Rise/Fall Time	Loaded with 50pF (10% to 90%)	-	-	1	µs
I/O						
V_{OL}	Low Level Output Voltage	Sink current =-1mA (V_{DATA}=0V)	-	-	0.3	V
V_{OH}	High Level Output Voltage	Source current =20µA (V_{DATA}=V_{DD})	0.8× V_{CC}	-	-	V
	Rise/Fall Time	Loaded with 50pF (10% to 90%)	-	-	1	µs
	Short-Circuit current	V_{DATA}=0V	-	3.5	10	mA
DATA						
I_{IL}	Low Level Input Current	-	-	-	1	mA
I_{IH}	High Level Input Current	-	-20	-	20	µA
V_{OL}	Low Level Output Voltage	Sink current =-500µA ($V_{I/O}$=0V)	-	-	0.3	V
V_{OH}	High Level Output Voltage	Source current =20µA ($V_{I/O}$=V_{CC})	0.8× V_{DD}	-	-	V
	Rise/Fall Time	Loaded with 50pF (10% to 90%)	-	125	500	ns
EN, RSTIN, CLKIN, VSEL						
V_{IL}	Low Input Threshold	-	-	-	0.2× V_{DD}	V
V_{IH}	High Input Threshold	-	0.8× V_{DD}	-	-	V
I_{IL} (I_{IH})	Input Current	-	-100	-	100	nA

Function Block Diagram



Function Description

V_{DD} (Pin 3): Power. Supply voltage and reference voltage for the control logic section.

V_{BAT} (Pin 5): Power. The supply voltage input of analog sections.

V_{CC} (Pin 7): Power supply output to the card socket V_{CC} pins and can be set to 1.8V or 3V via the V_{SEL} input. EN controls the V_{CC} turn on or turn off.

CLK (Pin 11): Clock output to the card socket CLK pin and the clock signal is derived from the CLKIN pin with level shift functions. The CLK pin is gated off until V_{CC} attain its correct value. This pin is pulled to ground during shutdown. Fast rising and falling edges necessitate careful board layout for the CLK node.

RST (Pin 14): Reset output to the card socket RST pin and the reset signal is derived from the RSTIN pin with level shift function. The RST pin is shutdown until V_{CC} attain its correct value. This pin is pulled to ground during shutdown.

I/O (Pin 8): Data output/input to the card socket I/O pin, transmit /receive data to/from the DATA pin with level shift function. The I/O pin is gated off until V_{CC} attain its correct value. The SIM card output must be on an open-drain driver capable of sourcing>1mA.

DATA (Pin 8): Input/Output. Connect this pin to microcontroller side I/O pin. The DATA pin provides the bidirectional communication path to card. The pin possesses a weak pull-up, allowing the controller to use an open drain output with capable of sinking greater than 1mA and maintain a HIGH state during shutdown, as long as V_{DD} is powered.

RSTIN (Pin 14): Input. Supply the reset signal to the card through RST. It is level shifted and transmitted directly to the RST pin of the selected card.

CLKIN (Pin 13): Input. Supply the clock signal to the card through CLK. It is level shifted and transmitted directly to the CLK

pin of the card.

EN (Pin 1): Input. EN pin enable and disable V_{CC}. RST, CLK, I/O pins are shutdown until V_{CC} attain its correct value.

V_{SEL} (Pin 2): Input. The V_{SEL} selects the voltage level of V_{CC}. Bring it LOW selects V_{CC}=1.8V while driving this pin HIGH selects V_{CC}= 3V. Details please see **V_{SEL} Truth Table**.

GND (Pin 10): Chip Ground. This pad must be soldered directly to a PCB ground plane.
EXPOSED PAD (Pin 17): Chip Ground. This pad must be soldered on PCB.

The PI4ULS5V4555 features regulated power 1.8V and 3V to SIM/Smart Card, and it has internal level shift function to allow low voltage controllers to interface with 1.8V and 3V SIMs or smart cards. The device meet ETSI, IMT-2000, and ISO7816 requirements for SIM and Smart card interface.

Bidirectional Channels

The bidirectional channel is level shifted to the appropriate V_{CC} voltages at the I/O pin. An NMOS pass transistor performs the level shifting. The gate of the NMOS transistor is biased such that the transistor is completely off when both sides have relinquished the channel. If I/O pin asserts a LOW, then the transistor will convey LOW to the other side.

When V_{CC} powered ok, it becomes a candidate to drive data on the DATA pin and likewise receive data from the DATA pin. When EN turns LOW and shut down the device, the communication with the DATA pin will be disabled and the DATA pin will be pulled HIGH by internal resistor to V_{DD}, as long as V_{DD} is powered.

Level Translators

The CLK and RST lines to SIM are level shifted from the controller supply (V_{DD} to GND) to the SIM supply (V_{CC} to GND). The data input to SIM requires an open-drain output on the controller. On-chip pull-up current sources are provided for both the DATA and I/O lines.

Fault Detection

The V_{CC}, I/O, RST, CLK and DATA pins are all protected against short-circuit faults. While there are no logic outputs to indicate that a fault has occurred, these pins will be able to tolerate the fault condition until it has been removed.

The V_{CC}, I/O, RST, CLK and DATA pins possess fault protection circuitry which will limit the current available to the pins. Each V_{CC} pin is capable of supplying approximately 50mA (typ.) before the output voltage is reduced.

The CLK pin is designed to tolerate faults by reducing the current drive capability of their output stages. After a fault is detected by the internal fault detection logic, the logic waits for a fault detection delay to elapse before reducing the current drive capability of the output stage. The reduced current drive allows the PI4ULS5V4555 to detect when the fault has been removed.

Capacitor Selection

A total of four capacitors are required for proper bypassing of the PI4ULS5V4555. An input bypass capacitor is required at V_{BAT} and V_{DD}.

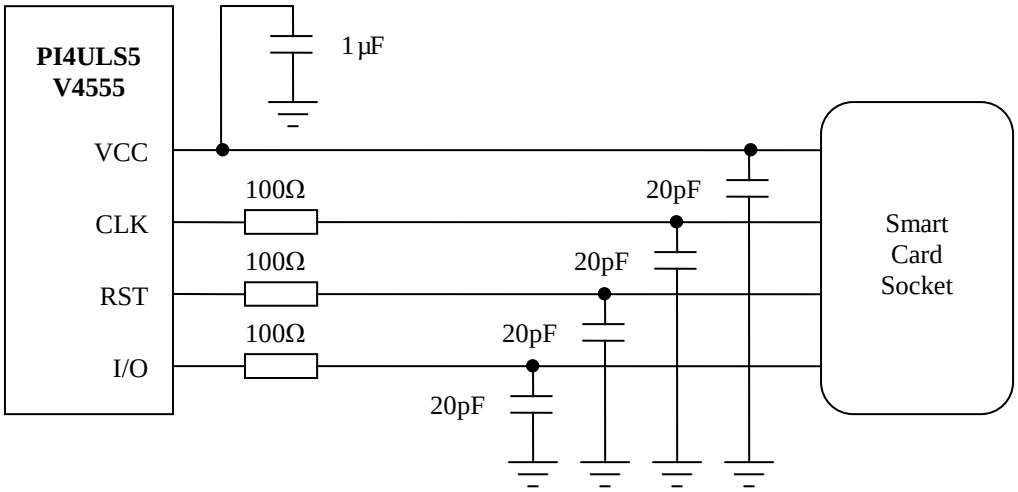
Output bypass capacitors are required on each of the Smart Card V_{CC} pins. Due to their extremely low equivalent series resistance (ESR), only multilayer ceramic chip capacitors should be used to ensure proper stability and ESD protection.

There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R/X5R ceramic capacitors have excellent voltage and temperature stability but relatively low packing density. Y5V ceramic capacitors have apparently higher packing density but poor performance over their rated voltage or temperature ranges. Under certain voltage and temperature conditions Y5V and X7R/X5R ceramic capacitors can be compared directly by case size rather than specified value for a desired minimum capacitance.

The V_{CC} outputs should be bypassed to GND with a 1μF capacitor. V_{DD} and V_{BAT} outputs should be bypassed to GND with a 0.1μF capacitor. Capacitors should be placed as close to the device as possible for improved ESD tolerance.

Compliance Testing

Inductance due to long leads on type approval equipment can cause ringing and overshoot that leads to testing problems. Small amounts of capacitance and damping resistors can be included in the application without compromising the normal electrical performance of the PI4ULS5V4555 or Smart Card system. Generally a 100Ω resistor and a 20pF capacitor will accomplish this, as shown in below.

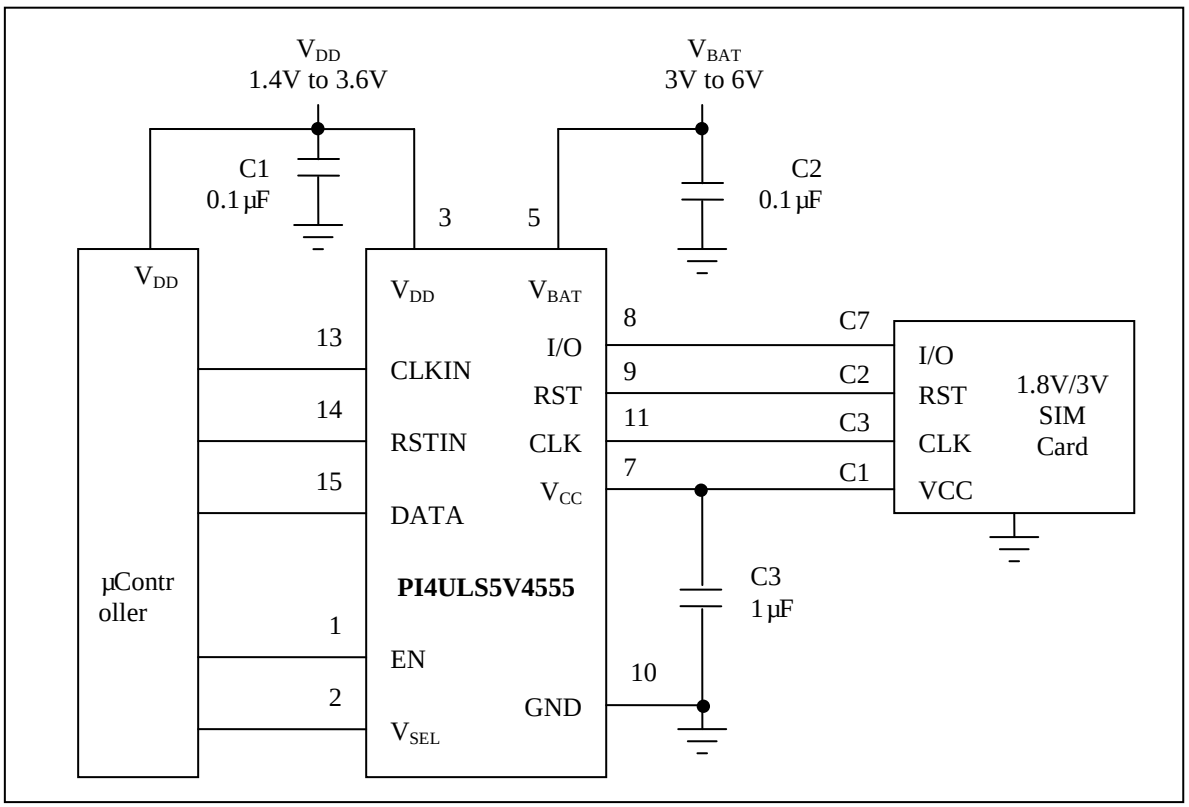


Additional Components for Improved Compliance Testing

Shutdown Modes

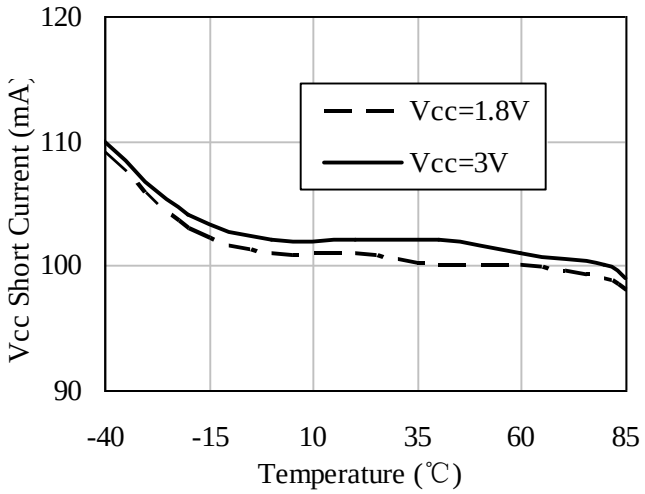
The device can enter to shutdown mode by EN pin. Bring EN pin to LOW directly shutdown the device. The shutdown current is less than 1µA.

Application Circuit

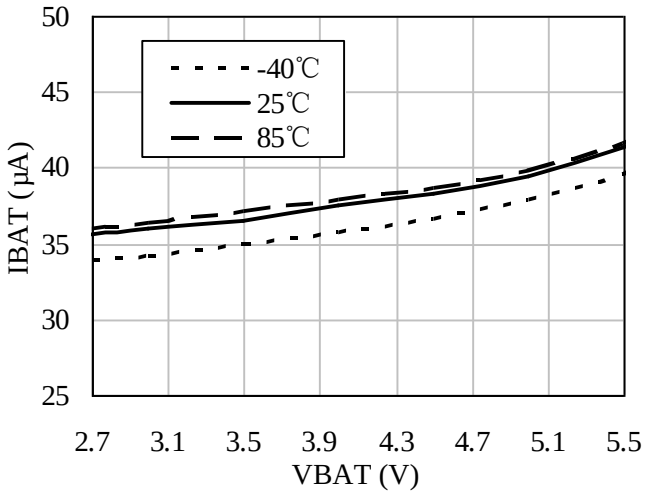


Typical Performance Characteristics

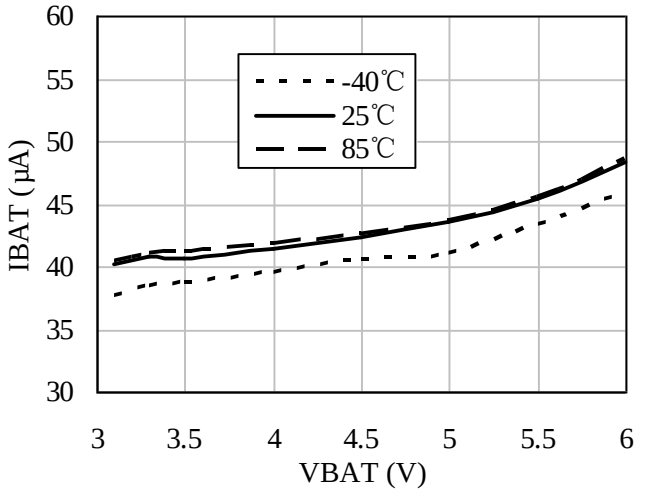
V_{CC} Short-circuit Current vs. Temperature



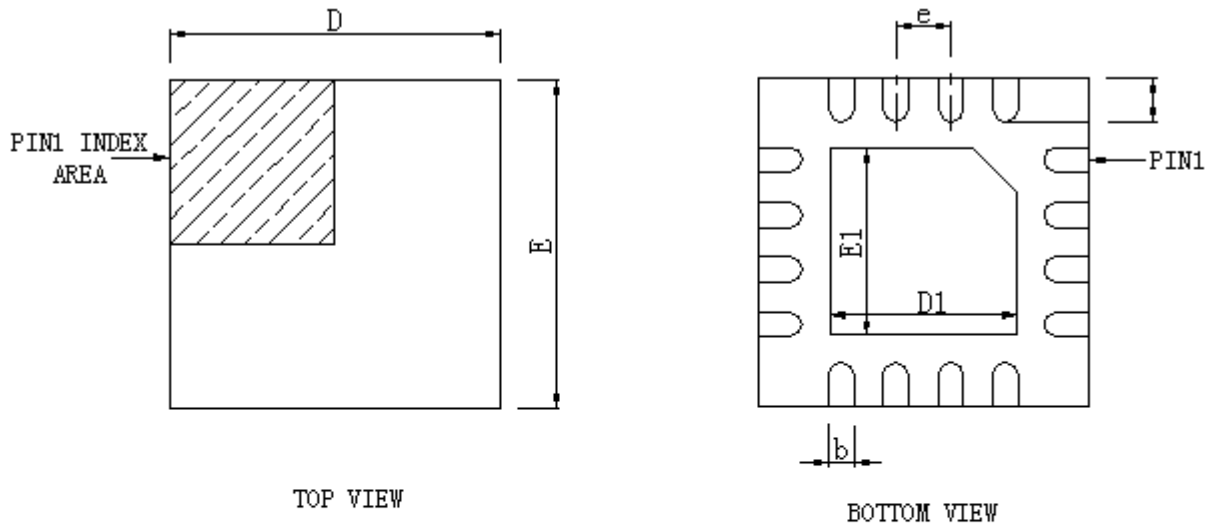
Supply Current I_{BAT} vs. Supply Voltage V_{BAT} (V_{CC}=1.8V)

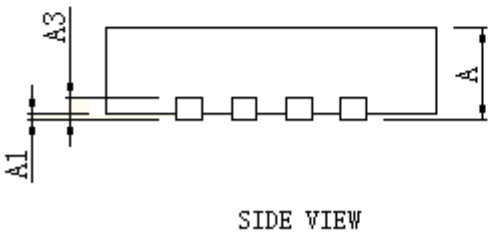


No load Supply Current I_{BAT} vs. Supply Voltage V_{BAT} (V_{CC}=3.0V)



Mechanical Information





Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-220J

PKG. DIMENSIONS(MM)		
SYMBOL	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
A3	0.203REF	
D	2.900	3.100
E	2.900	3.100
D1	1.600	1.800
E1	1.600	1.800
b	0.180	0.300
e	0.500TYP	
L	0.300	0.500

Ordering Information

Part Number	Package Code	Package
PI4ULS5V4555ZHE	ZH	Lead Free and Green TQFN-16 3mmx3mm (ZH)

Notes:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel