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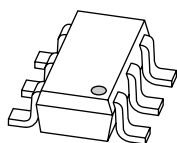
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Kind regards,

Team Nexperia



# PIMC31

500 mA, 50 V NPN/PNP double resistor-equipped transistor;  
 $R1 = 1\text{ k}\Omega$ ,  $R2 = 10\text{ k}\Omega$

Rev. 01 — 24 March 2009

Product data sheet

## 1. Product profile

### 1.1 General description

500 mA, 50 V NPN/PNP double Resistor-Equipped Transistor (RET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PIMN31

### 1.2 Features

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

### 1.3 Applications

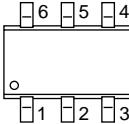
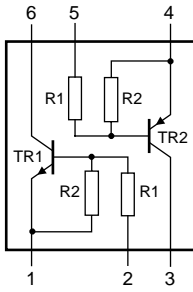
- Digital application in automotive and industrial segments
- Switching loads

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
$V_{CEO}$	collector-emitter voltage	open base	-	-	50	V
$I_O$	output current		-	-	500	mA
R1	bias resistor 1 (input)		0.7	1	1.3	$\text{k}\Omega$
R2/R1	bias resistor ratio		9	10	11	

2. Pinning information

Table 2. Pinning			
Pin	Description	Simplified outline	Graphic symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		
			006aaa143

3. Ordering information

Table 3. Ordering information			
Type number	Package		
	Name	Description	Version
PIMC31	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes	
Type number	Marking code
PIMC31	ZH

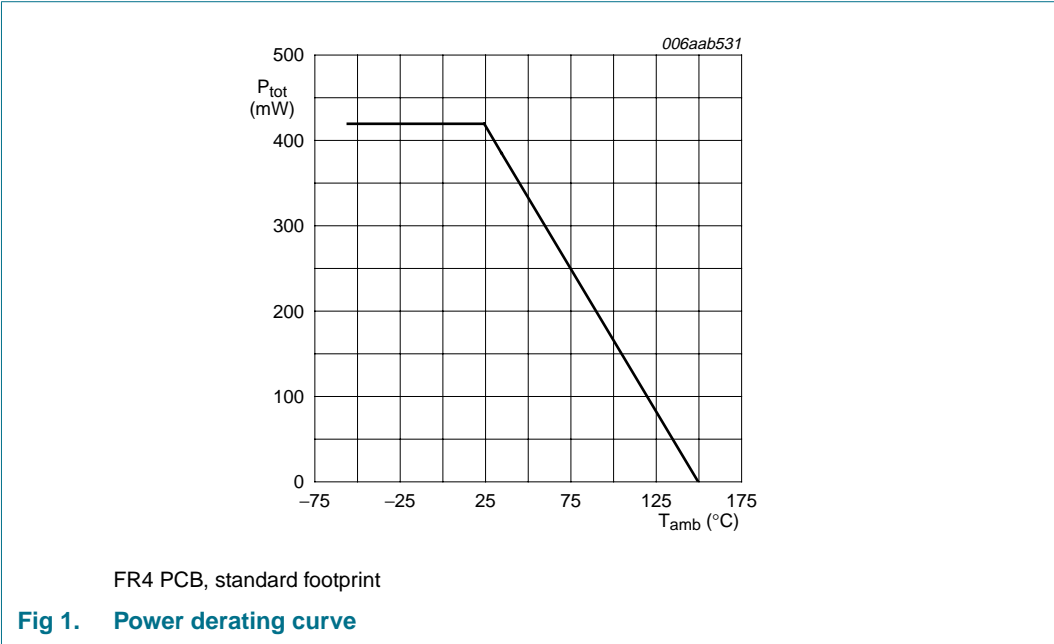
5. Limiting values

Table 5. Limiting values					
In accordance with the Absolute Maximum Rating System (IEC 60134).					
Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity					
V <sub>CBO</sub>	collector-base voltage	open emitter	-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	-	5	V
V <sub>I</sub>	input voltage TR1				
	positive		-	+10	V
	negative		-	-5	V
	input voltage TR2				
	positive		-	+5	V
	negative		-	-10	V

Table 5. Limiting values ...continued  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I <sub>O</sub>	output current		-	500	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	290	mW
Per device					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	420	mW
T <sub>j</sub>	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-55	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

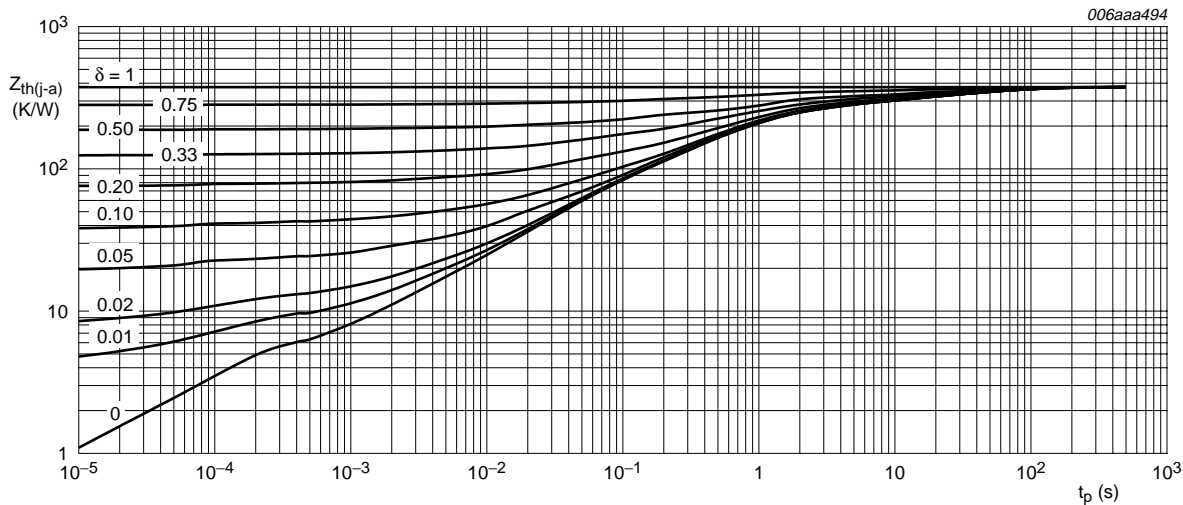


6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	431	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point		-	-	105	K/W
Per device						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	298	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



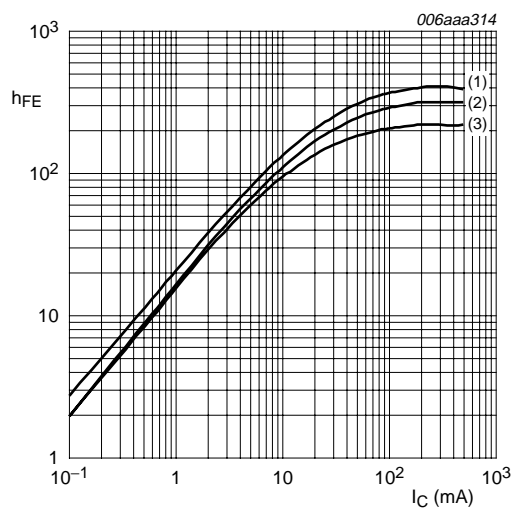
FR4 PCB, standard footprint

Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

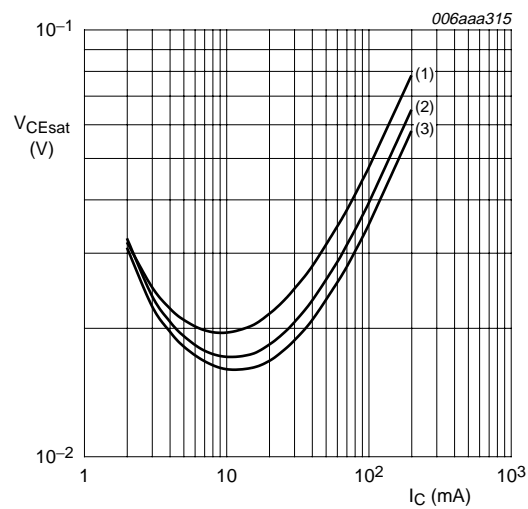
Table 7. Characteristics  
*T<sub>amb</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A	-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 50 V; I <sub>B</sub> = 0 A	-	-	0.5	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	-	-	0.72	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 50 mA	70	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 50 mA; I <sub>B</sub> = 2.5 mA	-	-	0.3	V
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA	0.3	0.6	1	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 20 mA	0.4	0.8	1.4	V
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		9	10	11	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A; f = 1 MHz				
	TR1 (NPN)		-	7	-	pF
	TR2 (PNP)		-	11	-	pF



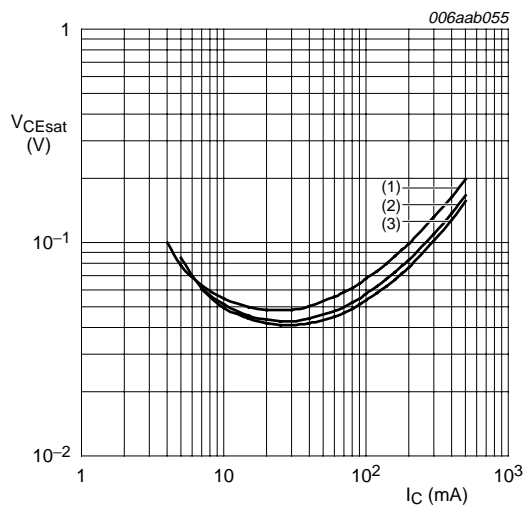
- $V_{CE} = 5\text{ V}$
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 3. TR1 (NPN): DC current gain as a function of collector current; typical values



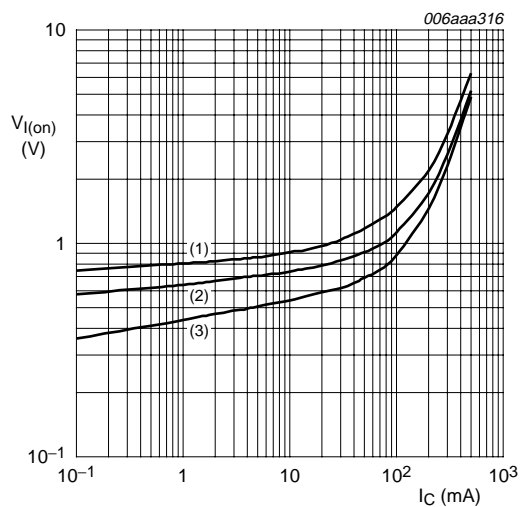
- $I_C/I_B = 20$
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



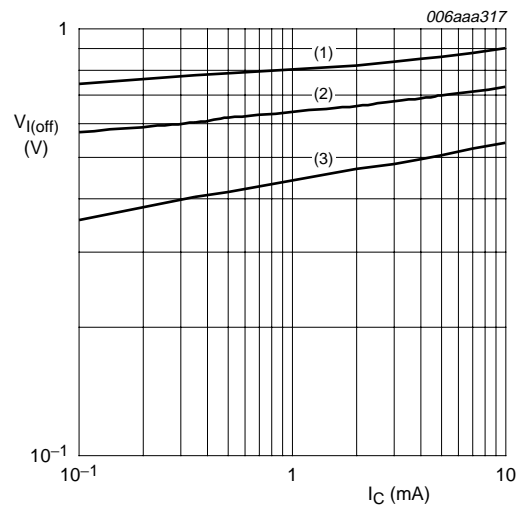
- $I_C/I_B = 50$
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



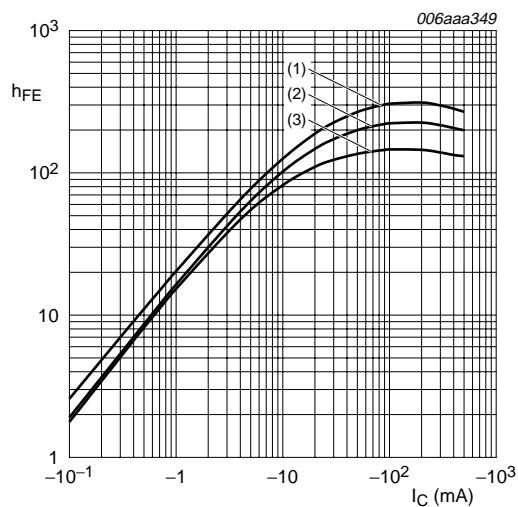
$V_{CE} = 0.3\text{ V}$   
(1)  $T_{amb} = -40^\circ\text{C}$   
(2)  $T_{amb} = 25^\circ\text{C}$   
(3)  $T_{amb} = 100^\circ\text{C}$

Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values



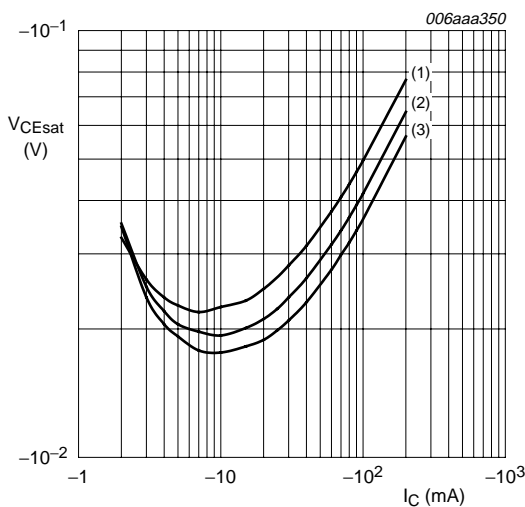
$V_{CE} = 5\text{ V}$   
(1)  $T_{amb} = -40^\circ\text{C}$   
(2)  $T_{amb} = 25^\circ\text{C}$   
(3)  $T_{amb} = 100^\circ\text{C}$

Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



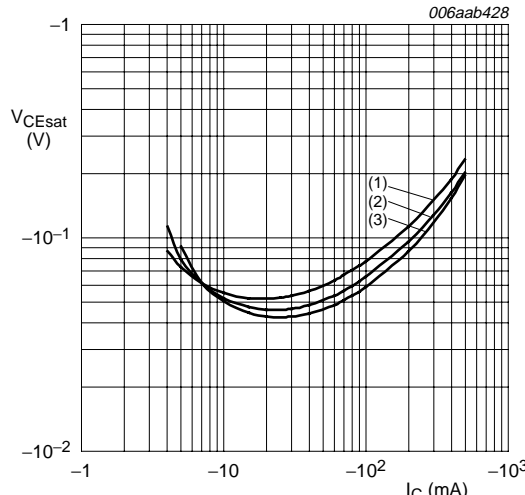
$V_{CE} = -5\text{ V}$   
(1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 8. TR2 (PNP): DC current gain as a function of collector current; typical values



$I_C/I_B = 20$   
(1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

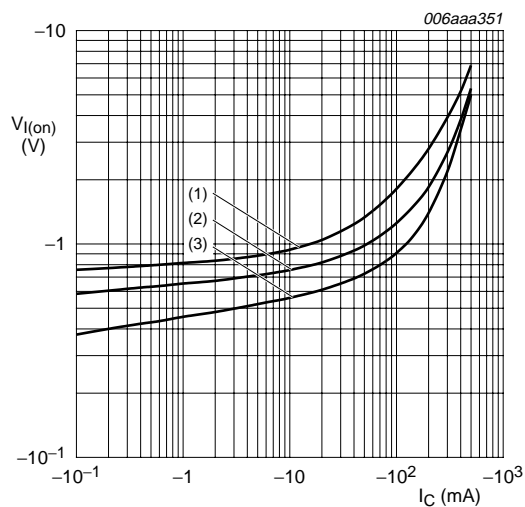
Fig 9. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 50$   
(1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

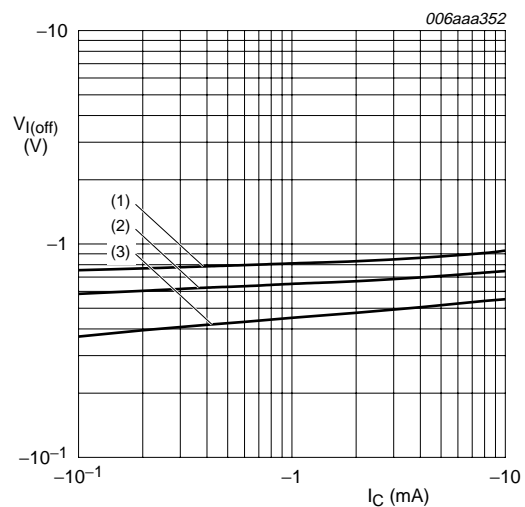
Fig 10. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values





$V_{CE} = -0.3\text{ V}$   
(1)  $T_{amb} = -40^\circ\text{C}$   
(2)  $T_{amb} = 25^\circ\text{C}$   
(3)  $T_{amb} = 100^\circ\text{C}$

Fig 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values



$V_{CE} = -5\text{ V}$   
(1)  $T_{amb} = -40^\circ\text{C}$   
(2)  $T_{amb} = 25^\circ\text{C}$   
(3)  $T_{amb} = 100^\circ\text{C}$

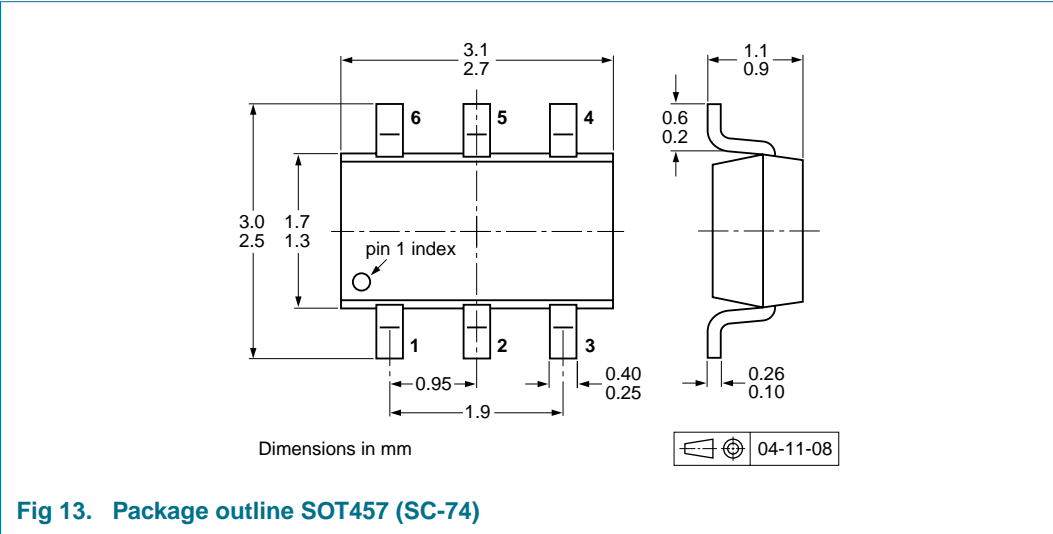
Fig 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

**Table 8. Packing methods**  
The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity	
			3000	10000
PIMC31	SOT457	4 mm pitch, 8 mm tape and reel; T1	<sup>[2]</sup> -115	-135
		4 mm pitch, 8 mm tape and reel; T2	<sup>[3]</sup> -125	-165

[1] For further information and the availability of packing methods, see [Section 14](#).  
[2] T1: normal taping  
[3] T2: reverse taping

11. Soldering

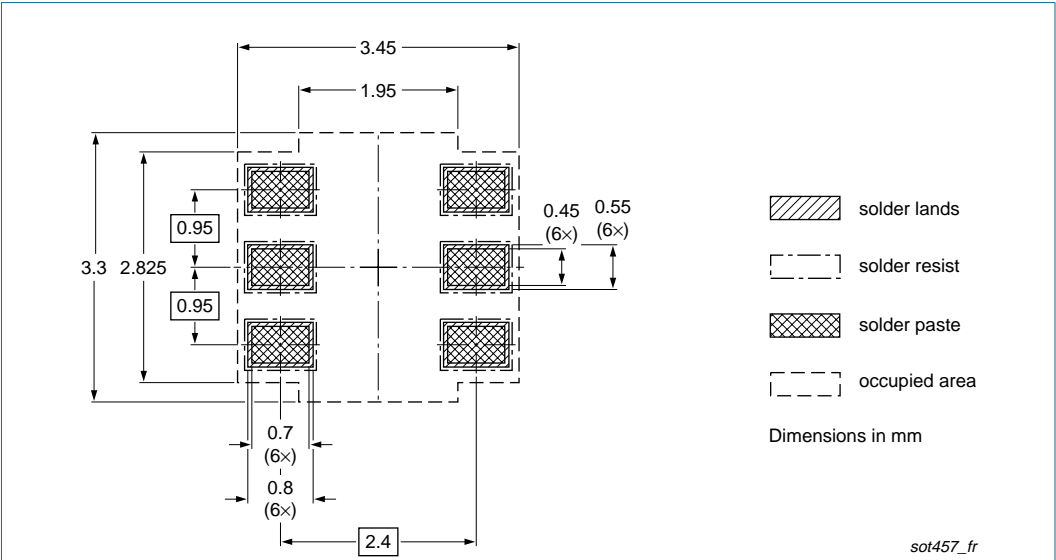


Fig 14. Reflow soldering footprint SOT457 (SC-74)

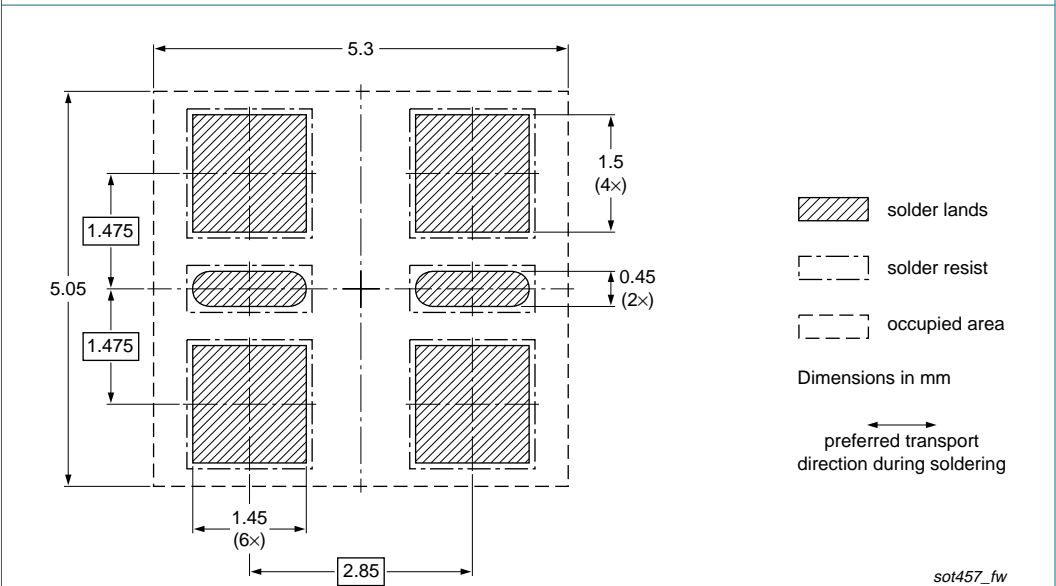


Fig 15. Wave soldering footprint SOT457 (SC-74)

## 12. Revision history

**Table 9.** Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PIMC31_1	20090324	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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