PM4332

TE-32

High Density 32 Channel T1/E1/J1 Framer

Data Sheet

Proprietary and Confidential

Released

Issue No. 5: June 2002

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PMC-2011402 (R5), (PMC-2010716 (R5)

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Revision History

Issue No.	Issue Date	Details of Change
1	June ‘01	Initial release.
2	Sep ‘01	Changes applicable to TE-32 Rev A device.
3	Feb ‘02	Changes for GCA. Incorporated TE-32 Rev A documentation errata items.
4	April ‘02	Changes for Revision B. Change bars relative to issue 3.
5	June ‘02	Updates for Production release. Change bars relative to issue 4.

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1 Features

- High Density 32 channel T1/E1/J1 framer.
- Software selectable between T1/J1 or E1 operation on a per device basis.
- Supports 8 Mbit/s H-MVIP on the system interface for all T1 or E1 links, a separate 8 Mbit/s H-MVIP system interface for all T1 or E1 CAS channels and a separate 8 Mbit/s H-MVIP system interface for all T1 or E1 CCS and V5.1/V5.2 channels.
- Supports a byte serial Scaleable Bandwidth Interconnect (SBI) bus interface for high density system side device interconnection of up to 32 T1 streams, 32 E1 streams.
- Provides jitter attenuation in the T1 or E1 receive and transmit directions.
- Provides per link diagnostic and line loopbacks.
- Also provides PRBS generators and detectors on each tributary for error testing at DS1, E1 and NxDS0 rates as recommended in ITU-T O.151 and O.152.
- Provides a generic 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 1.8V/3.3V CMOS technology. All pins are 5V tolerant.
- 324-pin fine pitch PBGA package (23mm x 23mm). Supports industrial temperature range (-40 ^{o}C to 85 ^{o}C) operation.
- Line side interface is SBI bus.
- System side interface is either H-MVIP or SBI bus.

Each one of 32 T1 receiver sections

- Frames to DS-1 signals in SF, SLC®96 and ESF formats.
- Frames to TTC JT-G.704 multiframe formatted J1 signals. Supports the alternate CRC-6 calculation for Japanese applications.
- Provides Red, Yellow, and AIS alarm integration.
- Supports RAI-CI and AIS-CI alarm detection and generation.
- Provides ESF bit-oriented code detection and an HDLC/LAPD interface for terminating the ESF facility data link.
- Provides Inband Loopback Code generation and detection.
- Indicates signaling state change, and two superframes of signaling debounce on a per-DS0 basis.
- Provides an HDLC interface with 127 bytes of buffering for terminating the facility data link.

- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.
- Provides an optional elastic store, which may be used to time the ingress streams to a common clock and frame alignment in support of a H-MVIP interface.
- Provides DS-1 robbed bit signaling extraction and insertion, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and two superframes of signaling debounce on a per-channel basis.
- A pseudo-random sequence user selectable from $2^7 - 1$, $2^{11} - 1$, $2^{15} - 1$ or $2^{20} - 1$, may be detected in the T1 stream in either the ingress or egress directions. The detector counts pattern errors using a 16-bit non-saturating PRBS error counter. The pseudo-random sequence can be the entire T1 or any combination of DS0s within a framed T1.
- Frames in the presence of and detects the "Japanese Yellow" alarm.

Each one of 32 E1 receiver sections

- Frames to ITU-T G.704 basic and CRC-4 multiframe formatted E1 signals. The framing procedures are consistent ITU-T G.706 specifications.
- Provides an HDLC interface with 127 bytes of buffering for terminating the national use bit data link.
- Extracts 4-bit codewords from the E1 national use bits as specified in ETS 300 233.
- V5.2 link indication signal detection.
- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.
- Provides a two-frame elastic store buffer for backplane rate adaptation that performs controlled slips and indicates slip occurrence and direction.
- Frames to the E1 signaling multiframe alignment when enabled and extracts channel associated signaling. Alternatively, a common channel signaling data link may be extracted from timeslot 16.
- Can be programmed to generate an interrupt on change of signaling state.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- A pseudo-random sequence user selectable from $2^7 - 1$, $2^{11} - 1$, $2^{15} - 1$ or $2^{20} - 1$, may be detected in the E1 stream in either the ingress or egress directions. The detector counts pattern errors using a 16-bit non-saturating PRBS error counter. The pseudo-random sequence can be the entire E1 or any combination of timeslots within the framed E1.

Each one of 32 T1 transmitter sections

- May be timed to its associated receive clock (loop timing) or may derive its timing from the data rate received at the system interface or a common transmit clock; the transmit line clock may be synthesized from an N*8 kHz reference.
- Provides minimum ones density through Bell (bit 7), GTE or "jammed bit 8" zero code suppression on a per-DS0 basis.
- Provides a 128 byte buffer to allow insertion of the facility data link using the host interface.
- Supports transmission of the alarm indication signal (AIS) or the Yellow alarm signal in SF, SLC®96 and ESF formats.
- Provides transparency for the F-bit to support SLC®96 data link insertion.
- Autonomously transmits an ESF Performance Report Message each second.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter.
- Supports the alternate ESF CRC-6 calculation for Japanese applications.
- A pseudo-random sequence user selectable from $2^7 - 1$, $2^{11} - 1$, $2^{15} - 1$ or $2^{20} - 1$, may be inserted into the T1 stream in either the ingress or egress directions. The pseudo-random sequence can be inserted into the entire T1 or any combination of DS0s within the framed T1.

Each one of 32 E1 transmitter sections

- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.
- Transmits G.704 basic and CRC-4 multiframe formatted E1.
- Supports unframed mode and framing bit, CRC, or data link by-pass.
- Provides signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- A pseudo-random sequence user selectable from $2^7 - 1$, $2^{11} - 1$, $2^{15} - 1$ or $2^{20} - 1$, may be inserted into the E1 stream in either the ingress or egress directions. The pseudo-random sequence can be inserted into the entire E1 or any combination of timeslots within the framed E1.
- Optionally inserts a datalink in the E1 national use bits.
- Supports 4-bit codeword insertion in the E1 national use bits as specified in ETS 300 233
- Supports transmission of the alarm indication signal (AIS) and the remote alarm indication (RAI) signal.

Six full featured T1/E1 Pattern Generators and Detectors

- Each generator and detector pair may be associated with any one of the 32 T1s or E1s.

- Any sub-set of DS0s within a tributary may be selected.
- Provides programmable pseudo-random test sequence generation (up to 2^{32}-1 bit length sequences conforming to ITU-T O.151 standards) or any repeating pattern up to 32 bits. Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

Synchronous System Interfaces

- Provides eight 8 Mbit/s H-MVIP data interfaces for synchronous access to all the DS0s of all 32 T1 links or all timeslots of all 32 E1s.
- Provides eight 8 Mbit/s H-MVIP interfaces for synchronous access to all channel associated signaling (CAS) bits for all T1 DS0s or E1 timeslots. The CAS bits occupy one nibble of every byte on the H-MVIP interfaces and are repeated over the entire T1 or E1 multi-frame.
- Provides three 8 Mbit/s H-MVIP interfaces for common channel signaling (CCS) channels as well as V5.1 and V5.2 channels. In T1 mode DS0 24 is available through this interface. In E1 mode timeslots 15, 16 and 31 are available through this interface. Optionally, timeslot 0 may be presented instead of timeslot 15.
- All links accessed via the H-MVIP interface will be synchronously timed to the common H-MVIP clock and frame alignment signals, CMV8MCLK, CMVFP, CMVFPC.
- H-MVIP access for Channel Associated Signaling is available with the Scaleable Bandwidth Interconnect bus as an optional replacement for CAS access over the SBI bus as well as with the H-MVIP data interface. Common Channel Signaling H-MVIP access is available with the SBI bus, serial PCM and H-MVIP data interfaces.
- Alarm status, T1 F-bit and inband signaling control is available using otherwise unused bit positions.
- Compatible with H-MVIP PCM backplanes supporting 8.192 Mbit/s.

Scaleable Bandwidth Interconnect (SBI) Bus

- Provides a high density byte serial interconnect for all TE-32 links. Utilizes an Add/Drop configuration to asynchronously multiplex up to 32 T1s or 32 E1s with multiple payload or link layer processors.
- External devices can access framed T1s and framed E1s over this interface.
- Framed T1 access can be selected on a per T1 basis. Framed E1 access can be selected on a per E1 basis.
- At the system interface, synchronous access for T1 DS0 channels or E1 timeslots is supported in a locked format mode. Selectable on a per tributary basis.
- At the system interface, channel associated signaling bits for channelized T1 and E1 are explicitly identified across the bus.
- Transmit timing is mastered either by the TE-32 or a layer 2 device connecting to the system interface SBI bus. Timing mastership is selectable on a per tributary basis, where a tributary is either an individual T1, E1.

- The line side SBI bus provides a time switch capability in support of redundancy.
- The system side SBI operates at either 19.44 MHz or 77.76 MHz. The line side SBI operates at 19.44 MHz.

2 Applications

- Multiservice Switches
- Voice Gateways
- Wireless Base Station Controllers
- Edge Routers
- Multiservice Add-Drop Multiplexers
- Digital Access Cross-Connect Systems

3 References

- American National Standard for Telecommunications – Digital Hierarchy – Formats Specification, ANSI T1.107-1995
- American National Standard for Telecommunications – Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring, ANSI T1.231-1997
- American National Standard for Telecommunications – Carrier to Customer Installation – DS-1 Metallic Interface Specification, ANSI T1.403-1999
- American National Standard for Telecommunications – Integrated Services Digital Network (ISDN) Primary Rate- Customer Installation Metallic Interfaces Layer 1 Specification, ANSI T1.408-1990
- Bell Communications Research, TR–TSY-000009 – Asynchronous Digital Multiplexes Requirements and Objectives, Issue 1, May 1986
- Bell Communications Research – DS-1 Rate Digital Service Monitoring Unit Functional Specification, TA-TSY-000147, Issue 1, October, 1987
- Bell Communications Research – Alarm Indication Signal Requirements and Objectives, TR-TSY-000191 Issue 1, May 1986
- Bell Communications Research – Wideband and Broadband Digital Cross-Connect Systems Generic Criteria, TR-NWT-000233, Issue 3, November 1993
- Bell Communications Research – Digital Interface Between The SLC®96 Digital Loop Carrier System And A Local Digital Switch, TR-TSY-000008, Issue 2, August 1987
- Bell Communications Research – Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface, TR-NWT-000303, Issue 2, December, 1992
- Bell Communications Research – Transport Systems Generic Requirements (TSGR): Common Requirement, TR-TSY-000499, Issue 5, December, 1993
- Bell Communications Research – OTGR: Network Maintenance Transport Surveillance – Generic Digital Transmission Surveillance, TR-TSY-000820, Section 5.1, Issue 1, June 1990
- AT&T – Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, TR 54016, September 1989.
- AT&T – Accunet T1.5 – Service Description and Interface Specification, TR 62411, December, 1990
- ITU Study Group XVIII – Report R 105, Geneva, 9-19 June 1992
- ETSI – ETS 300 011 – ISDN Primary Rate User-Network Interface Specification and Test Principles, 1992.
- ETSI – ETS 300 233 – Access Digital Section for ISDN Primary Rates, May 1994
- ETSI – ETS 300 324-1 – Signaling Protocols and Switching (SPS); V interfaces at the Digital Local Exchange (LE) V5.1 Interface for the Support of Access Network (AN) Part 1: V5.1 Interface Specification, February, 1994.

- ETSI – ETS 300 347-1 – Signaling Protocols and Switching (SPS); V Interfaces at the Digital Local Exchange (LE) V5.2 Interface for the Support of Access Network (AN) Part 1: V5.2 Interface Specification, September 1994.
- ITU-T – Recommendation G.704 – Synchronous Frame Structures Used at Primary Hierarchical Levels, July 1995.
- ITU-T – Recommendation G.706 – Frame Alignment and CRC Procedures Relating to G.704 Frame Structures, 1991.
- ITU-T – Recommendation G.732 – Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s, 1993.
- ITU-T Recommendation G.775, - Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria, 11/94
- ITU-T Recommendation G.823, - The Control of Jitter and Wander within Digital Networks which are Based on the 2048 kbit/s Hierarchy, 03/94
- ITU-T Recommendation G.964, - V-Interfaces at the Digital Local Ex–hange (LE) – V5.1 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), June 1994.
- ITU-T Recommendation G.965, - V-Interfaces at the Digital Local Ex–hange (LE) – V5.2 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), March 1995.
- ITU-T – Recommendation I.431 – Primary Rate User-Network Interface – Layer 1 Specification, 1993.
- ITU-T Recommendation O.151 – Error Performance Measuring Equipment Operating at the Primary Rate and Above, October 1992
- ITU-T Recommendation O.152 – Error Performance Measuring Equipment for Bit Rates of 64 kbit/s and N x 64 kbit/s, October 1992
- ITU-T Recommendation O.153 – Basic Parameters for the Measurement of Error Performance at Bit Rates below the Primary Rate, October 1992.
- ITU-T Recommendation Q.921 – ISDN User-Network Interface Data Link Layer Specification, March 1993
- International Organization for Standardization, ISO 3309:1984 – High-Level Data Link Control procedures – Frame Structure
- TTC Standard JT-G704 – Frame Structures on Primary and Secondary Hierarchical Digital Interfaces, 1995.
- TTC Standard JT-G706 – Frame Synchronization and CRC Procedure
- TTC Standard JT-I431 – ISDN Primary Rate User-Network Interface Layer 1 – Specification, 1995.
- Nippon Telegraph and Telephone Corporation – Technical Reference for High-Speed Digital Leased Circuit Services, Third Edition, 1990.
- GO-MVIP, Multi-Vendor Integration Protocol, MVIP-90, Release 1.1, 1994
- GO-MVIP, H-MVIP Standard, Release1.1a, 1997

4 Application Examples

Figure 1 Edge Router Line Card

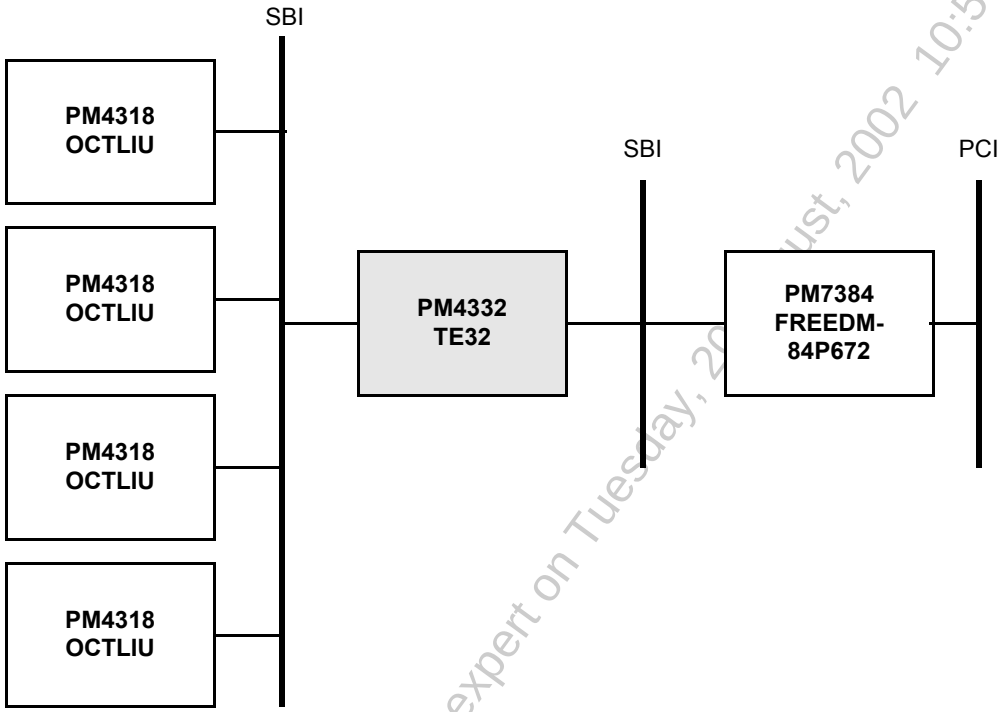


Figure 1 illustrates a 32-Channel T1/E1/J1 Edge Router Line Card using the FREEDM-84P672 (PM7384) and the OCTLIU (PM4318).

Figure 2 Multiservice Switch

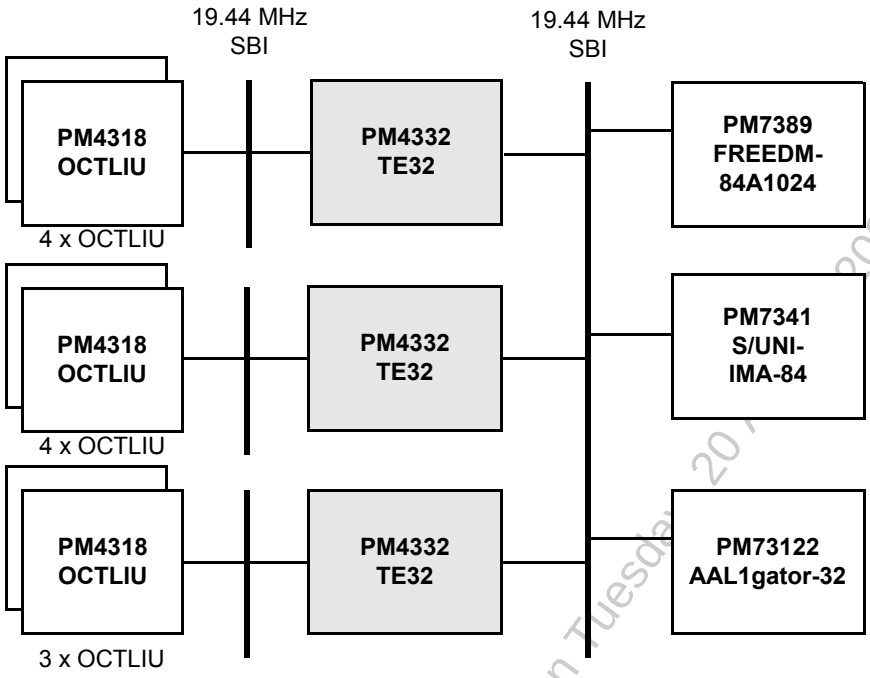


Figure 2 illustrates how frame relay (FREEDM-84A1024), circuit emulation (AAL1gator-32) and ATM inverse multiplexing (S/UNI-IMA-84) may all be supported on a single platform using a common SBI bus as the enabling technology. A high density T1/E1/J1 line interface is provided through an SBI bus connection to the OCTLIU (PM4318). Refer to 12.1 for details on connecting multiple TE-32s to the same system SBI bus.

Figure 3 Voice Gateway Application

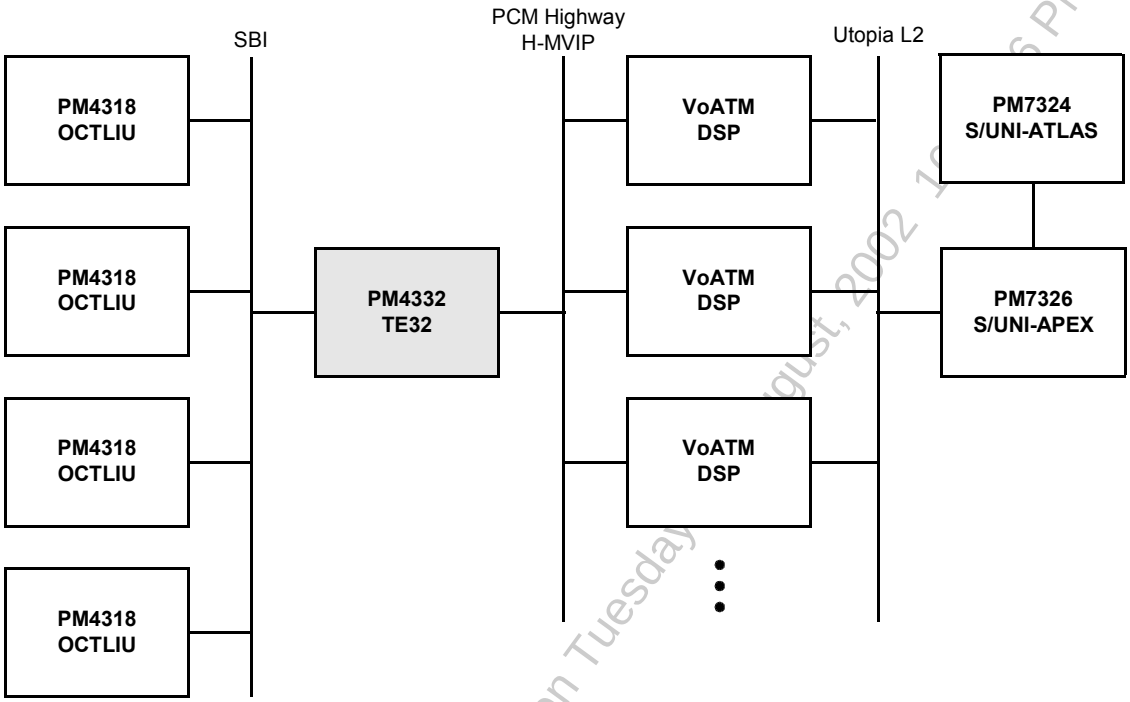
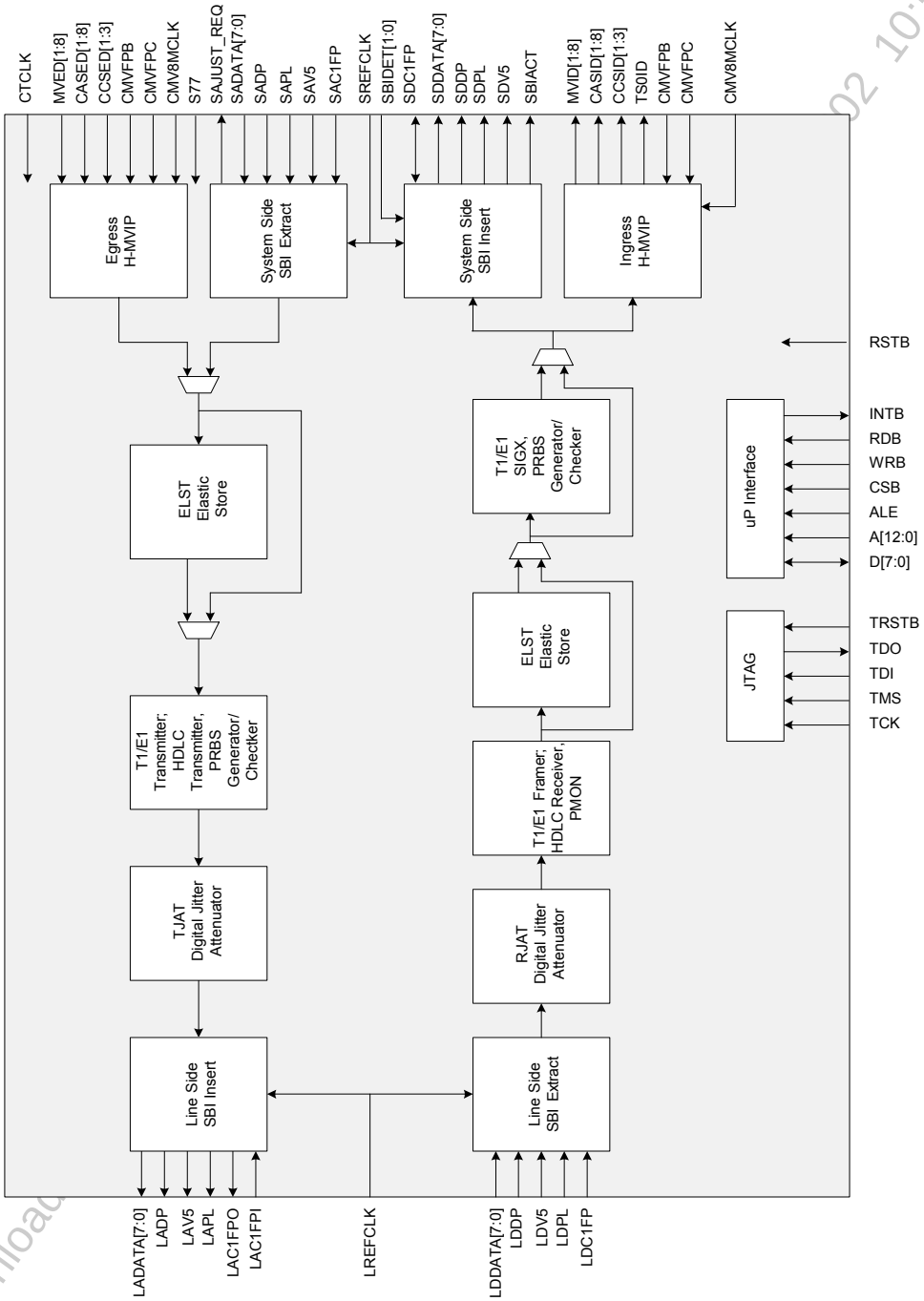


Figure 3 illustrates a typical voice gateway application using VoATM processing and ATM traffic management (PM7326, PM7324).

5 Block Diagram

Figure 4 TE-32 Block Diagram



6 Description

The PM4332 High Density 32 Channel T1/E1 Framer is a feature-rich device for use in any application requiring high density framing of T1/J1 and E1 links.

Each of the T1 and E1 framers and transmitters is independently software configurable, allowing timing master and feature selection without changes to external wiring. However, mixed framing modes are not supported. The framers must be all configured for either T1 or E1 framing.

6.1 T1 Operation

In the ingress direction, each of the 32 T1 links is extracted from the Scaleable Bandwidth Interconnect (SBI) bus. A Scaleable Bandwidth Interconnect (SBI) high density byte serial line interface provides higher levels of integration and dense interconnect. Each T1 framer detects the presence of Yellow and AIS patterns and also integrates Yellow, Red, and AIS alarms.

T1 performance monitoring with accumulation of CRC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided. The TE-32 also detects the presence of ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. The HDLC messages are terminated in a 127 byte FIFO. An elastic store that optionally supports slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The TE-32 also supports inband loopback code generation and detection, idle code substitution, digital milliwatt code insertion, data link extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation and detection on a per-DS0 basis.

In the egress direction, framing is generated for 32 T1s into an SBI add bus. A Scaleable Bandwidth Interconnect (SBI) high density byte serial line interface provides higher levels of integration and dense interconnect. Each T1 transmitter frames to SF or ESF DS1 formats, or framing can be optionally disabled. The TE-32 supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion and zero-code suppression on a per-DS0 basis. PRBS generation and detection is supported on a framed and unframed T1 basis.

6.2 E1 Operation

In the ingress direction, each of the 32 E1 links is extracted from Scaleable Bandwidth Interconnect (SBI). Each E1 framer detects and indicates the presence of remote alarm and AIS patterns and also integrates Red and AIS alarms.

The E1 framers support detection of various alarm conditions such as loss of frame, loss of signaling multiframe and loss of CRC multiframe. The E1 framers also support reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and time slot 16 alarm indication signal.

E1 performance monitoring with accumulation of CRC-4 errors, far end block errors and framing bit errors is provided. The TE-32 provides a receive HDLC controller for the detection and termination of messages on the national use bits. Detection of the 4-bit Sa-bit codewords defined in ITU-T G.704 and ETSI 300-233 is supported. V5.2 link ID signal detection is also supported. An interrupt may be generated on any change of state of the Sa codewords. An elastic store for slip buffering and rate adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

In the egress direction, framing is generated for 32 E1s into SBI add bus. Each E1 transmitter generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled. Transmission of the 4-bit Sa codewords defined in ITU-T G.704 and ETSI 300-233 is supported. PRBS generation or detection is supported on a framed and unframed E1 basis.

6.3 General Operation

The TE-32 can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path.

In synchronous backplane systems, 8 Mbit/s H-MVIP interfaces are provided for access to 768 DS0 channels, channel associated signaling (CAS) for all 768 DS0 channels and common channel signaling (CCS) for all 32 T1s or 32 E1s (or combination thereof). The CCS signaling H-MVIP interface is independent of the DS0 channel and CAS H-MVIP access. The use of any of the H-MVIP interfaces requires that common clocks and frame pulse be used along with T1 slip buffers.

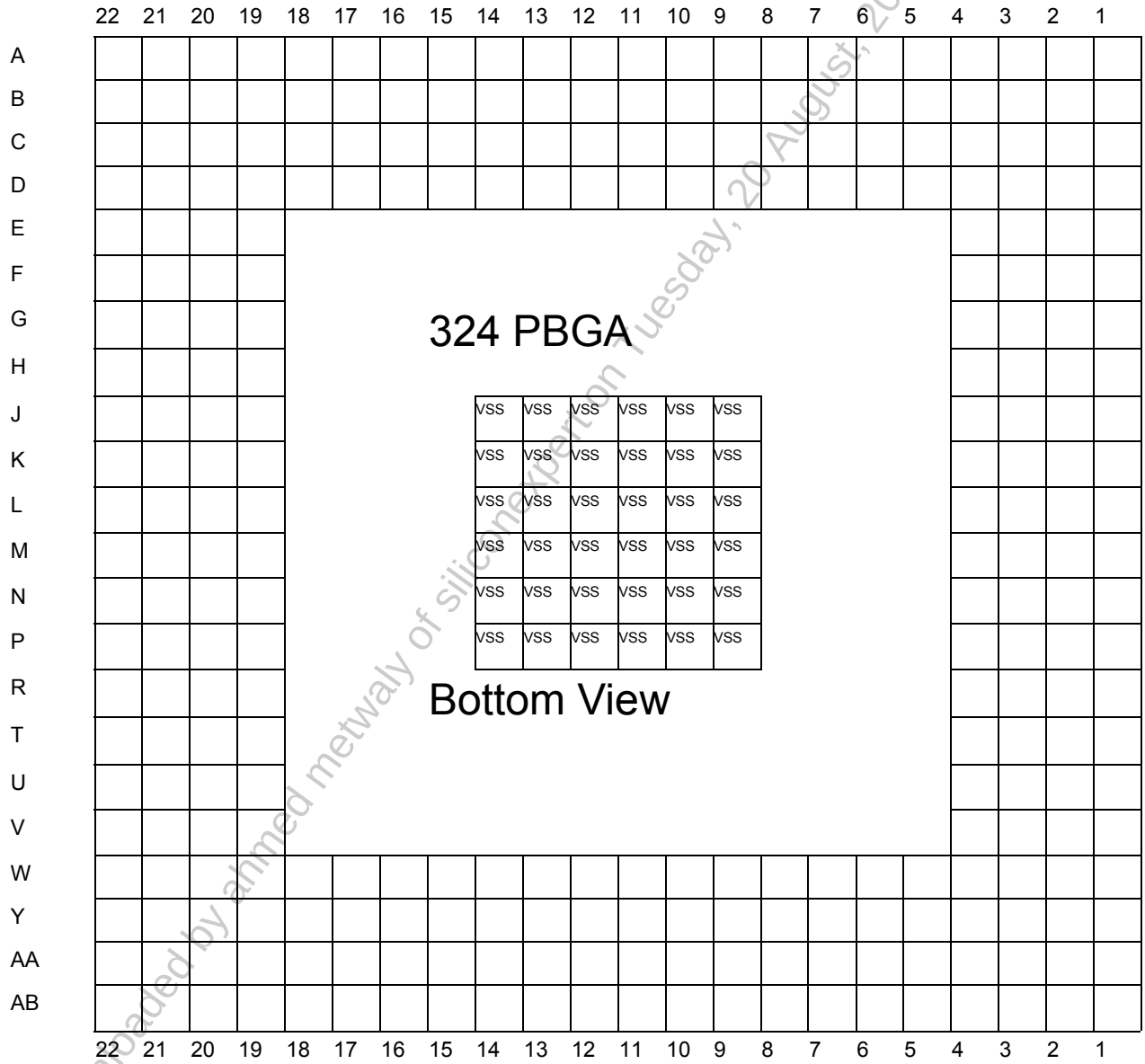
A Scaleable Bandwidth Interconnect (SBI) high density byte serial system interface provides higher levels of integration and dense interconnect. The SBI bus interconnects up to 32 T1s or E1s both synchronously or asynchronously. The SBI allows transmit timing to be mastered by either the TE-32 or link layer device connected to the system SBI bus. Error event accumulation is also provided by the TE-32. Framing bit errors, and far end block errors are accumulated. Error accumulation continues even while the off-line framers are indicating OOF. The counters are intended to be polled once per second, and are sized so as not to saturate at a 10^{-3} bit error rate. Transfer of count values to holding registers is initiated through the microprocessor interface.

The TE-32 is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

7 Pin Diagram

The TE-32 is packaged in a 324-pin PBGA package having a body size of 23mm by 23mm and a ball pitch of 1.0 mm. The center 36 balls are not used as signal I/Os and are thermal balls. Pin names and locations are defined in the Pin Description Table in section 8. Mechanical information for this package is in section 19.

Figure 5 Pin Diagram



8 Pin Description

Pin Name	Type	Pin No.	Function
H-MVIP System Side Interfaces			
CMV8MCLK	Input	T22	Common 8M H-MVIP Clock (CMV8MCLK). The common 8.192 Mbit/s H-MVIP data provides the data clock for receive and transmit links configured for operation in 8.192 Mbit/s H-MVIP mode. CMV8MCLK is used to sample the MVED[1:8], CASED[1:8] and CCSED[1:3] inputs and update MVID[1:8], CASID[1:8], CCSID[1:3] and TS0ID outputs. CMV8MCLK is nominally a 50% duty cycle clock with a frequency of 16.384 MHz. The H-MVIP interfaces are enabled via the SYSOPT[1:0] bits in the Global Configuration register. If the TE-32 is not configured for H-MVIP operation, this clock may be tied high or low.
CMVFPC	Input	R20	**Common H-MVIP Frame Pulse Clock (CMVFPC).** The common 8.192 Mbit/s H-MVIP frame pulse clock provides the frame pulse clock for receive and transmit links configured for operation in 8.192 Mbit/s H-MVIP mode. CMVFPC is used to sample CMVFPB. CMVFPC is nominally a 50% duty cycle clock with a frequency of 4.096 MHz. The falling edge of CMVFPC must be aligned with the falling edge of CMV8MCLK with no more than ±10ns skew. The H-MVIP interfaces are enabled via the SYSOPT[1:0] bits in the Global Configuration register. If the TE-32 is not configured for H-MVIP operation, this clock may be tied high or low.
CMVFPB	Input	R22	**Common H-MVIP Frame Pulse (CMVFPB).** The active low common frame pulse for 8.192 Mbit/s H-MVIP signals references the beginning of each frame for links operating in 8.192 Mbit/s H-MVIP mode. If the CMMFP bit of the Master H-MVIP Interface Configuration register is a logic 1, the CMVFPB is becomes a multiframe pulse. The H-MVIP interfaces are enabled via the SYSOPT[1:0] bits in the Global Configuration register. If the TE-32 is not configured for H-MVIP operation, this frame pulse may be tied high or low. The CMVFPB frame pulse occurs at multiples of 125us and is sampled on the falling edge of CMVFPC.

Pin Name	Type	Pin No.	Function
MVID[1]/SDC1FP MVID[2]/SBIACT MVID[3]/SAJUST_REQ MVID[4]/SDDATA[0] MVID[5]/SDDATA[4] MVID[6]/SDDATA[5] MVID[7]/SDDATA[6] MVID[8]/SDDATA[7]	Output	B3 A3 A2 C5 A5 B6 C7 D6	**H-MVIP Ingress Data (MVID[1:8]).** MVID[x] carries the recovered T1 or E1 channels which have passed through the elastic store. Each MVID[x] signal carries the channels of four complete T1s or E1s. MVID[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVID[x] is updated on every second rising or falling edge of the common H-MVIP 16.384Mb /s clock, CMV8MCLK, as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master and H-MVIP Interface Configuration register. Each of MVID[1:4] and MVID[5:8] carries 16 independent T1s or E1s. MVID[1:8] share the same pins as SDC1FP, SBIACT, SAJUST_REQ, SDDATA[0] and SDDATA[4:7]. MVID[1:8] are selected when the SYSOPT[1:0] are set to “01” (H-MVIP), in the Global Configuration register.
CASID[1] CASID[2] CASID[3] CASID[4] CASID[5] CASID[6] CASID[7] CASID[8]	Output	B18 A19 A20 B19 D20 B22 C21 D21	**Channel Associated Signaling Ingress Data (CASID[1:8]).** Each CASID[x] signal carries CAS for four complete T1s or E1s. CASID[x] carries the corresponding CAS values of the channel carried in MVID[x]. It also carries the framer and alarm statuses. CASID[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASID[x] is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master H-MVIP Interface Configuration register. Each of CASID[1:4] and CASID[5:8] carries 16 independent T1s or E1s.
CCSID[1] CCSID[2] CCSID[3]	Output	C16 D18 B17	**Common Channel Signaling Ingress Data (CCSID[1:3]).** In T1 mode, CCSID[1] carries the 32 common channel signaling channels extracted from each of the 32 T1s. In E1 mode, CCSID[1:3] carries up to 3 timeslots (15,16, 31) from each of the 32 E1s. CCSID is formatted according to the H-MVIP standard. CCSID[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSID is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master H-MVIP Interface Configuration register.

Pin Name	Type	Pin No.	Function
TS0ID	Output	D17	**E1 Timeslot 0 Ingress Data (TS0ID)**. In E1 mode, TS0ID carries the first timeslot of each frame. TS0ID is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. TS0ID is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master H-MVIP Interface Configuration register.
MVED[1] MVED[2] MVED[3]/S77 MVED[4]/SAC1FP MVED[5]/SADATA[3] MVED[6]/SADATA[4] MVED[7]/SADATA[5] MVED[8]/SADATA[6]	Input	B10 A10 D10 B11 C12 D13 B13 C13	**H-MVIP Egress Data (MVED[1:8]).** The egress data streams to be transmitted are input on these pins. Each MVED[x] signal carries the channels of four complete T1s or E1s formatted according to the H-MVIP standard. MVED[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVED[x] is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register. Each of MVED[1:4] and MVED[5:8] carries 16 independent T1s or E1s. MVED[3:8] share the same pins as S77, SAC1FP, and SADATA[3:6] respectively. MVED[3:8] are selected when the SYSOPT[1:0] are set to “01” (H-MVIP), in the Global Configuration register. MVED[3] is a Schmitt triggered input.
CASED[1] CASED[2] CASED[3] CASED[4] CASED[5] CASED[6] CASED[7] CASED[8]	Input	H19 J20 J21 J22 K19 L20 L22 M22	**Channel Associated Signaling Egress Data (CASED[1:8]).** Each CASED[x] signal carries CAS for four complete T1s or E1s formatted according to the H-MVIP standard. CASED[x] carries the corresponding CAS values of the channel data carried in MVED[x]. CASED[x] may also present inband information for the control of signaling insertion. CASED[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASED[x] is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master H-MVIP Interface Configuration register. Each of CASED[1:4] and CASED[5:8] carries 16 independent T1s or E1s.

Pin Name	Type	Pin No.	Function
CCSED[1] CCSED[2] CCSED[3]	Input	H20 H21 H22	**Common Channel Signaling Egress Data (CCSED[1:3]).** In T1 mode CCSED[1] carries the common channel signaling channels to be transmitted in each of the T1s. In E1 mode CCSED carries up to 3 timeslots (15,16, 31) to be transmitted in each of the E1s. CCSED is formatted according to the H-MVIP standard. CCSED is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSED is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master H-MVIP Interface Configuration register.
SBI Line Side Interface			
LREFCLK	Input	Y4	**Line Reference Clock (LREFCLK).** This signal provides reference timing for the line side SBI bus interface. On the incoming byte interface of the line side SBI bus, LDC1FP, LDDATA[7:0], LDDP, LDPL, LDV5 and LAC1FPI are sampled of the rising edge or LREFCLK. In the outgoing byte interface, LADATA[7:0], LADP, LAPL, LAV5 and LAC1FPO are updated on the rising edge of LREFCLK. This clock is nominally a 19.44 MHz +/-50ppm clock with a 50% duty cycle. This clock must be phase locked to SREFCLK and can be externally connected to SREFCLK, when the S77 input is logic '0'.
LAC1FPI	Input	W10	**Line Add C1 Frame Pulse Input (LAC1FPI).** The Add bus timing signal identifies the frame and multiframe boundaries on the Add Data bus LADATA[7:0]. LAC1FPI is set high to mark the first C1 byte of the first transport envelope frame of the 4 frame multiframe on the LADATA[7:0] bus. LAC1FPI need not be presented on every occurrence of the multiframe. LAC1FPI is sampled on the rising edge of LREFCLK.
LAC1FPO	Output	AA11	**Line Add Bus C1 Frame Pulse Output (LAC1FPO).** The Add bus C1 frame pulse output identifies the frame boundaries on the Line Add Data bus LADATA[7:0]. LAC1FPO pulses high to mark the first C1 byte of the SBI multiframe. LAC1FPO will align to LAC1FPI if present, but fly-wheels in its absence. Multiple TE-32's cannot be connected to the same line side SBI bus interface. LAC1FPO is updated on the rising edge of LREFCLK.

Pin Name	Type	Pin No.	Function
LAPL	Output Tristate	AB11	**Line Add Bus Tributary Payload Active (LAPL).** The tributary payload active signal marks the bytes carrying the tributary payload. LAPL is high during each tributary payload byte on the LADATA[7:0] bus. This signal goes high during the V3 octet of a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 octet of a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI bus structure. Multiple TE-32's cannot be connected to the same line side SBI bus interface. LAPL is updated on the rising edge of LREFCLK.
LADATA[0] LADATA[1] LADATA[2] LADATA[3] LADATA[4] LADATA[5] LADATA[6] LADATA[7]	Output Tristate	W14 Y13 AA13 AB13 W13 AA12 W12 W11	**Line Add Bus Data (LADATA[7:0]).** The add bus data contains the line side SBI Add bus payload data in byte serial format. LADATA[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit to be transmitted). By default, LADATA[7:0] is only asserted during the tributaries assigned to this device as determined by the ENBL bit in the Line Side INSBI Tributary Control Indirect Access Data register. As options, LADATA[7:0] can be driven all the time or during the first nine columns. LADATA[7:0] is updated on the rising edge of LREFCLK.
LADP	Output Tristate	AB14	**Line Add Bus Data Parity (LADP).** The Add Bus data parity signal carries the parity of the outgoing signals. The parity calculation encompasses the LADATA[7:0] bus, the LAV5 signal and the LAPL signal. Odd parity is selected by setting the LAOP register bit to logic 1 and even parity is selected by setting the LAOP bit to logic 0. LADP is valid for all non-tristate cycles. LADP is updated on the rising edge of LREFCLK.
LAV5	Output Tristate	W15	**Line Add Bus V5 Byte (LAV5).** The outgoing tributary V5 byte signal marks the various tributary V5 bytes. LAV5 marks each tributary V5 byte on the LADATA[7:0] bus when high. By default, LAV5 is only asserted during the T1/E1 tributaries assigned to this device as determined by the ENBL bit in Line Side INSBI Tributary Control Indirect Access Data register. As options, LAV5 can be driven all the time or during the first nine columns. LAV5 is updated on the rising edge of LREFCLK.
LDDATA[0] LDDATA[1] LDDATA[2] LDDATA[3] LDDATA[4] LDDATA[5] LDDATA[6] LDDATA[7]	Input	W5 AA6 AB5 Y3 Y6 AA5 AB4 AB3	**Line Drop Bus Data (LDDATA[7:0]).** The drop bus data contains the T1/E1 receive payload data in byte serial format. LDDATA[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. LDDATA[7:0] is sampled on the rising edge of LREFCLK.

Pin Name	Type	Pin No.	Function
LDDP	Input	Y7	**Line Drop Bus Data Parity (LDDP).** The incoming data parity signal carries the parity of the incoming signals. The parity calculation encompasses the LDDATA[7:0] bus, the LDV5 signal and the LDPL signal. Odd parity is selected by setting the SBI_PAR_CTL bit in the Line Side EXSBI Control Register high and even parity is selected by setting the SBI_PAR_CTL bit low. LDDP is sampled on the rising edge of LREFCLK.
LDC1FP	Input	AB6	**Line Drop C1 Frame Pulse (LDC1FP).** The LDC1FP provides frame synchronization for devices connected via an SBI interface. LDC1FP is asserted, for one LREFCLK cycle, for the first C1 byte of the SBI multiframe on the LDDATA[7:0] bus. This signal occurs every 500µS (i.e. every 9720 LREFCLK cycles). LDC1FP is sampled on the rising edge of LREFCLK.
LDV5	Input	W6	**Line Drop Bus V5 Byte (LDV5).** The incoming tributary V5 byte signal marks the various tributary V5 bytes. LDV5 marks each tributary V5 byte on the LDDATA[7:0] bus when high. LDV5 is sampled on the rising edge of LREFCLK.
LDPL	Input	Y8	**Line Drop Bus Payload Active (LDPL).** The payload active signal indicates valid data within the line side SBI structure. This signal must be high during all octets making up a tributary. This signal goes high during the V3 octet of a tributary to indicate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 octet of a tributary to indicate positive timing adjustments between the tributary rate and the fixed SBI bus structure. The TE-32 only monitors the drop bus payload active signal during the tributary timeslots assigned to this device. LDPL is sampled on the rising edge of LREFCLK.
SBI System Side Interface			
CTCLK	Input	F19	**Common Transmit Clock (CTCLK).** This input signal is used as a reference transmit tributary clock which can be used in egress Clock Master modes. CTCLK must be multiple of 8 kHz. The transmit clock is derived by the jitter attenuator PLL using CTCLK as a reference. The TE-32 may be configured to ignore the CTCLK input and lock to the data. The receive tributary clock is automatically substituted for CTCLK if line loopback or looptiming is enabled.
S77/MVED[3]	Input	D10	**System Side SBI 77.76 MHz Select (S77).** This input determines the frequency of SREFCLK. If S77 is low, SREFCLK is expected to be 19.44MHz. If S77 is high, SREFCLK is expected to be 77.76 MHz and data is driven and sampled every fourth cycle. S77 is expected to be held static. S77 shares the same pin as MVED[3]. S77 is selected when the SYSOPT[1:0] bits are set to “10” or “11”, in the Global Configuration register. S77 is a Schmitt triggered input.

Pin Name	Type	Pin No.	Function
SREFCLK	Input	C10	**System Reference Clock (SREFCLK).** This system reference clock is a nominal 19.44 MHz +/-50ppm or 77.76 MHz +/-50ppm 50% duty cycle clock. This clock is common to both the add and drop sides of the SBI bus. SREFCLK must be active for all applications. When the SYSOPT[1:0] register bits are binary "01" (H-MVIP interface), SREFCLK is required to be 19.44 MHz. This clock must be phase locked to LREFCLK and can be external connected to LREFCLK, when the S77 input is logic '0'.
SDC1FP/MVID[1]	I/O	B3	**SBI Drop C1 Frame Pulse (SDC1FP).** The SDC1FP C1 frame pulse synchronizes devices interfacing to the Insert SBI bus. The frame pulse indicates SBI bus multiframe alignment which occurs every 500 μS, therefore this signal is pulsed every 9720 SREFCLK cycles (38880 cycles if S77 is high). This signal does not need to occur every SBI multiframe and is also used to indicate T1 and E1 multiframe alignment in synchronous SBI mode by pulsing at multiples of every 12 SBI multiframes (48 T1/E1 frames). In synchronous locked mode, as selected by the SYNCSBI context bit programmed through the RX-SBI-ELST Indirect Channel Data register, SDC1FP pulses every 116640 SREFCLK cycles (466560 cycles if S77 is high). If the SYNCSBI bit is logic 1 for at least one tributary, SDC1FP must indicate T1 and E1 multiframe alignment. The TE-32 can be configured to generate this frame pulse. Only one device on the SBI bus should generate this signal. By default this signal is not enabled to generate the frame pulse. If a SDC1FP pulse is received at an unexpected cycle, the Drop bus with become high-impedance until two consecutive valid SDC1FP pulses occur. The system frame pulse is a single SREFCLK cycle long and is updated on the rising edge of SREFCLK. This signal must be held low if the SBI bus is not being used. SDC1FP shares the same pin as MVID[1]. SDC1FP is selected when the SYSOPT[1:0] bits are set to "10" or "11", in the Global Configuration register.
SAC1FP/MVED[4]	Input	B11	**SBI Add C1 Frame Pulse (SAC1FP).** The Extract C1 frame pulse synchronizes devices interfacing to the Extract SBI bus. The frame pulse indicates SBI bus multiframe alignment which occurs every 500 μS, therefore this signal is pulsed every 9720 SREFCLK cycles (38880 cycles if S77 is high). This signal does not need to occur every SBI multiframe. SAC1FP is sampled on the rising edge of SREFCLK. This signal must be held low if the SBI bus is not being used. SAC1FP shares the same pin as MVED[4]. SAC1FP is selected when the SYSOPT[1:0] bits are set to "10" or "11", in the Global Configuration register.

Pin Name	Type	Pin No.	Function
SADATA[0] SADATA[1] SADATA[2] SADATA[3]/MVED[5] SADATA[4]/MVED[6] SADATA[5]/MVED[7] SADATA[6]/MVED[8] SADATA[7]	Input	A11 D12 B12 C12 D13 B13 C13 D14	**System Add Bus Data (SADATA[7:0]).** The System add data bus is a time division multiplexed bus which carries the E1, T1 and DS3 tributary data is byte serial format over the SBI bus structure. This device only monitors the add data bus during the timeslots assigned to this device. SADATA[7:0] is sampled on the rising edge of SREFCLK. SADATA[3:6] share the same pins as MVED[5:8]. SADATA[3:6] is selected when the SYSOPT[1:0] bits are set to “10” or “11”, in the Global Configuration register.
SADP	Input	A14	**System Add Bus Data Parity (SADP).** The system add bus signal carries the even or odd parity for the add bus signals SADATA[7:0], SAPL and SAV5. The TE-32 monitors the add bus parity cycles when S77 is low and during the entire selected STM-1 when S77 is high. SADP is sampled on the rising edge of SREFCLK.
SAPL	Input	B14	**System Add Bus Payload Active (SAPL).** The add bus payload active signal indicates valid data within the SBI bus structure. This signal must be high during all octets making up a tributary. This signal goes high during the V3 octet of a tributary to indicate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 octet of a tributary to indicate positive timing adjustments between the tributary rate and the fixed SBI bus structure. The TE-32 only monitors the add bus payload active signal during the tributary timeslots assigned to this device. SAPL is sampled on the rising edge of SREFCLK.
SAV5	Input	C14	**System Add Bus Payload Indicator (SAV5).** The add bus payload indicator locates the position of the floating payloads for each tributary within the SBI bus structure. Timing differences between the tributary timing and the synchronous SBI bus are indicated by adjustments of this payload indicator relative to the fixed SBI bus structure. All timing adjustments indicated by this signal must be accompanied by appropriate adjustments in the SAPL signal. The TE-32 only monitors the add bus payload indicator signal during the tributary timeslots assigned to this device. SAV5 is sampled on the rising edge of SREFCLK.

Pin Name	Type	Pin No.	Function
SAJUST_REQ/ MVID[3]	Output Tristate	A2	**System Add Bus Justification Request (SAJUST_REQ).** The justification request signals the Link Layer device to speed up, slow down or maintain the rate which it is sending data to the TE-32. This is only used when the TE-32 is the timing master for the tributary transmit direction. This active high signal indicates negative timing adjustments when asserted high during the V3 octet of the tributary. In response to this the Link Layer device sends an extra byte in the V3 octet of the next SBI bus multi-frame. Positive timing adjustments are requested by asserting justification request high during the octet following the V3 octet. The Link Layer device responds to this request by not sending an octet during the V3 octet of the next multi-frame. SAJUST_REQ has a different significance in the flexible bandwidth mode. In this mode, SAJUST_REQ is high for one SREFCLK cycle for each byte that can be accepted. A valid byte on SADATA[7:0] with an accompanying SAPL assertion is expected in response. The TE-32 only drives the justification request signal during the tributary timeslots assigned to this device. When operating in 19.44 MHz mode (i.e. S77 low), SAJUST_REQ is aligned by the SAC1FP input. When operating in 77.76 MHz mode (i.e. S77 high), SAJUST_REQ's alignment is relative to the SDC1FP signal. SAJUST_REQ is updated on the rising edge of SREFCLK. SAJUST_REQ shares the same pin as MVID[3]. SAJUST_REQ is selected when the SYSOPT[1:0] bits are set to "10" or "11", in the Global Configuration register.
SDDATA[0]/MVID[4] SDDATA[1] SDDATA[2] SDDATA[3] SDDATA[4]/MVID[5] SDDATA[5]/MVID[6] SDDATA[6]/MVID[7] SDDATA[7]/MVID[8]	Output Tristate	C5 A4 B5 C6 A5 B6 C7 D6	**System Drop Bus Data (SDDATA[7:0]).** The System drop data bus is a time division multiplexed bus which carries the E1 and T1 tributary data is byte serial format over the SBI bus structure. This device only drives the data bus during the timeslots assigned to this device. SDDATA[7:0] is updated on the rising edge of SREFCLK. SDDATA[0] and SDDATA[4:7] share the same pins as MVID[4] and MVID[5:8]. SDDATA[0] and SDDATA[4:7] are selected when the SYSOPT[1:0] bits are set to "10" or "11", in the Global Configuration register.
SDDP	Output Tristate	A6	**System Drop Bus Data Parity (SDDP).** The system drop bus signal carries the even or odd parity for the drop bus signals SDDATA[7:0], SDPL and SDV5. Whenever the TE-32 drives the data bus, the parity is valid. SDDP is updated on the rising edge of SREFCLK.

Pin Name	Type	Pin No.	Function
SDPL	Output Tristate	A7	**System Drop Bus Payload Active (SDPL).** The payload active signal indicates valid data within the SBI bus structure. This signal is asserted during all octets making up a tributary. This signal goes high during the V3 octet of a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 octet of a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI bus structure. In the flexible bandwidth configuration, SDPL is asserted for each byte as it becomes available. Therefore, SDPL may be high or low arbitrarily during any SREFCLK cycle. The TE-32 only drives the payload active signal during the tributary timeslots assigned to this device. SDPL is updated on the rising edge of SREFCLK.
SDV5	Output Tristate	C8	**System Drop Bus Payload Indicator (SDV5).** The payload indicator locates the position of the floating payloads for each tributary within the SBI bus structure. Timing differences between the tributary timing and the synchronous SBI bus are indicated by adjustments of this payload indicator relative to the fixed SBI bus structure. All timing adjustments indicated by this signal are accompanied by appropriate adjustments in the SDPL signal. The TE-32 only drives the payload Indicator signal during the tributary timeslots assigned to this device. SDV5 is updated on the rising edge of SREFCLK.
SBIACT/MVID[2]	Output	A3	**SBI Output Active (SBIACT).** The SBI Output Active indicator is high whenever the TE-32 is driving the SBI drop bus signals. This signal is used by other TE-32s or other SBI devices to detect SBI configuration problems by detecting other devices driving the SBI bus during the same tributary as the device listening to this signal. This output is updated on the rising edge or SREFCLK. SBIACT shares the same pin as MVID[2]. SBIACT is selected when the SYSOPT[1:0] bits are set to “10” or “11”, in the Global Configuration register.
SBIDET[0] SBIDET[1]	Input	A15 B15	**SBI Bus Activity Detection (SBIDET[1:0]).** The SBI bus activity detect input detects tributary collisions between devices sharing the same SBI bus. Each SBI device driving the bus also drives an SBI active signal (SBIACT). This pair of activity detection inputs monitors the active signals from two other SBI devices. When unused this signal should be connected to ground. These inputs only have effect when the SBI bus is configured for 19.44 MHz (i.e. S77 is low). A collision is detected when either of SBIDET[1:0] signals are active concurrently with this device driving SBIACT. When collisions occur the SBI drivers are disabled and an interrupt is generated to signal the collision.

Pin Name	Type	Pin No.	Function
Microprocessor Interface			
INTB	Output OD	T21	**Active Low Open-Drain Interrupt (INTB).** This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
CSB	Input	AA15	**Active Low Chip Select (CSB).** This signal is low during TE-32 register accesses. The CSB input has an integral pull up resistor.
RDB	Input	W17	**Active Low Read Enable (RDB).** This signal is low during TE-32 register read accesses. The TE-32 drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	AB16	**Active Low Write Strobe (WRB).** This signal is low during a TE-32 register write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	U22 T20 V19 U21 U20 W22 Y22 Y21	**Bidirectional Data Bus (D[7:0]).** This bus provides TE-32 register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10] A[11] A[12]	Input	AB22 AA21 Y19 AA20 AA19 AB20 AA18 W19 AB18 AA17 W18 Y16 AA16	**Address Bus (A[12:0]).** This bus selects specific registers during TE-32 register accesses. A[12] has an internal pull down resistor. Tie A[12] directly to ground unless access to bit HIZIO in the Master Test Register (0x1000) is required.
RSTB	Input	W20	**Active Low Reset (RSTB).** This signal provides an asynchronous TE-32 reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	AA22	**Address Latch Enable (ALE).** This signal is active high and latches the address bus A[12:0] when low. When ALE is high, the internal address latches are transparent. It allows the TE-32 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
JTAG Interface			
TCK	Input	B1	**Test Clock (TCK).** This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	D2	**Test Mode Select (TMS).** This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	E3	**Test Data Input (TDI).** This signal carries test data into the TE-32 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Output	D1	**Test Data Output (TDO).** This signal carries test data out of the TE-32 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	C1	**Active low Test Reset (TRSTB).** This signal provides an asynchronous TE-32 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB must be connected to the RSTB input.
Power and Ground Pins			
VDD3.3[19] VDD3.3[18] VDD3.3[17] VDD3.3[16] VDD3.3[15] VDD3.3[14] VDD3.3[13] VDD3.3[12] VDD3.3[11] VDD3.3[10] VDD3.3[9] VDD3.3[8] VDD3.3[7] VDD3.3[6] VDD3.3[5] VDD3.3[4] VDD3.3[3] VDD3.3[2] VDD3.3[1]	Power	A18 A22 AB17 D11 D16 D4 E1 F20 L1 L19 R21 R4 V2 W16 W4 W8 Y18 Y20 Y5	**Power (VDD3.3[19:1]).** The VDD3.3[19:1] pins should be connected to a well decoupled +3.3V DC power supply.

Pin Name	Type	Pin No.	Function
VDD1.8[19] VDD1.8[18] VDD1.8[17] VDD1.8[16] VDD1.8[15] VDD1.8[14] VDD1.8[13] VDD1.8[12] VDD1.8[11] VDD1.8[10] VDD1.8[9] VDD1.8[8] VDD1.8[7] VDD1.8[6] VDD1.8[5] VDD1.8[4] VDD1.8[3] VDD1.8[2] VDD1.8[1]	Power	C2 D3 J2 R1 U3 AB2 AB9 Y12 Y15 AB19 N4 V20 U19 N21 K21 C22 C18 A13 B7	**Power (VDD1.8[19:1]).** The VDD1.8[19:1] pins should be connected to a well-decoupled +1.8V DC power supply.
VSS[116] VSS[115] VSS[114] VSS[113] VSS[112] VSS[111] VSS[110] VSS[109] VSS[108] VSS[107] VSS[106] VSS[105] VSS[104] VSS[103] VSS[102] VSS[101] VSS[100] VSS[99] VSS[98] VSS[97] VSS[96] VSS[95] VSS[94] VSS[93] VSS[92] VSS[91] VSS[90] VSS[89] VSS[88] VSS[87] VSS[86] VSS[85] VSS[84] VSS[83] VSS[82] VSS[81] VSS[80]	Ground	E2 F3 J19 M21 K20 K22 M20 N19 N22 N20 P19 P22 P21 P20 R19 P1 T1 Y1 P2 U1 V3 P3 T3 W2 T4 V4 Y2 G2 J3 L2 G1 J1 M1 A16 C15 B16 A17	**Ground (VSS[116:1]).** The VSS[116:1] pins should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS[79]		AB7	
VSS[78]		AA8	
VSS[77]		W7	
VSS[76]		Y9	
VSS[75]		AA9	
VSS[74]		W9	
VSS[73]		Y10	
VSS[72]		AA10	
VSS[71]		AB10	
VSS[70]		AA4	
VSS[69]		C4	
VSS[68]		A12	
VSS[67]		AA2	
VSS[66]		AA3	
VSS[65]		AA7	
VSS[64]		AB12	
VSS[63]		AB15	
VSS[62]		AB21	
VSS[61]		AB8	
VSS[60]		B4	
VSS[59]		C11	
VSS[58]		C17	
VSS[57]		C19	
VSS[56]		C3	
VSS[55]		D15	
VSS[54]		D19	
VSS[53]		D22	
VSS[52]		D5	
VSS[51]		D8	
VSS[50]		F1	
VSS[49]		G19	
VSS[48]		G4	
VSS[47]		J10	
VSS[46]		J11	
VSS[45]		J12	
VSS[44]		J13	
VSS[43]		J14	
VSS[42]		J9	
VSS[41]		K10	
VSS[40]		K11	
VSS[39]		K12	
VSS[38]		K13	
VSS[37]		K14	
VSS[36]		K3	
VSS[35]		K9	
VSS[34]		L10	
VSS[33]		L11	
VSS[32]		L12	
VSS[31]		L13	
VSS[30]		L14	
VSS[29]		L21	
VSS[28]		L9	
VSS[27]		M10	
VSS[26]		M11	
VSS[25]		M12	
VSS[24]		M13	

Pin Name	Type	Pin No.	Function
VSS[23] VSS[22] VSS[21] VSS[20] VSS[19] VSS[18] VSS[17] VSS[16] VSS[15] VSS[14] VSS[13] VSS[12] VSS[11] VSS[10] VSS[9] VSS[8] VSS[7] VSS[6] VSS[5] VSS[4] VSS[3] VSS[2] VSS[1]		M14 M19 M4 M9 N10 N11 N12 N13 N14 N9 P10 P11 P12 P13 P14 P9 T2 V21 V22 W21 Y11 Y14 Y17	
Unused or Unconnected			
Unused		B20 A21 B21 E20 E21 C20 E22 F21 E19 G20 F22 G21 G22 R3 V1 W3 R2 U2 AA1 U4 W1 AB1 H4 L3 N3 H2 K4 N2 H1 K2 M2 H3	These balls must be left floating.

Pin Name	Type	Pin No.	Function
		K1 N1 F4 J4 M3 B8 A8 D7 F2 E4 G3 C9 B9 A9 D9 AA14	
Unconnected		A1 B2 L4 P4 T19	These balls have no internal connections. They may be left floating or tied to a static logic level.

Notes on Pin Descriptions:

1. All TE-32 inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels.
2. All TE-32 outputs and bi-directionals have at least 2 mA drive capability. The bi-directional data bus outputs, D[7:0], have 4 mA drive capability. The outputs CASID[1:8], CCSID[1:3], TS0ID, TDO and INTB have 4 mA drive capability. The outputs MVID[2]/SBIACT, MVID[3]/SAJUST_REQ, MVID[4]/SDDATA[0], MVID[5:8]/SDDATA[4:7], SDDP, SDPL, SDV5, LAV5, LAC1FPO, LADATA[7:0], LADP and LAPL have 8mA drive capability. The bi-directional signal SDC1FP/MVID[1] has 8mA drive capability.
3. Inputs CSB, RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
4. Input A[12] has an internal pull-down resistor.
5. All unused inputs should be connected to GROUND.
6. Power to the VDD3.3 pins should be applied *before* power to the VDD1.8 pins is applied. Similarly, power to the VDD1.8 pins should be removed *before* power to the VDD3.3 pins is removed.

9 Functional Description

The TE-32 supports a total throughput of 65.536Mbit/s (including overhead) in both transmit (a.k.a. egress) and receive (a.k.a. ingress) directions.

9.1 T1 Framing

T1 framing can be performed on up to 32 tributaries.

The T1 framing function searches for the framing bit pattern in the standard Superframe (SF), SLC®96 or Extended Superframe (ESF) framing formats. When searching for frame each of the 193 (SF or SLC®96) or each of the 772 (ESF) framing bit candidates is simultaneously examined.

The time required to acquire frame alignment to an error-free ingress stream, containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0), is dependent upon the framing format. For SF format, the T1 framer will determine frame alignment within 4.4ms 99 times out of 100. For SLC®96 format, the T1 framer will determine frame alignment within 13ms. For ESF format, the T1 framer will determine frame alignment within 15 ms 99 times out of 100.

Once the T1 framer has found frame, the ingress data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or a CRC-6 error in ESF), and severely errored framing events. The performance data is accumulated for each tributary. The T1 framer also detects out-of-frame, based on a selectable ratio of framing bit errors. For ESF, out-of-frame declaration is based strictly on Frame Alignment Signal (F1-F6) bit errors; a new frame search is never initiated upon excessive CRC-6 errors.

The framing function can also be disabled to allow reception of unframed data.

9.1.1 Inband Code Detection

The framer detects the presence of either of two programmable inband loopback activate and deactivate code sequences in either framed or unframed data streams (whether data stream is framed or unframed is not programmable). The loopback codes will be detected in the presence of a mean bit error rate of up to 10^{-2}. When the inband code is framed, the framing bits overwrite the code bits, thus appearing to the receiver as a 2.6×10^{-3} BER (which is within the tolerable BER of 10-2).

Code indication is provided on the active high loopback activate (LBA) and loopback deactivate (LBD) status bits. Changes in these status bits result in the setting of corresponding interrupt status bits, LBAI and LBDI respectively, and can also be configured to result in the setting of a maskable interrupt indication.

The inband loopback activate condition consists of a repetition of the programmed activate code sequence in all bit positions for a minimum of 5.08 seconds (± 40 ms). The inband loopback deactivate condition consists of a repetition of the programmed deactivate code sequence in all bit positions for a minimum of 5.08 seconds (± 40 ms). Programmed codes can be from three to eight bits in length.

The code sequence detection and timing is compatible with the specifications defined in T1.403, TR-TSY-000312, and TR-TSY-000303.

9.1.2 T1 Bit Oriented Code Detection

The presence of 63 of the possible 64 bit oriented codes transmitted in the T1 Facility Data Link channel in ESF framing format is detected, as defined in ANSI T1.403 and in TR-TSY-000194. The 64^{th} code (111111) is similar to the HDLC flag sequence and is used to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0). The receiver declares a received code valid if it has been observed for two consecutive times. The code is declared removed if two code sequences containing code values different from the detected code are received two consecutive times.

Valid BOC are indicated through the BOCI status bit. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a detected code has been validated, or when a valid code goes away (i.e. the BOC bits go to all ones).

9.1.3 T1 Alarm Integration

The presence of Yellow, Red, and AIS Carrier Fail Alarms (CFA) in SF, SLC®96 or ESF formats is detected and integrated in accordance with the specifications defined in ANSI T1.403 and TR-TSY-000191.

The presence of Yellow alarm is declared when the Yellow pattern has been received for 400 ms (± 50 ms); the Yellow alarm is removed when the Yellow pattern has been absent for 400 ms (± 50 ms). The presence of Red alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the Red alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms). The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream have been present for 2.55 sec (±40 ms); the AIS alarm is removed when the AIS condition has been absent for 16.6 sec (±500 ms).

CFA alarm detection algorithms operate in the presence of a 10^{-3} bit error rate.

Customer Interface Alarms

The RAI-CI and AIS-CI alarms defined in T1.403 are detected reliably.

By definition, RAI-CI is a repetitive pattern within the ESF data link with a period of 1.08 seconds. It consists of sequentially interleaving 0.99 seconds of 00000000 11111111 (right-to-left) with 90 ms of 00111110 11111111.

RAI-CI is declared when a bit oriented code of "00111110 11111111" is validated (i.e. two consecutive patterns) while RAI (a.k.a. Yellow alarm) is declared. RAI-CI is cleared upon deassertion of RAI or upon 28 consecutive 40ms intervals without validation of "00111110 11111111".

By definition, AIS-CI is a repetitive pattern of 1.26 seconds. It consists of 1.11 seconds of an unframed all ones pattern and 0.15 seconds of all ones modified by the AIS-CI signature. The AIS-CI signature is a repetitive pattern 6176 bits in length in which, if the first bit is numbered bit 0, bits 3088, 3474 and 5790 are logical zeros and all other bits in the pattern are logical ones. AIS-CI is an unframed pattern, so it is defined for all framing formats.

AIS-CI is declared between 1.40 and 2.56 seconds after initiation of the AIS-CI signal and is deasserted 16.6 seconds after it ceases.

9.2 E1 Framing

E1 framing can be performed on up to 32 tributaries.

The E1 framing function searches for basic frame alignment, CRC multiframe alignment, and channel associated signaling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once basic (or FAS) frame alignment has been found, the incoming PCM data stream is continuously monitored for FAS/NFAS framing bit errors, which are accumulated in a framing bit error counter dedicated to each tributary. Once CRC multiframe alignment has been found, the PCM data stream is continuously monitored for CRC multiframe alignment pattern errors and CRC-4 errors, which are accumulated in a CRC error counter dedicated to each tributary. Once CAS multiframe alignment has been found, the PCM data is continuously monitored for CAS multiframe alignment pattern errors. The E1 framer also detects and indicates loss of basic frame, loss of CRC multiframe, and loss of CAS multiframe, based on user-selectable criteria. The reframe operation can be initiated by software, by excessive CRC errors, or when CRC multiframe alignment is not found within 400 ms.

The E1 framer extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe). Moreover, the framer also extracts submultiframe-aligned 4-bit codewords from each of the National bit positions Sa4 to Sa8, and stores them in microprocessor-accessible registers that are updated every CRC submultiframe.

The E1 framer identifies the raw bit values for the Remote (or distant frame) Alarm (bit 3 in timeslot 0 of NFAS frames) and the Remote Signaling Multiframe (or distant multiframe) Alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe). Access is also provided to the "debounced" remote alarm and remote signaling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 4 (provided the RAIC bit is logic 1) and 3 consecutive occurrences, respectively, as per Recommendation O.162. Detection of AIS and timeslot 16 AIS are provided. AIS is also integrated, and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a Red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (INF, INSMF, INCMF, AIS or RED), and to signal when any event (RAI, RMAI, AISD, TS16AISD, COFA, FER, SMFER, CMFER, CRCE or FEBE) has occurred. Additionally, interrupts may be generated every frame, CRC submultiframe, CRC multiframe or signaling multiframe.

9.2.1 Basic Frame Alignment Procedure

The E1 framer searches for basic frame alignment using the algorithm defined in ITU-T Recommendation G.706 sections 4.1.2 and 4.2.

The algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS ('0011011');

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed non-frame alignment sequence (NFAS) TS 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed TS 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the second 7-bit FAS sequence check. This "hold-off" is done to ensure that new frame alignment searches are done in the next bit position, modulo 512. This facilitates the discovery of the correct frame alignment, even in the presence of fixed timeslot data imitating the FAS.

The algorithm provides robust framing operation even in the presence of random bit errors; the algorithm provides a 99.98% probability of finding frame alignment within 1 ms in the presence of 10^{-3} bit error rate and no mimic patterns.

Once frame alignment is found, the INF context bit is set to logic 1, a change of frame alignment is indicated (if it occurred), and the frame alignment signal is monitored for errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and the debounced value of the Remote Alarm bit (bit 3 of NFAS frames) is reported. Loss of frame alignment is declared if 3 consecutive FASs have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The E1 framer can be forced to initiate a basic frame search at any time when any of the following conditions are met:

- the software re-frame bit, REFR, in the T1/E1 Framer Indirect Channel Data registers is set to logic 1;
- the CRC Frame Find Block is unable to find CRC multiframe alignment; or
- the CRC Frame Find Block accumulates excessive CRC evaluation errors (≥ 915 CRC errors in 1 second) and is enabled to force a re-frame under that condition.

9.2.2 CRC Multiframe Alignment Procedure

The E1 framer searches for CRC multiframe alignment by observing whether the International bits (bit 1 of TS 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms

Once CRC multiframe alignment is found, the INCMF register bit is set to logic 1, and the E1 framer monitors the multiframe alignment signal (MFAS), indicating errors occurring in the 6-bit MFAS pattern, errors occurring in the received CRC and the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe). The E1 framer declares loss of CRC multiframe alignment if basic frame alignment is lost. However, once CRC multiframe alignment is found, it cannot be lost due to errors in the 6-bit MFAS pattern.

Under the CRC-to-non-CRC interworking algorithm, if the E1 framer can achieve basic frame alignment with respect to the incoming PCM data stream, but is unable to achieve CRC-4 multiframe alignment within the subsequent 400 ms, the distant end is assumed to be a non CRC-4 interface. The details of this algorithm are illustrated in the state diagram in Figure 6.

Figure 6 CRC Multiframe Alignment Algorithm

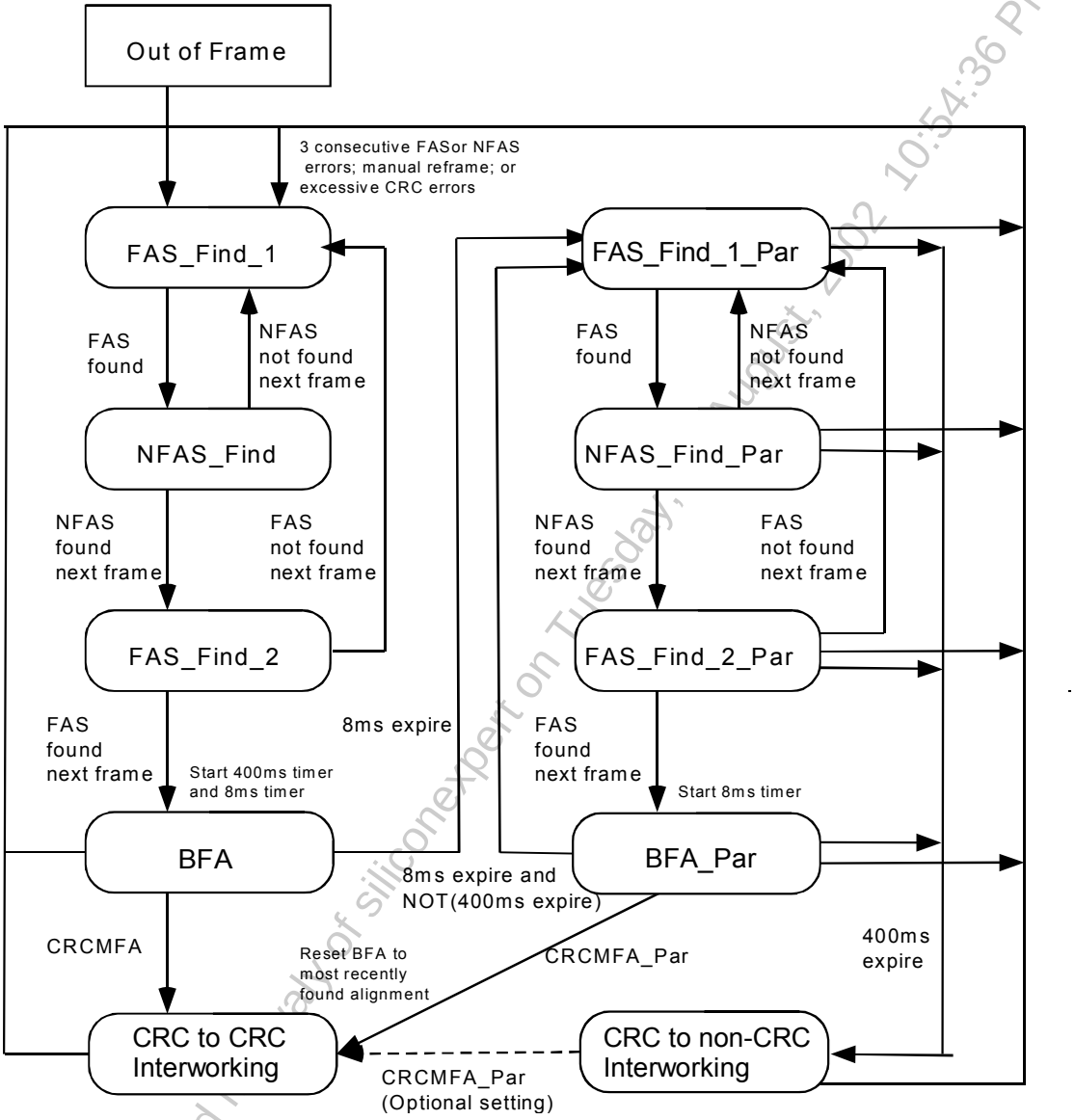


Table 1 E1 Framer Framing States

State	Out of Frame	Out of Offline Frame
FAS_Find_1	Yes	No
NFAS_Find	Yes	No
FAS_Find_2	Yes	No
BFA	No	No
CRC to CRC Interworking	No	No
FAS_Find_1_Par	No	Yes
NFAS_Find_Par	No	Yes
FAS_Find_2_Par	No	Yes
BFA_Par	No	No
CRC to non-CRC Interworking	No	No

The states of the primary basic framer and the parallel/offline framer in the E1 framer block at each stage of the CRC multiframe alignment algorithm are shown in Table 1.

From an out of frame state, the E1 framer attempts to find basic frame alignment in accordance with the FAS/NFAS/FAS G.706 Basic Frame Alignment procedure outlined above. Upon achieving basic frame alignment, a 400 ms timer is started, as well as an 8 ms timer. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared.

If the 8 ms timer expires without achieving multiframe alignment, a new offline search for basic frame alignment is initiated. This search is performed in accordance with the Basic Frame Alignment procedure outlined above. However, this search does not immediately change the actual basic frame alignment of the system (i.e., PCM data continues to be processed in accordance with the first basic frame alignment found after an out of frame state while this frame alignment search occurs as a parallel operation).

When a new basic frame alignment is found by this offline search, the 8 ms timer is restarted. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared and the basic frame alignment is set accordingly (i.e., the basic frame alignment is set to correspond to the frame alignment found by the parallel offline search, which is also the basic frame alignment corresponding to the newly found CRC multiframe alignment).

Subsequent expirations of the 8 ms timer will likewise reinitiate a new search for basic frame alignment. If, however, the 400 ms timer expires at any time during this procedure, the E1 framer stops searching for CRC multiframe alignment and declares CRC-to-non-CRC interworking. In this mode, the E1 framer may be optionally set to either halt searching for CRC multiframe altogether, or may continue searching for CRC multiframe alignment using the established basic frame alignment. In either case, no further adjustments are made to the basic frame alignment, and no offline searches for basic frame alignment occur once CRC-to-non-CRC interworking is declared: it is assumed that the established basic frame alignment at this point is correct.

9.2.3 AIS Detection

When an unframed all-ones receive data stream is received, an AIS defect is indicated by setting the AISD context bit to logic 1 when fewer than three zero bits are received in 512 consecutive bits or, optionally, in each of two consecutive periods of 512 bits. The AISD bit is reset to logic 0 when three or more zeros in 512 consecutive bits or in each of two consecutive periods of 512 bits. Finding frame alignment will also cause the AISD bit to be set to logic 0.

9.2.4 Signaling Frame Alignment

Once the basic frame alignment has been found, the E1 framer searches for Channel Associated Signaling (CAS) multiframe alignment using the following G.732 compliant algorithm: signaling multiframe alignment is declared when at least one non-zero time slot 16 bit is observed to precede a time slot 16 containing the correct CAS alignment pattern, namely four zeros (“0000”) in the first four bit positions of timeslot 16.

Once signaling multiframe alignment has been found, the E1 framer sets the INSMF context bit of the tributary to logic 1, and monitors the signaling multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the Remote Signaling Multiframe Alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe).

This E1 framer also indicates the reception of TS 16 AIS when time slot 16 has been received with three or fewer zeros in each of two consecutive multiframe periods. The TS16AIS status is cleared when each of two consecutive signaling multiframe periods contain four or more zeros OR when the signaling multiframe signal is found.

The block declares loss of CAS multiframe alignment if two consecutive CAS multiframe alignment signals have been received in error, or additionally, if all the bits in time slot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes. Loss of CAS multiframe alignment is also declared if basic frame alignment has been lost.

9.2.5 National Bit Extraction

The E1 framer extracts and assembles the submultiframe-aligned National bit codewords Sa4[1:4] , Sa5[1:4] , Sa6[1:4] , Sa7[1:4] and Sa8[1:4]. The corresponding register values are updated upon generation of the CRC submultiframe interrupt.

This E1 framer also detects the V5.2 link ID signal, which is detected when 2 out of 3 Sa7 bits are zeros. Upon reception of this Link ID signal, the V52LINKV context bit is set to logic 1. This bit is cleared to logic 0 when 2 out of 3 Sa7 bits are ones.

9.2.6 E1 Alarm Integration

The OOF and the AIS defects are integrated, verifying that each condition has persisted for 104 ms (± 6 ms) before indicating the alarm condition. The alarm is removed when the condition has been absent for 104 ms (± 6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD (AIS detection). The E1 framer counts the occurrences of AISD over a 4 ms interval and indicates a valid AIS is present when 13 or more AISD indications (of a possible 16) have been received. Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated. An interval with no valid AIS presence indication decrements the interval counter. The AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.8% probability of declaring an AIS Alarm within 104 ms in the presence of a 10^{-3} mean bit error rate.

The Red alarm algorithm monitors occurrences of out of frame (OOF) over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval. Each interval with a valid OOF indication increments an interval counter which declares Red Alarm when 25 valid intervals have been accumulated. An interval with valid INF indication decrements the interval counter; the Red Alarm declaration is removed when the counter reaches 0. This algorithm biases OOF occurrences, leading to declaration of Red alarm when intermittent loss of frame alignment occurs.

The E1 framer can also be disabled to allow reception of unframed data.

9.3 T1/E1 Performance Monitoring

CRC error events, Frame Synchronization bit error events, and Out Of Frame events, or optionally, Change of Frame Alignment (COFA) events are accumulated with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the counter values are transferred into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, the OVR context bit is asserted to indicate data loss.

A bit error event (BEE) is defined as an F-bit error for SF and SLC®96 framing format or a CRC-6 error for ESF framing format. A framing bit error (FER) is defined as an F_s or F_t error for SF and SLC®96 and an F_e error for ESF framing format.

The transfer clock within the TE-32 chip is generated precisely once per second (i.e. 19440000 SREFCLK cycles) if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1 or by writing to the Global PMON Update register with the FRMR bit set. Coincident with the counter transfer, a Performance Report Message (PRM) is transmitted for each T1 tributary for which the PRMEN context bit is logic 1.

9.4 T1/E1 HDLC Receiver

The HDLC Receiver is a microprocessor peripheral used to receive HDLC frames on the 4 kHz ESF facility data link or the E1 Sa-bit data link. A data link can also be extracted from any sub-set of bits within a single DS0.

The HDLC Receiver detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 127-byte FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The RHDL Indirect Channel Data Registers contain bits that indicate the overrun or empty FIFO status, the interrupt status, and the occurrence end of message bytes written into the FIFO. The RHDL Indirect Channel Data Registers also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the RHDL Indirect Channel Data Registers indicates the FCS status and if the packet contained a non-integer number of bytes.

9.5 T1/E1 Elastic Store (ELST)

Frame slip buffers exist in both the ingress and egress directions.

In the ingress direction, the Elastic Store (ELST) synchronizes ingress frames to the common ingress H-MVIP clock and frame pulse (CMV8MCLK, CMVFPB, CMVFPC) in H-MVIP modes. When using the SBI bus, the elastic store is required in locked or slave mode.

In the egress direction, the Elastic Store is required in H-MVIP mode or in SBI slave or locked modes when the transmit data is loop timed.

The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer. When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane/transmit clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The subsequent frame is deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane/transmit clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The previous frame is repeated.

A slip operation is always performed on a frame boundary.

When the ingress timing is recovered from the receive data, the ingress elastic store can be bypassed to eliminate the 2 frame delay.

To allow for the extraction of signaling information in the data channels, superframe identification is also passed through the ELST.

For payload conditioning, the ingress ELST may optionally insert a programmable idle code into all channels when the framer is out of frame synchronization. This code is set to all 1's when the ELST is reset.

9.6 T1/E1 Signaling Extraction

Channel associated signaling (CAS) is extracted from an E1 signaling multi-frame or from ESF, SLC®96 and SF T1 formats.

In T1 mode, signaling bits are extracted from the received data streams for ESF, SLC®96 and SF framing formats. The signaling states are optionally debounced and serialized onto the CASID[x] H-MVIP outputs or CAS bits within the SBI Bus structure. Debouncing is performed on the entire signaling state. This CASID[x] output is channel aligned with the MVID[x] output, and the signaling bits are repeated for the entire superframe, allowing downstream logic to reinsert signaling into any frame, as determined by system timing. The signaling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5, 6, 7 and 8) in ESF framing format. In SF and SLC®96 format, bits 5 and 6 contain the A and B bits from every second superframe. Bits 7 and 8 contain the A and B bits from the alternate superframes. The four bits are updated every 24 frames and are debounced collectively.

Three superframes for ESF and six superframes for SLC®96 and SF worth of signal are buffered to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801. With signaling debounce enabled, the per-channel signaling state must be in the same state for 2 ESF superframes or 4 SF/SLC®96 superframes before appearing on the serial output stream.

One superframe or signaling-multiframe of signal freezing is provided on the occurrence of slips. When a slip event occurs, output signaling for the entire superframe in which the slip occurred is frozen; the signaling is unfrozen when the next slip-free superframe occurs.

Control over timeslot signaling bit fixing and signaling debounce is provided on a per-timeslot basis.

An interrupt is provided to indicate a change of signaling state on a per channel basis.

9.7 T1/E1 Receive Per-Channel Control

Data and signaling trunk conditioning may be applied on the ingress stream on a per-channel basis. Also provided is per-channel control of data inversion and the detection and generation of pseudo-random patterns. These operations occur on the data after its passage through frame slip buffer, so that data and signaling conditioning may overwrite the trouble code.

9.8 T1 Transmitter

The T1 transmitter generates the 1.544 Mbit/s T1 data streams according to SF, SLC®96 or ESF frame formats.

The transmitter provides per-channel control of idle code substitution, data inversion (either all 8 bits, sign bit magnitude or magnitude only), and zero code suppression. Three types of zero code suppression (GTE, Bell and "jammed bit 8") are supported and selected on a per-channel basis to provide minimum ones density control. Context bits provide per-channel control of robbed bit signaling and selection of the signaling source. All channels can be forced into a trunk conditioning state by the Master Trunk Conditioning (MTRK) context bit. The transmitter may source pseudo-random bit sequences (PRBS) in a selected sub-set of channels, while simultaneously monitoring the data from the system interface for PRBS errors.

A data link is provided for ESF mode. The data link sources include bit oriented codes and HDLC messages. If the T1_FDL_DIS context bit is logic 1, the data link is sourced from the F-bit position of the SBI interface. Support is provided for the transmission of framed or unframed Inband Code sequences and transmission of AIS, Yellow, AIS-CI and RAI-CI (ESF only) alarm signals for all formats.

If the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1, the T1 transmitter automatically sends an ANSI T1.403-formatted performance report on the T1 facility data link once per second.

The F-bit may be passed transparently from the SBI interface.

Note: In SBI mode (with the transmit Elastic store enabled) the F-bit will not be aligned to CMVFPB or the SBI PP bits.

The transmitter can be disabled for framing via the FDIS context bit.

9.8.1 SLC®96

SLC®96 is partially supported. The F-bits must be sourced from the system interface. To pass the F-bits transparently, the FDIS context bit must be set. Also, a superframe alignment must be provided to ensure the robbed-bit signaling is inserted in the correct frames relative to the F-bits. To ensure the framing is not corrupted, the timing must be configured to avoid controlled frame slips.

The SBI system interface must be used to implement SLC-96. Further, the transmit elastic store must be bypassed and it is recommended the transmit clock be locked to the data stream (i.e. TJAT LOOPT and REFSEL context bits logic 0).

9.8.2 T1 Bit Oriented Code Generation

63 of the possible 64 bit oriented codes may be transmitted in the Facility Data Link (FDL) channel in ESF framing format, as defined in ANSI T1.403-1995. When transmission is disabled the FDL is set to all ones.

Bit oriented codes are transmitted on the T1 Facility Data Link as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. When driving the T1 facility data link, the transmitted bit oriented codes have priority over any data transmitted except for ESF Yellow Alarm. The code to be transmitted is programmed by writing to the BOC code context bits where it is held until the latest code has been transmitted at least 10 times. If a second code is written before ten repetitions of the first have been transmitted, the second code will be transmitted immediately after the tenth transmission of the first code. If a third consecutive code is desired, its write must be delayed until the transmission of the second code has started, lest the third code over write the second.

9.9 E1 Transmitter

The E1 transmitter generates a 2048 kbit/s data streams according to ITU-T recommendations, providing individual enables for frame generation, CRC multiframe generation, and channel associated signaling (CAS) multiframe generation.

The E1 transmitter provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data. All timeslots can be forced into a trunk conditioning state (idle code substitution and signaling substitution) by use of the master trunk conditioning (MTRK) context bit. The transmitter may source pseudo-random bit sequences (PRBS) in a selected sub-set of channels, while simultaneously monitoring the data from the system interface for PRBS errors.

Common Channel Signaling (CCS) is supported in time slots 15, 16 and 31. Support is provided for the transmission of AIS and TS16 AIS, and the transmission of remote alarm (RAI) and remote multiframe alarm signals.

The National Use bits (Sa-bits) can be sourced from the National Bits Codeword context bits as 4-bit codewords aligned to the submultiframe. Alternatively, the Sa-bits may individually carry data links sourced from the internal HDLC controller, or may be passed transparently from the MVED[x] inputs.

9.10 T1/E1 HDLC Transmitters

The HDLC transmitter provides a serial data link for the 4 kHz ESF facility data link or E1 Sa-bit data link. The data link may also be presented in any sub-set of bits within a selected DS0. The HDLC transmitter is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) may be appended, followed by flags. If the HDLC transmitter data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the HDLC transmitter continuously transmits the flag sequence (01111110) until data is ready to be transmitted.

The default procedure provides automatic transmission of data once a complete packet is written. All complete packets of data will be transmitted. After the last data byte of a packet, the CRC word (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The HDLC transmitter then returns to the transmission of flag characters until the next packet is available for transmission. While working in this mode, the user must only be careful to avoid overfilling the FIFO; underruns cannot occur unless the packet is greater than 128 bytes long. The HDLC transmitter minimum packet size is 2 bytes.

A second mechanism transmits data when the FIFO depth has reached a user configured upper threshold. The HDLC transmitter will continue to transmit data until the FIFO depth has fallen below the upper threshold and the transmission of the last packet with data above the upper threshold has completed. In this mode, the user must be careful to avoid overruns and underruns. An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data.

Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO falls below a lower threshold, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting the ABT bit. During packet transmission, an underrun situation can occur if data is not written before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDRI interrupt.

9.11 T1/E1 Receive and Transmit Digital Jitter Attenuators

The TE-32 contains two separate jitter attenuators, one between the line side receive T1 or E1 link and the ingress interface and the other between the egress interface and the line side transmit T1 or E1 link. Each jitter attenuator receives jittered data and stores the stream in a FIFO timed to the associated clock. The jitter attenuated data emerges from the FIFO timed to the jitter attenuated clock. In the receive jitter attenuator, the jitter attenuated clock is referenced to the demultiplexed or demapped tributary receive clock. In the transmit jitter attenuator, the jitter attenuated transmit tributary clock feeding the line side SBI interface may be referenced to either the data stream, the CTCLK primary input, or the tributary receive clock.

The following describes the T1/E1 jitter attenuators in isolation. The system and network in which the TE-32 device operates may alter the jitter characteristics of the T1/E1 tributaries.

9.11.1 Jitter Characteristics

The jitter attenuators provide excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. In T1 mode, each jitter attenuator can accommodate up to 48 Uipp of input jitter at jitter frequencies above 4 Hz. For jitter frequencies below 4 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In E1 mode each jitter attenuator can accommodate up to 48 Uipp of input jitter at jitter frequencies above 5 Hz. For jitter frequencies below 5 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications, each jitter attenuator will limit jitter tolerance at lower jitter frequencies only. The jitter attenuator meet the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and ITU-T Recommendation G.823, and thus allow compliance with these standards and the other less stringent jitter tolerance standards cited in the references.

The jitter attenuators exhibit negligible jitter gain for jitter frequencies below 3.4 Hz, and attenuate jitter at frequencies above 3.4 Hz by 20 dB per decade in T1 mode. They exhibit negligible jitter gain for jitter frequencies below 5 Hz, and attenuates jitter at frequencies above 5 Hz by 20 dB per decade in E1 mode. In most applications the jitter attenuators will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through the jitter attenuators. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the waiting time jitter introduced by mapping into SBI. The jitter attenuator allows the implied T1 jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met. The jitter attenuator meets the E1 jitter attenuation requirements of the ITU-T Recommendations G.737, G.738, G.739 and G.742.

9.11.2 Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For T1 modes the jitter attenuator input jitter tolerance is 48 Unit Intervals peak-to-peak (Uipp) with a worst case frequency offset of 278 Hz. For E1 modes the input jitter tolerance is 48 Unit Intervals peak-to-peak (Uipp) with a worst case frequency offset of 369 Hz.

Figure 7 Jitter Tolerance T1 Modes

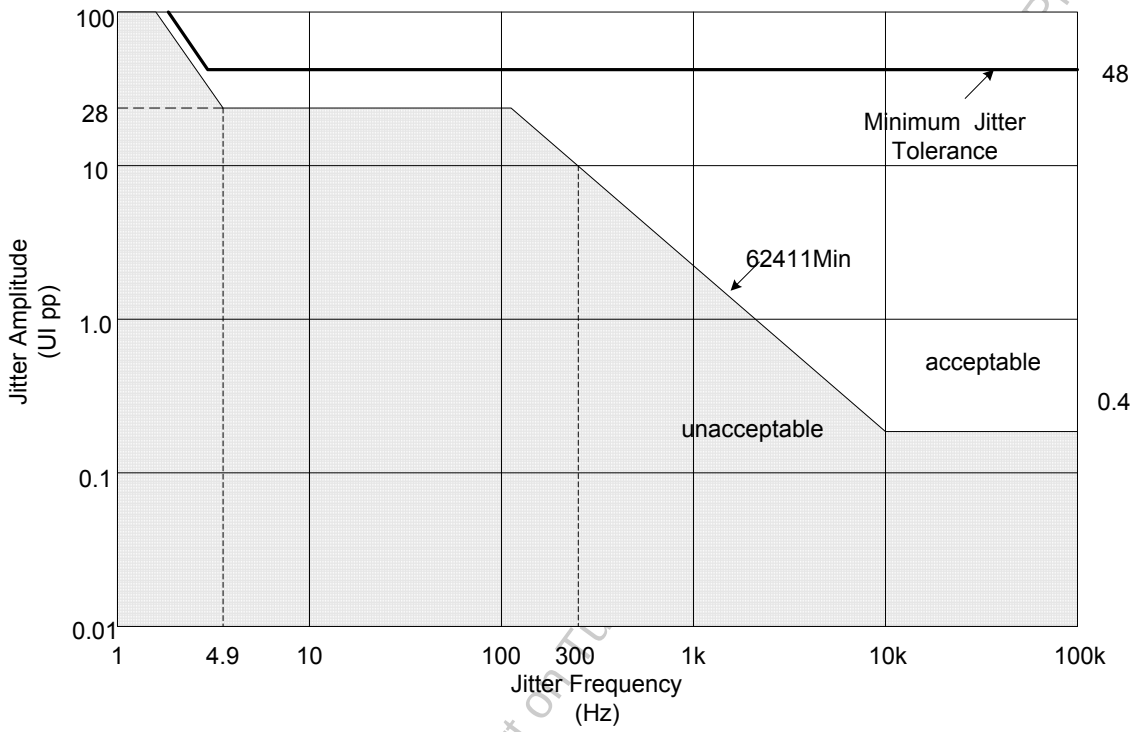
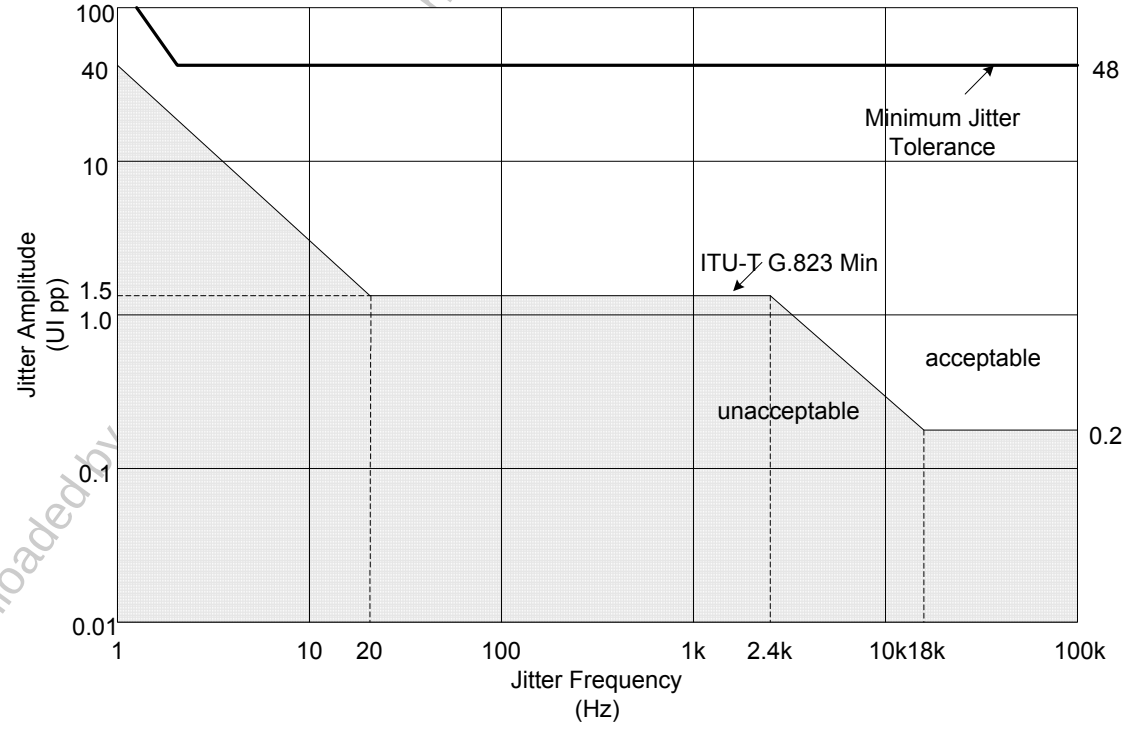


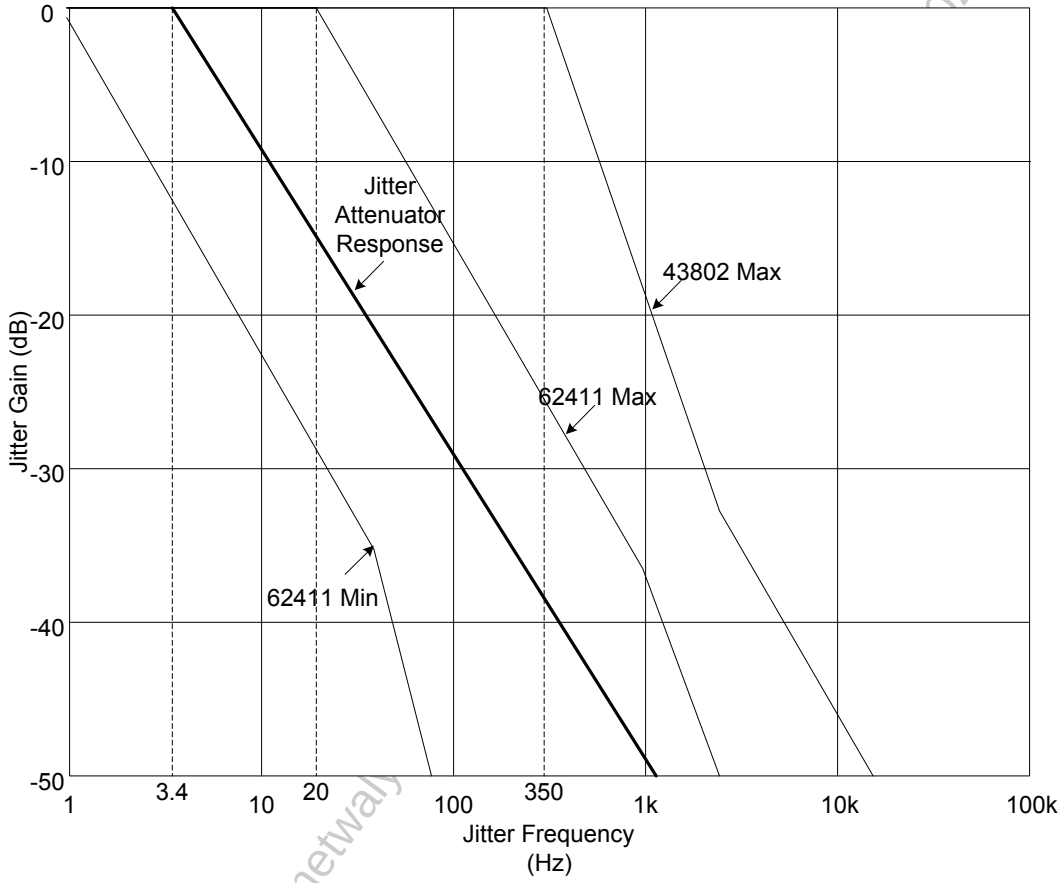
Figure 8 Jitter Tolerance E1 Modes



9.11.3 Jitter Transfer

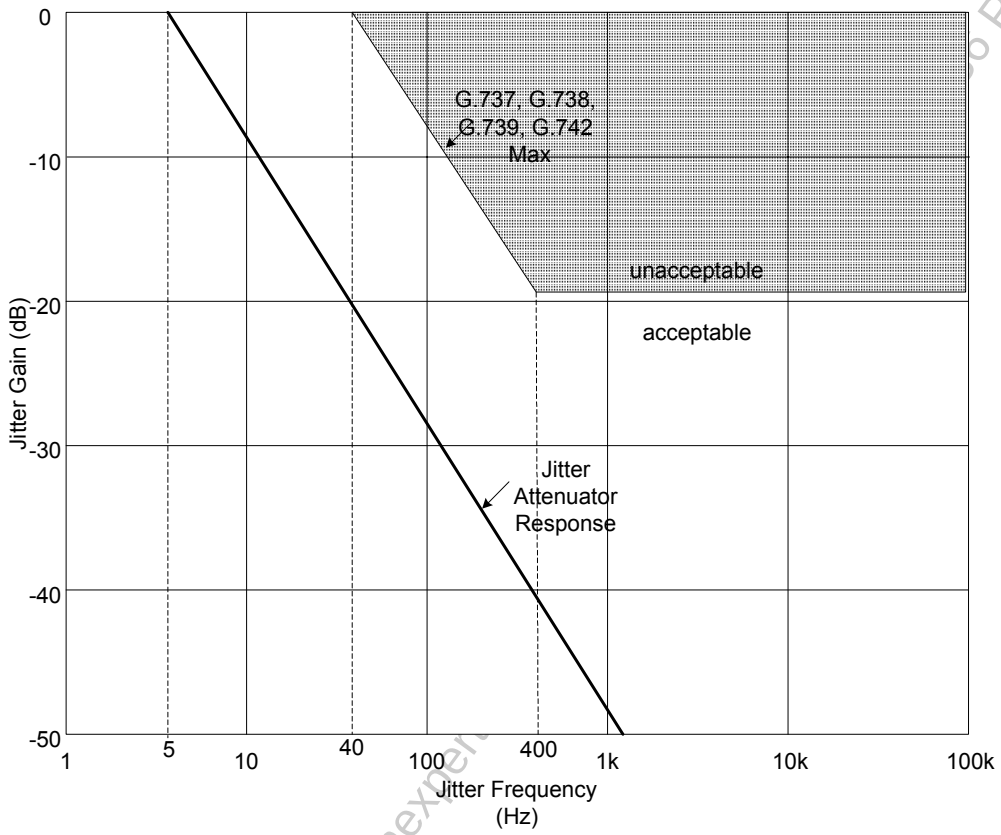
The output jitter in T1 mode for jitter frequencies from 0 to 3.4 Hz is no more than 0.1 dB greater than the input jitter, excluding the residual jitter. Jitter frequencies above 3.4 Hz are attenuated at a level of 20 dB per decade, as shown in Figure 9.

Figure 9 Jitter Transfer T1 Modes



The output jitter in E1 mode for jitter frequencies from 0 to 5.0 Hz is no more than 0.1 dB greater than the input jitter, excluding the residual jitter. Jitter frequencies above 2.5 Hz are attenuated at a level of 20 dB per decade, as shown in Figure 10.

Figure 10 Jitter Transfer E1 Modes



9.11.4 Frequency Range

The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (48 Uipp) and maximum SREFCLK frequency offset (± 50 ppm). The tracking range is 1.544 MHz ± 997 Hz with no jitter or SREFCLK frequency offset.

The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 266 Hz with worst case jitter (48 Uipp) and maximum SREFCLK frequency offset (± 50 ppm). The tracking range is 2.048 MHz ± 999 Hz with no jitter or SREFCLK frequency offset.

9.12 T1/E1 Pseudo Random Binary Sequence Generation and Detection (PRBS)

The Pseudo Random Binary Sequence Generator/Detector (PRBS) is a software selectable PRBS generator and checker for 2^7-1, 2^{11}-1, 2^{15}-1 or 2^{20}-1 PRBS polynomials for use in the T1 and E1 links. PRBS patterns may be generated and monitored in both the transmit or receive directions for all T1 and E1 links simultaneously. The generator is capable of inserting single bit errors under microprocessor control.

The following pseudo random bit sequences are supported:

Sequence Length	Polynomial
$2^{11} - 1$	$x^{11} + x^9 + 1$
$2^{15} - 1$	$x^{15} + x^{14} + 1$
$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
$2^{20} - 1$	$x^{20} + x^3 + 1$
$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

The detector auto-synchronizes to the expected PRBS pattern and accumulates the total number of bit errors in a 16-bit counter. The error count accumulates over the interval defined by writes to the Global PMON Update register. When a transfer is triggered, the holding register is updated, and the counter reset to begin accumulating for the next interval. The counter is reset in such a way that no events are missed. The data is then available until the next transfer.

In addition to the basic PRBS generators and receivers associated with each T1/E1 link, six full featured pattern generator/detector pairs are available for association with any software selectable link. Any subset of bits within a frame (except the T1 F-bit) may be programmed to carry either a pseudo-random or fixed pattern.

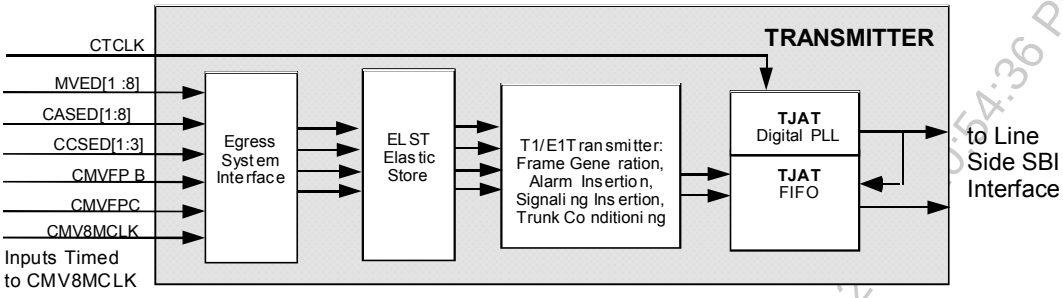
The six generators can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. It also can generate the four DDS codes specified by Bellcore GR-819-CORE. In addition, the pattern generator can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The six receivers can be programmed to check for the generated pseudo random pattern. The receivers can perform an auto synchronization to the expected pattern and accumulates the total number of bits received and the total number of bit errors in two 32-bit counters. If a repetitive pattern is selected, the receiver will synchronize to any bit sequence that repeats with the programmed periodicity. A bit error accumulates when a bit disagrees with the original bit sequence synchronized to. The counters accumulate either over intervals defined by writes to the Pattern Detector registers or upon writes to the Global PMON Update Register. When a transfer is triggered, the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next transfer.

9.13 Egress H-MVIP System Interface

The Egress H-MVIP System Interface (Figure 11) provides system side H-MVIP access for up to 32 T1 or E1 transmit streams. There are three separate interfaces for data, CAS signaling and CCS signaling. The H-MVIP signaling interfaces can be used in combination with the SBI interface in certain applications. Control of the system side interface is global to TE-32 and is selected through the SYSOPT[1:0] bits in the Global Configuration register. The system interface options are H-MVIP, SBI bus and SBI bus with CAS or CCS H-MVIP.

Figure 11 Egress Clock Slave H-MVIP



When Clock Slave: H-MVIP mode is enabled a 8.192 Mbit/s H-MVIP egress interface multiplexes up to 768 channels from 32 T1s or E1s, up to 768 channel associated signaling (CAS) channels from 32 T1s or E1s and common channel signaling from up to 32 T1s or E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

Eight H-MVIP data signals, MVED[1:8], share pins with the SBI inputs to provide H-MVIP access for up to 768 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links make up the individual 8.192 Mbit/s H-MVIP signal. This mode is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to H-MVIP.

The option exists to transmit at a rate locked to the CTCLK input or to be looped timed. Regardless of transmit timing source, the transmit elastic store may not be bypassed. To avoid controlled frame slips, the source of the transmit timing needs to be traceable to the source of the CMV8MCLK input.

A separate eight signal H-MVIP interface is for access to the channel associated signaling for 768 channels. The CAS H-MVIP interface is time division multiplexed exactly the same way as the data channels. The CAS H-MVIP is synchronized with the H-MVIP data channels when SYSOPT[1:0] is set to H-MVIP mode. Over a T1 or E1 multi-frame, the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in parallel with each data byte. Optionally, the third and fourth bit of each byte may be used as inband control of whether CAS signalling is inserted or whether the timeslot is 64 kbit/s clear channel.

The CAS H-MVIP interface can be used in parallel with the SBI Add bus as an alternative method for accessing the CAS bits while data transfer occurs over the SBI bus. This is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to “SBI Interface with CAS or CCS H-MVIP Interface”.

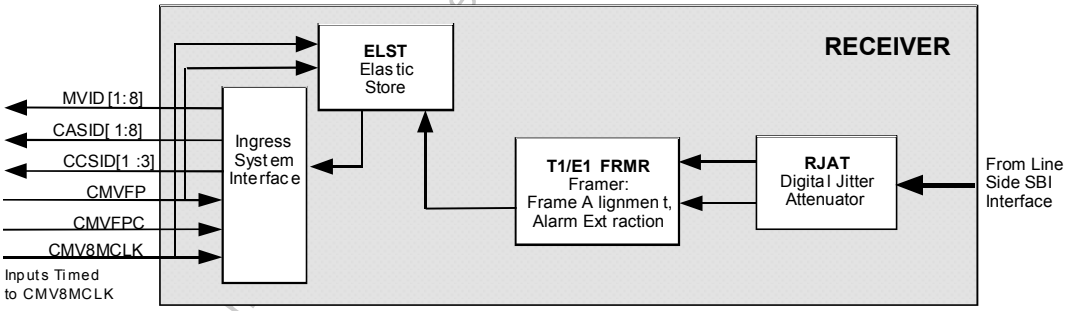
A separate H-MVIP interface consisting of three signals is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSED[1:3], is not multiplexed with any other pins. CCSED[1:3] can be used in parallel with the Clock Slave:H-MVIP mode when SYSOPT[1:0] is set to "H-MVIP Interface" or in parallel with the SBI Add bus when SYSOPT[1:0] is set to "SBI Interface with CAS or CCS H-MVIP Interface". The TS16 CCS and V5 channels for E1 tributaries and channel 24 CCS for T1 tributaries can be enabled when the CCS16EN, CCS15EN, CCS31EN and/or CCSEN context bits are set to logic 1 through the T1/E1 Transmitter Indirect Channel Data Registers.

When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with the SBI interface a transmit signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

9.14 Ingress System H-MVIP Interface

The Ingress System Interface (Figure 12) provides H-MVIP access for up to 32 T1 or E1 receive streams. When enabled for 8.192 Mbit/s H-MVIP there are three separate interfaces for data and signaling. The H-MVIP signaling interfaces can be used in combination with the SBI interface in certain applications. Control of the system side interface is global to TE-32 and is selected through the SYSOPT[1:0] bits in the Global Configuration register at address 0x0002. The system interface options are H-MVIP, SBI bus and SBI bus with CAS or CCS H-MVIP. The ingress H-MVIP interface is always a clock slave.

Figure 12 Ingress Clock Slave H-MVIP



When Clock Slave: H-MVIP mode is enabled a 8.192 Mbit/s H-MVIP ingress interface multiplexes up to 768 channels from 32 T1s or E1s, up to 768 channel associated signaling (CAS) channels from 32 T1s or E1s and common channel signaling (CCS) from up to 32 T1s or E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

The three ingress H-MVIP interfaces operate independently except that using any one of these forces the T1 or E1 framer to operate in synchronous mode, meaning that elastic stores are used.

Eight H-MVIP data signals, MVID[1:8] provide H-MVIP access for up to 768 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links make up the individual 8.192 Mbit/s H-MVIP signal. This mode is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to H-MVIP.

A separate H-MVIP interface consisting of eight pins is for access to the channel associated signaling for all of the 768 data channels. The CAS is time division multiplexed exactly the same way as the data channels and is synchronized with the H-MVIP data channels. Over a T1 or E1 multi-frame, the four CAS bits per channel are repeated with each data byte.

The CAS H-MVIP interface can be used in parallel with the SBI Drop bus as an alternative method for accessing the CAS bits while data transfer occurs over the SBI bus. This is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to "SBI Interface with CAS or CCS H-MVIP Interface".

A separate H-MVIP interface consisting of three signals is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSID[1:3], is not multiplexed with any other pins. The CCSID[1:3] outputs are always available provided CMV8MCLK, CMVFPB and CMVFPC are active.

The TS0ID output provides the contents of E1 TS0.

When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with the SBI interface a receive signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

9.15 Extract Scaleable Bandwidth Interconnect (EXSBI)

The Extract Scaleable Bandwidth Interconnect block demaps up to 32 1.544 Mbit/s links, 32 2.048 Mbit/s links from the SBI shared bus. The 1.544 Mbit/s links can be unframed (on the line side) or they can be T1 framed (on the system side). The 2.048 Mbit/s links can be unframed (line side) or they can be E1 framed (system side). The SBI Bus Data Formats section provides the details of the mapping formats.

9.15.1 System Side SBI Add Bus

All egress links extracted from the SBI bus can be timed from the source or from the TE-32. When timing is from the source, the 1.544 Mbit/s or 2.048 Mbit/s, internal clocks are slaved to the arrival rate of the data. A T1/E1 tributary may be transmitted at a rate different from that of the SBI bus if the tributary is looped timed or locked to the CTCLK input. In this case, the frame slip buffer (ELST) must be used to adapt the data rate.

When the TE-32 is the SBI egress clock master for a link, clocks are sourced from within the TE-32. The data rate is set by the frequency of the CTCLK input. Based on buffer fill levels, the EXSBI sends link rate adjustment commands to the link source indicating that it should send one additional or one fewer bytes of data during the next 500 µS interval. Failure of the source to respond to these commands will ultimately result in overflows or underflows which can be configured to generate per link interrupts.

Channelized T1s extracted from the SBI bus optionally have the channel associated signaling (CAS) bits explicitly defined and carried in parallel with the DS0s.

9.15.2 Line Side SBI Drop Bus

The line side SBI Drop bus can only be a timing slave. It has no mechanism for requesting justifications; it simply accepts tributary bytes at the rate offered.

For T1, any out of band signaling that may be encoded in $S_1S_2S_3S_4$ bits is ignored on the line side SBI Drop bus. The PP bits are ignored. It is assumed the signaling is transported in the robbed bit positions of the DS0s. For E1, the signaling multiframe alignment is not communicated via the PP bits. The E1 framer establishes signaling multiframe assuming TS16 contains a valid multiframe alignment pattern.

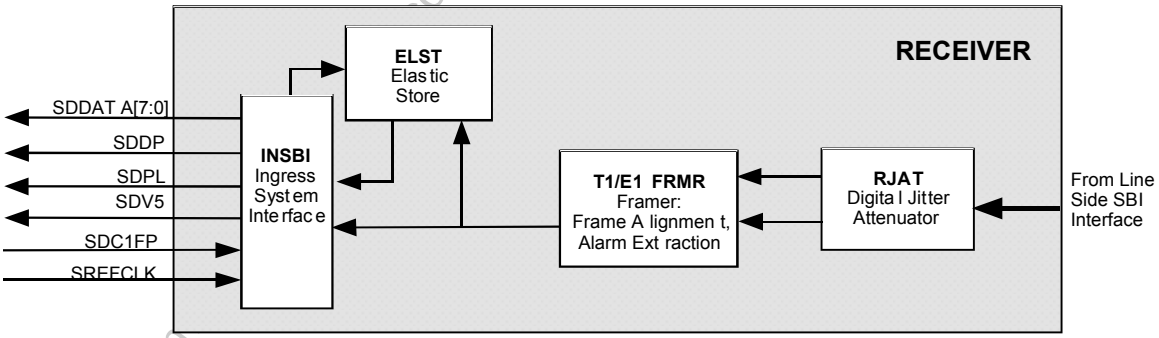
Note: Multiple TE-32's cannot be connected to the same Line Side SBI bus.

9.16 Insert Scaleable Bandwidth Interconnect (INSBI)

The Insert Scaleable Bandwidth Interconnect block maps up to 32 1.544 Mbit/s links or 32 2.048 Mbit/s links into the SBI shared bus. The 1.544 Mbit/s and 2.048 Mbit/s links can be unframed (on the line side), or they can be T1/E1 channelized when sourced by the T1/E1 framers (on the system side). The SBI Bus Data Formats section provides the details of the mapping formats.

9.16.1 System Side SBI Drop Bus

Figure 13 Insert SBI System Interface



Links inserted into the SBI bus can be synchronous to the SBI bus (by setting SYNCH_TRIB=1 in the INSBI Control RAM) or timed from the upstream data source via the line side SBI bus. When SYNCH_TRIB is logic 0, the INSBI makes link rate adjustments by adding or deleting an extra byte of data over a 500 µS interval based on buffer fill levels. Timing adjustments are detected by the receiving SBI interface by explicit signals in the SBI bus structure. When SYNCH_TRIB is logic 1, the tributary is "locked" in which no timing adjustments are allowed. The frame slip buffer (ELST) must be in the datapath in "locked" mode, and the incoming link must not be configured as "unframed data" since the frame slip buffers expect to use framing information to perform the controlled slips (full frame slips) needed to frequency align the incoming tributary with the SBI bus.

The INSBI always sends valid link rate information across the SBI Drop bus, which contains both ClkRate(1:0) and Phase(3:0) field information. This gives an external device receiving data from the INSBI three methods of creating a recovered link clock: the ClkRate field, the Phase field, or just the rate of data flow across the SBI drop bus.

Channelized T1s inserted into the SBI bus optionally have the channel associated signaling (CAS) bits explicitly defined and carried in parallel with the DS0s or timeslots.

9.16.2 Line Side SBI Add Bus

In a strict sense, the line side SBI Add Bus is best thought of as SBI compatible as opposed to compliant to the full SBI bus definition.

The line side SBI Add Bus can only act as a timing master; it has no AJUST_REQ input by which to receive flow control information. The link rates are determined by the CTCLK input by system interface bit rates.

There is no collision detection capability via SBIDET and SBIACT signals. Instead, parity is provided for the detection of data corruption and mis-configuration.

For T1, the $S_1S_2S_3S_4$ bits are unused. Any channel associated signaling is transported in the robbed bit positions of the DS0s. The PP bits are generated, but they carry no useful information. For E1, the signaling multiframe alignment is not communicated; the PP octet is irrelevant. A valid signaling multiframe alignment pattern is encoded in TS16.

Note: Multiple TE-32's cannot be connected to the same Line Side SBI bus.

9.17 Transparent Tributaries

Transparent Tributaries (TTs) are supported on the egress datapath between the Line Side SBI Bus and the System Side SBI Bus. Conceptually, a TT is passed straight from the System Side SBI Bus to the Line Side SBI Bus with no knowledge of the mapping protocol or T1/E1 framing.

The Clock and Frame Synchronization Constraints section indicates constraints on bus alignments imposed by TT support.

Note: TT mode is recommended when using unstructured AAL1 with the OCTLIU (PM4318) - TE-32 – AAL1gator32 (PM73122) devices.

9.18 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The TE-32 identification code is 183160CD hexadecimal.

9.19 Microprocessor Interface

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Microprocessor Interface.

The Register Memory Map in Table 2 shows where the normal mode registers are accessed. The resulting register organization splits into sections: Master configuration registers, T1/E1 Framer registers and SBI registers.

On power up reset the TE-32 defaults to 32 T1 framers with the SBI buses disabled. System side access defaults to the SBI bus without any tributaries enabled which will leave the SBI Drop bus tristated. By default interrupts will not be enabled and automatic alarm generation is disabled. For proper operation some register configuration is necessary.

Table 2 Register Memory Map

Address	Register
0x0000	Revision
0x0001	Global Reset
0x0002	Global Configuration
0x0003	SPE #1 Configuration
0x0004	SPE #2 Configuration
0x0005	SPE #3 Configuration
0x0006	Bus Configuration
0x0007	Global Performance Monitor Update
0x0008	Reference Clock Select
0x000C	Master H-MVIP Interface Configuration
0x000D	Master Clock Monitor #1
0x0010	Master Interrupt Source
0x0011	Master Interrupt Source T1E1
0x0012	Master Interrupt Source Line Side SBI
0x0015	Master Interrupt Source System Interface SBI
0x0020	Master SBIDET0 Collision Detect LSB
0x0021	Master SBIDET0 Collision Detect MSB
0x0022	Master SBIDET1 Collision Detect LSB
0x0023	Master SBIDET1 Collision Detect MSB
0x0040	T1/E1 Master Configuration
0x0042	T1/E1 PRGD #1 Tributary Select

Address	Register
0x0043	T1/E1 PRGD #2 Tributary Select
0x0044	T1/E1 PRGD #3 Tributary Select
0x0045	T1/E1 PRGD #4 Tributary Select
0x0046	T1/E1 PRGD #5 Tributary Select
0x0047	T1/E1 PRGD #6 Tributary Select
0x0048	RJAT Indirect Status
0x0049	RJAT Indirect Channel Address Register
0x004A	RJAT Indirect Channel Data Register
0x004B	RJAT Programmable Corner Frequency Register
0x004C	TJAT Indirect Status
0x004D	TJAT Indirect Channel Address Register
0x004E	TJAT Indirect Channel Data Register
0x004F	TJAT Programmable Corner Frequency Register
0x0050	RPCC-MVIP Indirect Status/Time-slot Address
0x0051	RPCC-MVIP Indirect Channel Address Register
0x0052-0x0056	RPCC-MVIP Indirect Channel Data Registers
0x0057	RPCC-MVIP Configuration Bits
0x0058 – 0x005D	RPCC-MVIP Interrupt Status
0x0063	RPCC-MVIP PRBS Error Insertion
0x0064	RPCC-MVIP PRBS Error Insert Status
0x0068	RPCC-SBI Indirect Status/Time-slot Address
0x0069	RPCC-SBI Indirect Channel Address Register
0x006A-0x006E	RPCC-SBI Indirect Channel Data Registers
0x006F	RPCC-SBI Configuration Bits
0x0070 – 0x0075	RPCC-SBI Interrupt Status
0x007B	RPCC-SBI PRBS Error Insertion
0x007C	RPCC-SBI PRBS Error Insert Status
0x0083	RX-MVIP-ELST Idle Code
0x0084 – 0x0086, 0x0088, 0x0089	RX-MVIP-ELST Slip Status
0x0087, 0x008A – 0x008E	RX-MVIP-ELST Reserved
0x008F – 0x0094	RX-MVIP-ELST Slip Direction
0x009A	RX-MVIP-ELST Slip Interrupt Enable
0x00A0	RX-SBI-ELST Indirect Status
0x00A1	RX-SBI-ELST Indirect Channel Address Register
0x00A2	RX-SBI-ELST Indirect Channel Data Register
0x00A3	RX-SBI-ELST Idle Code
0x00A4 – 0x00A6, 0x00A8, 0x00A9	RX-SBI-ELST Slip Status

Address	Register
0x00A7, 0x00AA – 0x00AE	RX-SBI-ELST Reserved
0x00AF – 0x00B4	RX-SBI-ELST Slip Direction
0x00BA	RX-SBI-ELST Slip Interrupt Enable
0x00C0	TX-ELST Indirect Status
0x00C1	TX-ELST Indirect Channel Address Register
0x00C2	TX-ELST Indirect Channel Data Register
0x00C4 – 0x00C6, 0x00C8, 0x00C9	TX-ELST Slip Status
0x00C7, 0x00CA – 0x00CE	TX-ELST Reserved
0x00CF – 0x00D4	TX-ELST Slip Direction
0x0DA	TX-ELST Slip Interrupt Enable
0x0100	TPCC Indirect Status/Time-slot Address
0x0101	TPCC Indirect Channel Address Register
0x0102-0x0106	TPCC Indirect Channel Data Registers
0x0107	TPCC Configuration
0x0108 – 0x010D	TPCC Interrupt Status
0x0113	TPCC PRBS Error Insertion
0x0114	TPCC PRBS Error Insert Status
0x0118	RHDL Indirect Status
0x0119	RHDL Indirect Channel Address Register
0x011A – 0x011D	RHDL Indirect Channel Data Registers
0x011E	RHDL Interrupt Control
0x011F – 0x0124	RHDL Interrupt Status
0x0130	THDL Indirect Status
0x0131	THDL Indirect Channel Address Register
0x0132 – 0x0136	THDL Indirect Channel Data Registers
0x0137 – 0x013C	THDL Interrupt Status
0x0150	SIGX Indirect Status/Time-slot Address
0x0151	SIGX Indirect Channel Address Register
0x0152 – 0x0156	SIGX Indirect Channel Data Registers
0xx157	SIGX Configuration
0x0158 – 0x015D	Change of Signaling Status
0x0163	Change of Signaling Status Interrupt Enable
0x0168	T1/E1 Transmitter Indirect Status
0x0169	T1/E1 Transmitter Indirect Channel Address
0x016A – 0x016F	T1/E1 Transmitter Indirect Channel Data Registers
0x0170	T1/E1 Framer Indirect Status
0x0171	T1/E1 Framer Indirect Channel Address Register

Address	Register
0x0172 – 0x0186	T1/E1 Framer Indirect Channel Data Registers
0x0187	T1/E1 Framer Configuration and Status
0x0188 – 0x018D	T1/E1 Framer Interrupt Status
0x01C0	System Side SBI Master Reset / Bus Signal Monitor
0x01C1	System Side SBI Master Configuration
0x01C2	System Side SBI Bus Master Configuration
0x01C4	System Side SBI DLL Configuration
0x01C6	System Side SBI DLL Tap Status
0x01C7	System Side SBI DLL Control Status
0x01D0	System Side EXSBI Control
0x01D1	System Side EXSBI FIFO Underrun Interrupt Status
0x01D2	System Side EXSBI FIFO Overrun Interrupt Status
0x01D3	System Side EXSBI Tributary RAM Indirect Access Address
0x01D4	System Side EXSBI Tributary RAM Indirect Access Control
0x01D5	System Side EXSBI Tributary Mapping Indirect Access Data
0x01D6	System Side EXSBI Tributary Control Indirect Access Data
0x01D7	System Side SBI Parity Error Interrupt Status
0x01D8	System Side EXSBI MIN_DEPTH for T1 and E1 Register
0x01DA	System Side EXSBI T1 Thresholds Register
0x01DB	System Side EXSBI E1 Thresholds Register
0x01DE	System Side EXSBI Depth Check Interrupt Status
0x01DF	System Side EXSBI FIFO Control
0x01E0	System Side INSBI Control
0x01E1	System Side INSBI FIFO Underrun Interrupt Status
0x01E2	System Side INSBI FIFO Overrun Interrupt Status
0x01E3	System Side INSBI Tributary Indirect Access Address
0x01E4	System Side INSBI Tributary Indirect Access Control
0x01E5	System Side INSBI Tributary Mapping Indirect Access Data
0x01E6	System Side INSBI Tributary Control Indirect Access Data
0x01E7	System Side INSBI MIN_DEPTH for T1 and E1 Register
0x01E9	System Side INSBI T1 Thresholds Register
0x01EA	System Side INSBI E1 Thresholds Register
0x01F1	System Side INSBI Depth Check Interrupt Status
0x01F2	System Side INSBI External ReSynch Interrupt Status
0x0500, 0x0520, 0x0540, 0x0560, 0x0580, 0x05A0	T1/E1 Pattern Generator and Detector Control
0x0501, 0x0521, 0x0541, 0x0561, 0x0581, 0x05A1	T1/E1 Pattern Generator and Detector Interrupt Enable/Status
0x0502, 0x0522, 0x0542, 0x0562, 0x0582, 0x05A2	T1/E1 Pattern Generator and Detector Length

Address	Register
0x0503, 0x0523, 0x0543, 0x0563, 0x0583, 0x05A3	T1/E1 Pattern Generator and Detector Tap
0x0504, 0x0524, 0x0544, 0x0564, 0x0584, 0x05A4	T1/E1 Pattern Generator and Detector Error Insertion
0x0508, 0x0528, 0x0548, 0x0568, 0x0588, 0x05A8	T1/E1 Pattern Generator and Detector Pattern Insertion #1
0x0509, 0x0529, 0x0549, 0x0569, 0x0589, 0x05A9	T1/E1 Pattern Generator and Detector Pattern Insertion #2
0x050A, 0x052A, 0x054A, 0x056A, 0x058A, 0x05AA	T1/E1 Pattern Generator and Detector Pattern Insertion #3
0x050B, 0x052B, 0x054B, 0x056B, 0x058B, 0x05AB	T1/E1 Pattern Generator and Detector Pattern Insertion #4
0x050C, 0x052C, 0x054C, 0x056C, 0x058C, 0x05AC	T1/E1 Pattern Generator and Detector Pattern Detector #1
0x050D, 0x052D, 0x054D, 0x056D, 0x058D, 0x05AD	T1/E1 Pattern Generator and Detector Pattern Detector #2
0x050E, 0x052E, 0x054E, 0x056E, 0x058E, 0x05AE	T1/E1 Pattern Generator and Detector Pattern Detector #3
0x050F, 0x052F, 0x054F, 0x056F, 0x058F, 0x05AF	T1/E1 Pattern Generator and Detector Pattern Detector #4
0x0510, 0x0530, 0x0550, 0x0570, 0x0590, 0x05B0	Generator Controller Configuration
0x0511, 0x0531, 0x0551, 0x0571, 0x0591, 0x05B1	Generator Controller µP Access Status
0x0512, 0x0532, 0x0552, 0x0572, 0x0592, 0x05B2	Generator Controller Channel Indirect Address/Control
0x0513, 0x0533, 0x0553, 0x0533, 0x0593, 0x05B3	Generator Controller Channel Indirect Data Buffer
0x0514, 0x0534, 0x0554, 0x0574, 0x0594, 0x05B4	Receiver Controller Configuration
0x0515, 0x0535, 0x0555, 0x0575, 0x0595, 0x05B5	Receiver Controller µP Access Status
0x0516, 0x0536, 0x0556, 0x0576, 0x0596, 0x05B6	Receiver Controller Channel Indirect Address/Control
0x0517, 0x0537, 0x0557, 0x0577, 0x0597, 0x05B7	Receiver Controller Channel Indirect Data Buffer
0x0700	Line Side SBI Master Reset
0x0702	Line Side SBI Master Egress Configuration
0x0703	Line Side SBI Master Ingress Configuration
0x0704	Line Side SBI DLOOP Enable
0x070A	Line Side SBI Master Loopback Control
0x070B	Line Side SBI Bus Signal Monitor

Address	Register
0x0900, 0x0902, 0x0904, 0x0906, 0x0908, 0x090A, 0x090C, 0x0940, 0x0942, 0x0944, 0x0946, 0x0948, 0x094A, 0x094C	T1/E1 Mode Configuration 1
0x09C0	Line Side INSBI Control
0x09C1	Line Side INSBI FIFO Underrun Interrupt Status
0x09C2	Line Side INSBI FIFO Overrun Interrupt Status
0x09C3	Line Side INSBI Tributary Indirect Access Address
0x09C4	Line Side INSBI Tributary Indirect Access Control
0x09C6	Line Side INSBI Tributary Control Indirect Access Data
0x09C7	Line Side INSBI MIN_DEPTH for T1 and E1 Register
0x09C9	Line Side INSBI T1 Thresholds Register
0x09CA	Line Side INSBI E1 Thresholds Register
0x09D1	Line Side INSBI Depth Check Interrupt Status
0x09D2	Line Side INSBI Master Interrupt Status
0x09E0	Line Side EXSBI Control
0x09E1	Line Side EXSBI FIFO Underrun Interrupt Status
0x09E2	Line Side EXSBI FIFO Overrun Interrupt Status
0x09E3	Line Side EXSBI Tributary RAM Indirect Access Address
0x09E4	Line Side EXSBI Tributary RAM Indirect Access Control
0x09E6	Line Side EXSBI Tributary Control RAM Indirect Access Data
0x09E7	Line Side SBI Parity Error Interrupt Status
0x09E8	Line Side EXSBI MIN_DEPTH for T1 and E1 Register
0x09EA	Line Side EXSBI T1 Thresholds Register
0x09EB	Line Side EXSBI E1 Thresholds Register
0x09EE	Line Side EXSBI Depth Check Interrupt Status
0x0x9EF	Line Side EXSBI FIFO Control
0x0D00, 0x0D01, 0x0D02, 0x0D03, 0x0D04, 0x0D05, 0x0D06, 0x0D20, 0x0D21, 0x0D22, 0x0D23, 0x0D24, 0x0D25, 0x0D26	T1/E1 Mode Configuration 2
0x0D80, 0x0D81, 0x0D82, 0x0D83, 0x0D84, 0x0D85, 0x0D86, 0x0DA0, 0x0DA1, 0x0DA2, 0x0DA3, 0x0DA4, 0x0DA5, 0x0DA6	T1/E1 Mode Configuration 3
0x0E00 - 0x0E11, 0x0E20 - 0x0E31	T1/E1 Mode Configuration 4
0x1000	Master Test

For all register accesses, CSB must be low.

10 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the TE-32. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[12]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits typically has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bit must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TE-32 to determine the programming state of the block.
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect TE-32 operation unless otherwise noted.
5. Write Logic 1 to clear bits are indicated by W12C. (W12C = “Write One to Clear”)

10.1 Top Level Master Registers

Register 0x0000: Revision

Bit	Type	Function	Default
Bit 7	R	TYPE[3]	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

ID[3:0]:

The version identification bits ID[3:0], are set to a fixed value representing the version number of the TE-32. These bits can be read by software to determine the version number.

TYPE[3:0]:

The type identification bits TYPE[3:0], identify this device from other products in the same Framer family of devices.

Register 0x0001: Global Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

RESET:

The RESET bit implements a software reset for the entire TE-32. If the RESET bit is a logic 1, the entire TE-32 is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the TE-32 out of reset. Holding the TE-32 in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Register 0x0002: Global Configuration

Bit	Type	Function	Default
Bit 7	R/W	MINTE	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	SYSOPT[1]	1
Bit 0	R/W	SYSOPT[0]	0

MINTE:

The Master Interrupt Enable allows internal interrupt statuses to be propagated to the interrupt output. If MINTE is logic 1, INTB will be asserted low upon the assertion of an interrupt status bit whose individual enable is set. If MINTE is logic 0, INTB is unconditionally high-impedance.

SYSOPT[1:0]:

The System Side Options bits, SYSOPT[1:0], configure the system side interface of the TE-32. The possible system side interface selections are H-MVIP backplane interfaces, Scaleable Bandwidth Interconnect bus interface and a combination SBI bus with CAS or CCS H-MVIP interface. The following table shows the SYSOPT[1:0] values for each system side interface configuration:

SYSOPT[1:0]	System Interface Mode
00	Reserved
01	H-MVIP Interface
10	SBI Interface (default)
11	SBI Interface with CAS or CCS H-MVIP Interface

Register 0x0003: SPE #1 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	E1T1B_SPE1	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 0x0004: SPE #2 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	E1T1B_SPE2	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 0x0005: SPE #3 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	E1T1B_SPE3	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

E1T1B_SPEx:

The E1T1B_SPEx bits configure the T1/E1 framers associated with the system side SPE to be configured as either T1 framers or E1 framers. When E1T1B_SPEx is a logic 0 the T1/E1 framers are configured as T1 framers. When E1T1B_SPEx is a logic 1 the T1/E1 framers are configured as E1 framers.

The RESET bit of the T1/E1 Master Configuration register should be set then cleared after any the E1T1B_SPEx bit have been modified.

Note: All E1T1B_SPEx bits must be set to the same value, either all T1 or all E1. Mixed modes are not supported.

Reserved:

Reserved bit 4 must be set to logic 1 for correct operation. The other reserved bits must be set to the default for correct operation.

Register 0x0006: Bus Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	GSOE	0
Bit 5	R/W	SSTM[1]	1
Bit 4	R/W	SSTM[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	LADDOE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

LADDOE:

The Line ADD Bus output enable bit, LADDOE, determines if only driven for enabled links or always. When LADDOE is a logic 1, the Line ADD Bus signals are driven permanently. When LADDOE is a logic 0, the Line ADD Bus signals are driven only during valid data and are otherwise tristated.

The Line ADD Bus defaults to high impedance upon reset.

SSTM[1:0]:

These bits are only relevant when the S77 input is high.

The System Side SBI STM-1 Select bits, SSTM[1:0], determine during which one of the four byte interleaved STM-1s the TE-32 drives SADATA[7:0] and expects data on SDDATA[7:0]:

SSTM[1:0]	Byte Alignment
00	Byte aligned to SAC1FP and SDC1FP, and every fourth byte thereafter.
01	Byte after SAC1FP and SDC1FP, and every fourth byte thereafter.
10	Two bytes after SAC1FP and SDC1FP, and every fourth byte thereafter.
11	Three bytes after SAC1FP and SDC1FP, and every fourth byte thereafter.

GSOE:

The Global System Interface SBI Output Enable (GSOE) determines whether the System Interface SBI Drop bus is driven. If GSOE is logic 0, the SDDATA[7:0], SDDP, SDPL, SDV5, SBIACT, and SAJUST_REQ outputs are unconditionally high impedance. If GSOE is logic 1, these outputs drive during the programmed tributaries.

The System Interface SBI Bus defaults to high impedance upon reset.

Reserved:

These bits must be set to the default for correct operation.

Register 0x0007: Global Performance Monitor Update

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	E1T1_PRBS	0
Bit 0	R/W	E1T1_FRMR	0

Each write to this register triggers the selected performance monitors to be updated simultaneously and the associated internal counters to be reset to begin a new cycle of error accumulation. Be aware some performance counters maybe configured to be updated autonomously, so it may not be appropriate to update them via writing this register. Once transferred, the data in the microprocessor accessible registers remains valid until the next transfer.

E1T1_PRBS:

If a logic 1 is written to this bit, the E1/T1 PRBS error counts for both the receive and transmit directions are transferred to holding registers. This includes the counts associated with the Full-Featured T1/E1 Pattern Detector.

E1T1_FRMR:

If a logic 1 is written to this bit, the performance monitor counts associated with the T1/E1 framers are transferred to holding registers.

Reserved:

These bits must be set to the default for correct operation.

Register 0x0008: Reference Clock Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	REFCLK[1]	0
Bit 0	R/W	REFCLK[0]	0

REFCLK[1:0]:

The Reference Clock select bits, REFCLK[1:0], select the source of the clock to be used as the common transmit T1/E1 clock. Regardless of the state of these bits, each tributary may also be loop timed or be slave to the system interface. The following table shows the REFCLK[1:0] selections:

REFCLK[1:0]	Clock
00	CTCLK pin
01	Unused
10	Unused
11	Unused

Register 0x000C: Master H-MVIP Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CMVFPINV	1
Bit 3	R/W	CMVIFE	0
Bit 2	R/W	CMVIDE	0
Bit 1	R/W	CMMFP	0
Bit 0	R/W	CMVEDE	1

CMVEDE:

In H-MVIP mode when CMVEDE is set to logic 1, the egress H-MVIP signals (MVED[1:8], CASED[1:8], CCSED[1:3]) are sampled by the rising edge of CMV8MCLK. When CMVEDE is set to logic 0, the egress H-MVIP signals are sampled by the falling edge of CMV8MCLK.

CMMFP:

The CMMFP bit controls whether the common H-MVIP frame pulse, CMVFPB, indicates frame alignment or multiframe alignment. When CMMFP is a logic 1, the frame pulse, CMVFPB, indicates a multiframe boundary. To support any combination of SF, ESF and E1, the CMVFPB must pulse low (high if CMVFPINV is logic 0) at a multiple of 48 frames at the beginning of the frame. When CMMFP is a logic 0, CMVFPB indicates a frame boundary.

Indicating multiframe alignment assures the framing and signaling inserted by TE-32 in the transmit direction aligns to the data being presented on the H-MVIP inputs.

CMMFP has no effect on the multiframe alignment of the egress interface.

Note: Frame slips must be avoided to achieve multiframe alignment. Therefore, the transmit clock must be referenced to CTCLK and CTCLK must be frequency locked to CMVFPB when SYSOPT[1:0] equals binary 01 (H-MVIP Interface). For the System Interface SBI interface with CAS or CCS H-MVIP interface, CTCLK need not be frequency locked to CMVFPB.

CMVIDE:

In H-MVIP mode when CMVIDE is set to logic 1, the ingress H-MVIP signals (MVID[1:8], CASID[1:8] and CCSID[1:3]) are updated on the rising edge of CMV8MCLK. When CMVIDE is set to logic 0, the ingress H-MVIP signals are updated on the falling edge of CMV8MCLK.

CMVIFE:

When using the H-MVIP interface, the CMVFPC clock rising edge is in the center of CMVFPB when CMVIFE is set to logic 1. When CMVIFE is set to logic 0, the CMVFPC clock falling edge is in the center of CMVFPB.

CMVFPINV:

When using the H-MVIP interface and CMVFPINV is set to logic 1, the H-MVIP frame pulse, CMVFPB, is inverted. When inverted, CMVFPB is nominally high and pulses low to indicate a frame boundary. When CMVFPINV is a logic 0, CMVFPB is nominally low and pulses high to indicate a frame boundary.

Register 0x000D: Master Clock Monitor

Bit	Type	Function	Default
Bit 7	R	CMVFPA	X
Bit 6	R	CMV8MCLKA	X
Bit 5	R	CTCLKA	X
Bit 4	R	XCLK_E1A	X
Bit 3	R	XCLK_T1A	X
Bit 2		Unused	X
Bit 1	R	LREFCLKA	X
Bit 0	R	SREFCLKA	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set to logic 1. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

SREFCLKA:

The SREFCLK active, SREFCLKA, bit detects low to high transitions on the SREFCLK input. SREFCLKA is set to logic 1 on a rising edge of SREFCLK, and is set to logic 0 when this register is read.

LREFCLKA:

The LREFCLK active, LREFCLKA, bit detects low to high transitions on the LREFCLK input. LREFCLKA is set to logic 1 on a rising edge of LREFCLK, and is set to logic 0 when this register is read.

XCLK_T1A:

The XCLK_T1 active, XCLK_T1A, bit detects for low to high transitions on the XCLK_T1 input. XCLK_T1A is set to logic 1 on a rising edge of XCLK_T1, and is set to logic 0 when this register is read.

XCLK_E1A:

The XCLK_E1 active, XCLK_E1A, bit detects for low to high transitions on the XCLK_E1 input. XCLK_E1A is set to logic 1 on a rising edge of XCLK_E1, and is set to logic 0 when this register is read.

CTCLKA:

The CTCLK active, CTCLKA, bit detects for low to high transitions on the CTCLK input. CTCLKA is set to logic 1 on a rising edge of CTCLK, and is set to logic 0 when this register is read.

CMV8MCLKA:

The C8MVCLK active, C8MVCLKA, bit detects for low to high transitions on the C8MVCLK input. C8MVCLKA is set to logic 1 on a rising edge of C8MVCLK, and is set to logic 0 when this register is read.

CMVFPA:

The CMVFPB active, CMVFPA, bit detects for low to high transitions on the CMVFPB input. CMVFPA is set to logic 1 on a rising edge of CMVFPB, and is set to logic 0 when this register is read.

Register 0x0010: Master Interrupt Source

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	T1E1PRGD	X
Bit 5	R	T1E1INT	X
Bit 4	R	SSBIINT	X
Bit 3	R	LSBIINT	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

LSBIINT:

If the LSBIINT bit is a logic 1, at least one bit in the Master Interrupt Source Line Side SBI Register is set.

SSBIINT:

If the SBIINT bit is a logic 1, at least one bit in the Master Interrupt Source System Interface SBI Register is set.

T1E1INT:

If the T1E1INT bit is a logic 1, at least one bit in the Master Interrupt Source T1E1 Register is set.

T1E1PRGD:

If T1E1PRGD is a logic 1, at least one of the six full featured T1/E1 pattern generators and detectors is generating an interrupt. To clear the interrupt signal, each T1/E1 Pattern Generator and Detector Interrupt Enable/Status register must be read.

Register 0x0011: Master Interrupt Source T1E1

Bit	Type	Function	Default
Bit 7	R	RHDL	X
Bit 6	R	THDL	X
Bit 5	R	RPRBS	X
Bit 4	R	TPRBS	X
Bit 3	R	RXELST	X
Bit 2	R	TXELST	X
Bit 1	R	SIGX	X
Bit 0	R	FRMR	X

FRMR:

If the FRMR bit is a logic 1, an interrupt has been generated by the T1/E1 framer. To clear the interrupt signal, clear all FRMRI[44:29,16:1] bits in the T1/E1 Framer Interrupt Status registers by writing logic 1 to them.

SIGX:

If the SIGX bit is a logic 1, an interrupt has been generated by the T1/E1 signaling extractor caused by a change in signaling state. To clear the interrupt signal, clear all COSSI[44:29,16:1] bits in the Change of Signaling Status registers by writing logic 1 to them.

TXELST:

If the TXELST bit is a logic 1, an interrupt has been generated by the transmit T1/E1 elastic store upon a controlled frame slip. To clear the interrupt signal, read the TX-ELST Slip Status registers.

RXELST:

If the RXELST bit is a logic 1, an interrupt has been generated by either the receive H-MVIP or receive SBI T1/E1 elastic store upon a controlled frame slip. To clear the interrupt signal, read the RX-SBI-ELST and/or the RX-MVIP-ELST Slip Status registers.

TPRBS:

If the TPRBS bit is a logic 1, an interrupt has been generated by an event related to monitoring a PRBS pattern in the transmit direction. To clear the interrupt signal, clear all TPCCI[44:29,16:1] bits in the T1/E1 Framer Interrupt Status registers by writing logic 1 to them.

RPRBS:

If the RPRBS bit is a logic 1, an interrupt has been generated by an event related to monitoring a PRBS pattern in the receive direction. To clear the interrupt signal, clear all RPCCI[44:29,16:1] bits in the RPCC-MVIP Interrupt Status registers and/or RPCC-SBI Interrupt Status registers by writing logic 1 to them.

THDL:

If the THDL bit is a logic 1, an interrupt has been generated by the T1/E1 transmit HDLC processor. To clear the interrupt signal, clear all THDLI[44:29,16:1] bits in the THDL Interrupt Status registers by writing logic 1 to them.

RHDL:

If the RHDL bit is a logic 1, an interrupt has been generated by the T1/E1 receive HDLC processor. To clear the interrupt signal, clear all RHDLI[44:29,16:1] bits in the RHDL Interrupt Status registers by writing logic 1 to them.

Register 0x0012: Master Interrupt Source Line Side SBI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LEXSBIINT	X
Bit 3	R	LINSBIINT	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

LINSBIINT:

If the LINSBIINT bit is a logic 1, the line side INSBI block is generating an interrupt due to a FIFO error. The line side INSBI interrupt registers must be read to clear this interrupt.

LEXSBIINT:

If the LEXSBIINT bit is a logic 1, the line side EXSBI block is generating an interrupt due to a parity or FIFO error. The line side EXSBI interrupt registers must be read to clear this interrupt.

Register 0x0015: Master Interrupt Source System Interface SBI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	SBIDLLINT	X
Bit 5	R	SEXSBIINT	X
Bit 4	R	SINSBIINT	X
Bit 3	R/W	SDET1E	0
Bit 2	R/W	SDET0E	0
Bit 1	R	SDET1INT	X
Bit 0	R	SDET0INT	X

SDET0INT:

This bit only has significance if the S77 input is low.

If the SDET0INT bit is a logic 1, an interrupt has been generated by the SBIDET[0] signal high concurrently with this device driving the System Interface SBI DROP bus. This is an indication that there are multiple devices driving the System Interface SBI DROP bus simultaneously. The TE-32 will not output data when SBIDET[0] is asserted. The SBIDET0 Collision Detect register should be read to determine which tributary was in conflict. This Interrupt register will be cleared when read.

SDET1INT:

This bit only has significance if the S77 input is low.

If the SDET1INT bit is a logic 1, an interrupt has been generated by the SBIDET[1] signal high concurrently with this device driving the System Interface SBI DROP bus. This is an indication that there are multiple devices driving the System Interface SBI DROP bus simultaneously. The TE-32 will not output data when SBIDET[1] is asserted. The SBIDET1 Collision Detect register should be read to determine which tributary was in conflict. This Interrupt register will be cleared when read.

SDET0E:

This bit only has significance if the S77 input is low.

The System Interface SBI DROP activity detect interrupt enable bit, SDET0E, enables interrupts to be generated on INTB when the SBIDET[0] signal is asserted concurrently with this device driving the System Interface SBI DROP bus. When SDET0E is a logic 1, an interrupt will be generated when SBIDET[0] is active with this device driving the System Interface SBI DROP bus. When SBIDET[0] is a logic 0, errors are not generated due to SBIDET[0] concurrent with this device driving the System Interface SBI DROP bus.

SDET1E:

This bit only has significance if the S77 input is low.

The System Interface SBI DROP activity detect interrupt enable bit, SDET1E, enables interrupts to be generated on INTB when the SBIDET[1] signal is asserted concurrently with this device driving the System Interface SBI DROP bus. When SDET1E is a logic 1, an interrupt will be generated when SBIDET[1] is active with this device driving the System Interface SBI DROP bus. When SBIDET[1] is a logic 0, errors are not generated due to SBIDET[1] concurrent with this device driving the System Interface SBI DROP bus.

SINSBIINT:

If the SINSBIINT bit is a logic 1, the System Side INSBI block is generating an interrupt due to a FIFO underrun or overrun. The System Side INSBI interrupt registers must be read to clear this interrupt.

SEXSBIINT:

If the SEXSBIINT bit is a logic 1, the System Side EXSBI block is generating an interrupt due to a parity error, FIFO underrun or overrun. The System Side EXSBI interrupt status registers must be read to clear this interrupt.

SBIDLLINT:

This bit only has significance if the S77 input is pulled high (i.e., the system side SBI is enabled for 77.76 MHz operation). If the SBIDLLINT bit is a logic 1, the SBI DLL has generated an interrupt. Register 0x01C7 DLL Control Status must be read to clear this interrupt.

Register 0x0020: Master SBIDET0 Collision Detect LSB

Bit	Type	Function	Default
Bit 7	R	COL[7]	X
Bit 6	R	COL[6]	X
Bit 5	R	COL[5]	X
Bit 4	R	COL[4]	X
Bit 3	R	COL[3]	X
Bit 2	R	COL[2]	X
Bit 1	R	COL[1]	X
Bit 0	R	COL[0]	X

Register 0x0021: Master SBIDET0 Collision Detect MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COL[8]	X

COL[8:0]:

The SBIDET[0] Collision Detection identifier, COL[8:0], identifies the System Side SBI column number of the last collision as indicated by the SDET0INT interrupt. The tributary experiencing contention is calculated from COL[8:0] as follows:

SPE# = MOD(COL[8:0]-1,3)+1

T1# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),28)+1

E1# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),21)+1

Register 0x0022: Master SBIDET1 Collision Detect LSB

Bit	Type	Function	Default
Bit 7	R	COL[7]	X
Bit 6	R	COL[6]	X
Bit 5	R	COL[5]	X
Bit 4	R	COL[4]	X
Bit 3	R	COL[3]	X
Bit 2	R	COL[2]	X
Bit 1	R	COL[1]	X
Bit 0	R	COL[0]	X

Register 0x0023: Master SBIDET1 Collision Detect MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COL[8]	X

COL[8:0]:

The SBIDET[1] Collision Detection identifier, COL[8:0], identifies the System Side SBI column number of the last collision as indicated by the SDET1INT interrupt.

The tributary experiencing contention is calculated from COL[8:0] as follows:

SPE# = MOD(COL[8:0]-1,3)+1

T1# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),28)+1

E1# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),21)+1

10.2 T1/E1 Master Configuration Registers

Register 0x0040: T1/E1 Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	RX_LKRATE_SEL	0
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	RX_SBI_SIGINS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	EALMEN	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold the T1/E1 framers in a reset condition. When RESET is a logic 1, the entire T1/E1 block will be held in a reset state which is also a low power state. This will force all registers to their default state. While in reset, the clocks can not be guaranteed accurate or existing. When RESET is a logic 0, the T1/E1 framers are in normal operating mode.

EALMEN:

The EALMEN bit enables an egress System Side SBI alarm indication signal to force the transmit data stream into an all ones AIS. When EALMEN is a logic 1 and the System Side SBI bus is selected, the ALM bit set to one in the System Side SBI LinkRate Octet(V4) will force the transmit data to all ones. When EALMEN is a logic 0, ALM bit will not affect the transmit data stream. A logic 1 in the TAISEN bit in the TJAT Indirect Channel Data register forces all ones in the tributary regardless of the state of EALMEN.

The diagnostic loopback point is upstream of this AIS insertion point.

Reserved:

These bits must be logic 0 for correct operation.

RX_SBI_SIGINS:

This bit enables the re-insertion of signaling into the T1 robbed-bit positions. By default, the signaling is extracted and presented in the S-bits. If RX_SBI_SIGINS is a logic 1 and the appropriate per-tributary configuration is done, the signaling is also inserted into the robbed bit positions as determined by the multiframe alignment being communicated across the System Side SBI bus. These robbed bit positions may be different from the positions the signaling was received on. The inserted signaling is subjected to the same trunk conditioning, freezing and debouncing as the S-bits.

For the RX_SBI_SIGINS bit to have effect on a specific tributary, the following must be true: the global PCCE of the RPCC-SBI Configuration Bits register is logic 1, the per-tributary PCCE bit of the RPCC-SBI Indirect Channel Data Registers has been set to logic 1 and the SIGSRC[1:0] bits of the RPCC-SBI Indirect Channel Data Registers are 01 or 10.

RX_LKRATE_SEL:

The Receive Linkrate Select (RX_LKRATE_SEL) bit allows the link rate information to be either passed (unchanged) from the Line Side SBI Drop Bus, or alternatively be re-generated by the RJAT. When RX_LKRATE_SEL is set to logic 0 the linkrate information is generated by the RJAT. Otherwise, if RX_LKRATE_SEL is set to logic 1 the linkrate information is passed unchanged through the RJAT.

Register 0x0042: T1/E1 PRGD #1 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD1SPE[1]	0
Bit 5	R/W	PRGD1SPE[0]	0
Bit 4	R/W	PRGD1LNK[4]	0
Bit 3	R/W	PRGD1LNK[3]	0
Bit 2	R/W	PRGD1LNK[2]	0
Bit 1	R/W	PRGD1LNK[1]	0
Bit 0	R/W	PRGD1LNK[0]	0

PRGD1SPE[1:0], PRGD1LNK[4:0]:

Selects the T1/E1 tributary associated with the first full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD1SPE[1:0] values of 1 to 2 select the SPE from which the tributary is extracted. PRGD1LNK[4:0] values from 1 to 16 select the tributary from one of the 16 T1/E1 tributaries per SPE.

Register 0x0043: T1/E1 PRGD #2 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD2SPE[1]	0
Bit 5	R/W	PRGD2SPE[0]	0
Bit 4	R/W	PRGD2LNK[4]	0
Bit 3	R/W	PRGD2LNK[3]	0
Bit 2	R/W	PRGD2LNK[2]	0
Bit 1	R/W	PRGD2LNK[1]	0
Bit 0	R/W	PRGD2LNK[0]	0

PRGD2SPE[1:0], PRGD2LNK[4:0]:

Selects the T1/E1 tributary associated with the second full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD2SPE[1:0] values of 1 to 2 select the SPE from which the tributary is extracted. PRGD2LNK[4:0] values from 1 to 16 select the tributary from one of the 16 T1/E1 tributaries per SPE.

Register 0x0044: T1/E1 PRGD #3 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD3SPE[1]	0
Bit 5	R/W	PRGD3SPE[0]	0
Bit 4	R/W	PRGD3LNK[4]	0
Bit 3	R/W	PRGD3LNK[3]	0
Bit 2	R/W	PRGD3LNK[2]	0
Bit 1	R/W	PRGD3LNK[1]	0
Bit 0	R/W	PRGD3LNK[0]	0

PRGD3SPE[1:0], PRGD3LNK[4:0]:

Selects the T1/E1 tributary associated with the third full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD3SPE[1:0] values of 1 to 2 select the SPE from which the tributary is extracted. PRGD3LNK[4:0] values from 1 to 16 select the tributary from one of the 16 T1/E1 tributaries per SPE.

Register 0x0045: T1/E1 PRGD #4 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD4SPE[1]	0
Bit 5	R/W	PRGD4SPE[0]	0
Bit 4	R/W	PRGD4LNK[4]	0
Bit 3	R/W	PRGD4LNK[3]	0
Bit 2	R/W	PRGD4LNK[2]	0
Bit 1	R/W	PRGD4LNK[1]	0
Bit 0	R/W	PRGD4LNK[0]	0

PRGD4SPE[1:0], PRGD4LNK[4:0]:

Selects the T1/E1 tributary associated with the fourth full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD4SPE[1:0] values of 1 to 2 select the SPE from which the tributary is extracted. PRGD4LNK[4:0] values from 1 to 16 select the tributary from one of the 16 T1/E1 tributaries per SPE.

Register 0x0046: T1/E1 PRGD #5 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD5SPE[1]	0
Bit 5	R/W	PRGD5SPE[0]	0
Bit 4	R/W	PRGD5LNK[4]	0
Bit 3	R/W	PRGD5LNK[3]	0
Bit 2	R/W	PRGD5LNK[2]	0
Bit 1	R/W	PRGD5LNK[1]	0
Bit 0	R/W	PRGD5LNK[0]	0

PRGD5SPE[1:0], PRGD5LNK[4:0]:

Selects the T1/E1 tributary associated with the fifth full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD5SPE[1:0] values of 1 to 2 select the SPE from which the tributary is extracted. PRGD5LNK[4:0] values from 1 to 16 select the tributary from one of the 16 T1/E1 tributaries per SPE.

Register 0x0047: T1/E1 PRGD #6 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD6SPE[1]	0
Bit 5	R/W	PRGD6SPE[0]	0
Bit 4	R/W	PRGD6LNK[4]	0
Bit 3	R/W	PRGD6LNK[3]	0
Bit 2	R/W	PRGD6LNK[2]	0
Bit 1	R/W	PRGD6LNK[1]	0
Bit 0	R/W	PRGD6LNK[0]	0

PRGD6SPE[1:0], PRGD6LNK[4:0]:

Selects the T1/E1 tributary associated with the sixth full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD6SPE[1:0] values of 1 to 2 select the SPE from which the tributary is extracted. PRGD6LNK[4:0] values from 1 to 16 select the tributary from one of the 16 T1/E1 tributaries per SPE.

10.3 T1/E1 Receive Jitter Attenuator (RJAT) Registers

Register 0x0048: RJAT Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RJAT Indirect Channel Data register. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RJAT Indirect Channel Data register.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RJAT Indirect Channel Data register or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0049: RJAT Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RJAT channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x004A: RJAT Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	DLOOP	0
Bit 2	R/W	Unused	0
Bit 1	R/W	TXPMON	0
Bit 0	R/W	RJATBYP	0

This register contains data read from the RJAT channel context RAM after an indirect read operation or data to be inserted into the RJAT channel context RAM in an indirect write operation.

The bits to be written to the RJAT channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Regardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

RJATBYP:

The RJATBYP bit disables jitter attenuation in the receive direction. When receive jitter attenuation is not being used, setting RJATBYP to logic 1 will reduce the latency through the receiver section by typically 40 bits.

TXPMON:

TXPMON can be used for unchannelized tributaries. When TXPMON is logic 1, performance monitoring is performed on the egress tributary. Performance monitoring includes maintenance of all T1/E1 framer counts and statuses plus HDLC termination. When TXPMON is logic 0, performance monitoring is performed on the ingress tributary.

DLOOP:

The DLOOP bit selects the T1/E1 diagnostic loopback, where the tributary is configured to internally direct the output of the TJAT to the input of the RJAT. When DLOOP is set to logic 1, the diagnostic loopback mode is enabled. When DLOOP is set to logic 0, the diagnostic loopback mode is disabled. The TJATBYP context bit can be used to bypass the egress jitter attenuator FIFO to decrease latency.

Reserved:

These bits must be logic 0 for correct operation.

Register 0x004B: RJAT Programmable Corner Frequency Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	M [2]	1
Bit 1	R/W	M [1]	0
Bit 0	R/W	M [0]	0

M[2:0]:

This register is used to program the corner frequency of the receive T1/E1 jitter attenuator. M[2:0] can be used to select one of eight possible corner frequencies as follows:

M[2:0]	T1	E1
000	18.0 Hz	25.0 Hz
001	9.0 Hz	12.0 Hz
010	6.0 Hz	8.0 Hz
011	4.4 Hz	6.0 Hz
100	3.4 Hz (default)	5.0 Hz (default)
101	3.0 Hz	4.0 Hz
110	2.5 Hz	3.3 Hz
111	2.1 Hz	3.0 Hz

10.4 T1/E1 Transmit Jitter Attenuator (TJAT) Registers

Register 0x004C: TJAT Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the TJAT Indirect Channel Data register. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the TJAT Indirect Channel Data register.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the TJAT Indirect Channel Data register or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x004D: TJAT Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the TJAT channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x004E: TJAT Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	REFSEL	0
Bit 5	R/W	LOOPT	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LLOOP	0
Bit 2	R/W	Unused	0
Bit 1	R/W	TAISEN	0
Bit 0	R/W	TJATBYP	0

This register contains data read from the TJAT channel context RAM after an indirect read operation or data to be inserted into the TJAT channel context RAM in an indirect write operation.

The bits to be written to the TJAT channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Regardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

TJATBYP:

The TJATBYP bit bypasses the transmit jitter attention FIFO. Although setting TJATBYP has the effect of reducing latency, it also has the side effect of reducing jitter tolerance at the system interface. Jitter attenuation should be used when additional jitter attenuation is required on the external transmit reference clock or when in clock slave mode and the data needs jitter attenuation.

Note: The transmit jitter attenuator may be used to generate a transmit clock for clock master applications and when using the transmit elastic store even if TJATBYP is logic 1.

TAISEN:

The TAISEN bit enables generation of an all ones AIS alarm in the egress tributary. When TAISEN is a logic 1 the egress data stream is forced to all ones. When TAISEN is a logic 0 the egress tributary operates normally. The diagnostic loopback point is upstream of this AIS insertion point.

LLOOP:

The LLOOP bit selects the line loopback mode, where the recovered data are internally directed to back to the line side SBI Interface. When LLOOP is set to logic 1, the line loopback mode is enabled. When LLOOP is set to logic 0, the line loopback mode is disabled.

When LLOOP is logic 1, the RJATBYP bit for the tributary must be logic 0.

Reserved:

This bit must be logic 0 for correct operation.

LOOPT, REFSEL:

The LOOPT context bit is used to enable loop-timing. The REFSEL input determines the reference for the egress data rate. If LLOOP is logic 1, the transmit data is automatically loop-timed.

LOOPT	REFSEL	Description
0	0	Transmit data locked to egress data rate at the SBI Add bus system interface. Legal only if transmit elastic store is bypassed. Cannot be used when SYSOPT[1:0] register bits are binary 01 or 11.
0	1	Transmit data locked to CTCLK or recovered clock selected by the REFCLK[1:0] bits of the Reference Clock Select register.
1	0	Transmit data locked to ingress recovered clock for the tributary.
1	1	Reserved.

Register 0x004F: TJAT Programmable Corner Frequency Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	M [2]	1
Bit 1	R/W	M [1]	0
Bit 0	R/W	M [0]	0

M[2:0]:

This register is used to program the corner frequency of the transmit T1/E1 jitter attenuator. M[2:0] can be used to select one of eight possible corner frequencies as follows:

M[2:0]	T1	E1
000	18.0 Hz	25.0 Hz
001	9.0 Hz	12.0 Hz
010	6.0 Hz	8.0 Hz
011	4.4 Hz	6.0 Hz
100	3.4 Hz (default)	5.0 Hz (default)
101	3.0 Hz	4.0 Hz
110	2.5 Hz	3.3 Hz
111	2.1 Hz	3.0 Hz

10.5 T1/E1 Receive H-MVIP Per-Channel Controller (RPCC) Registers

Register 0x0050: RPCC-MVIP Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers an indirect channel register access to the Receive Per-Channel Controller (RPCC-MVIP) context RAM.

TSADDR[4:0]:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RPCC-MVIP Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RPCC-MVIP Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RPCC-MVIP Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0051: RPCC-MVIP Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RPCC-MVIP context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.
CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Registers 0x0052-0x0056: RPCC-MVIP Indirect Channel Data Registers

These registers contain data read from the RPCC-MVIP channel context RAM after an indirect read operation or data to be inserted into the RPCC-MVIP channel context RAM in an indirect write operation.

The bits to be written to the RPCC-MVIP channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All three registers from 0x0052 through 0x0054 inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the RPCC-MVIP Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

TSACCESS=0:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0052	RPRBSLEN[2:0]			RPRBS UNF	MDTRK	MSTRK	PCCE	Unused	00000000
0x0053	T56K PRBS	TPRBS INV	TPRBSLEN[2:0]			TPRBS UNF	R56K PRBS	RPRBS INV	00000000
0x0054	PRBSERR[2:0]			PSYNCI	PSYNC	Reserved	PSYNCE	INV LAST	XXXXXX00
0x0055	PRBSERR[10:3]								XXXXXXXX
0x0056	Unused			PRBSERR[15:11]					XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0052	SIGSR C	INV[1:0]		ALAW	DMW	IDLC	ZCS[1:0]		00000000
0x0053	IDLE[2:0]			A’	B’	C’	D’	Reserved	000000000
0x0054	Unused	TPRBS	RPRBS	IDLE[7:3]					XX000000
0x0055	Unused								XXXXXXXX
0x0056	Unused								XXXXXXXX

In the following bit descriptions, the system interface refers to the Ingress H-MVIP Interface. Be aware that the PRBS receiver documented is down stream of the frame slip buffer; therefore, controlled slips will corrupt the bit sequence and result in bit errors and momentary loss of synchronization.

PCCE:

The per-tributary configuration enable bit, PCCE, enables the configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, it enables the both the TSACCESS=0 and TSACCESS=1 Configuration bits. The global PCCE bit of the RPCC-MVIP Configuration Bits register must also be logic 1 for this bit to have effect.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

MSTRK:

Master Signaling Trunk Conditioning. When this bit is logic 1, signaling substitution at the system interface (CASID output) is performed on all channels/time slots for a tributary. Setting MSTRK is equivalent to setting the SIGSRC bit to logic 1 for all channels/timeslots.

MDTRK:

Master Data Trunk Conditioning. When this bit is logic 1, idle code substitution at the system interface (MVID output) is performed on all channels/time slots for a tributary. For E1, this includes overwriting TS0 with its IDLE[7:0] bits. For T1, the F-bit is not altered. Setting MDTRK is equivalent to setting the IDLC Per-Channel context bit to logic 1 for all channels/timeslots.

RPRBSUNF:

If this bit is logic 1, the PRBS is expected to fill all bits in the tributary data stream received from the line side. This bit supercedes the Per-Channel RPRBS context bits and the R56KPRBS context bits. The T1 F-bit is excluded from the pattern, so setting RPRSBUNF is equivalent to setting all 24 RPRBS per-channel bits. For E1, the PRBS pattern fills all bit positions.

RPRBSLEN[2:0]:

The Receive PRBS Length field determines the sequence length of the expected bit pattern received from line side:

RPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

RPRBSINV:

If this bit is logic 1, the logical polarity of the received PRBS is inverted before comparison.

R56KPRBS:

If this bit is logic 1, the PRBS is expected to fill only the first seven bits of the selected channels/time slots. Otherwise, the PRBS is expected to occupy the entire selected channels/time slots.

TPRBSUNF:

If this bit is logic 1, the PRBS fills all bits of the tributary at the system interface (H-MVIP MVID output). This bit supercedes the Per-Channel TPRBS context bits and the T56KPRBS context bits. The T1 F-bit is excluded from the pattern, so setting TPRSBUNF is equivalent to setting all 24 TPRBS per-channel bits. For E1, the PRBS pattern fills all bit positions.

TPRBSLEN[2:0]:

The Transit PRBS Length field determines the sequence length of the generated bit pattern destined for the H-MVIP output:

TPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

TPRBSINV:

If this bit is logic 1, the logical polarity of the generated PRBS is inverted before transmission.

T56KPRBS

If this bit is logic 1, the generated PRBS fills only the first seven bits of the selected channels/time slots. Otherwise, the PRBS occupies the entire selected channels/time slots.

INVLAST:

If this bit is logic 1, inversion (as controlled by the INV[1:0] Per-Channel context bits) is the last per-channel operation performed on the data. Otherwise, inversion is the first operation performed.

PSYNCE:

If this bit is a logic 1, the associated RPCCI[x] bit is set upon a change in the PSYNC context bit.

PSYNC:

PSYNC is the PRBS synchronization status. PSYNC becomes a logic 1 if the received data matched the expected sequence for the latest four bytes. PSYNC is set to logic 0 only if 3 consecutive bytes are in error.

PSYNCI:

PSYNCI becomes a logic 1 upon a change in the PSYNC context bit. It is cleared upon an indirect read access.

PRBSERR[15:0]:

The PRBS Error holding register contains a count of the discrepancies between the expected PRBS sequence and the receive data that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1. The count saturates at all ones.

ZCS[1:0]:

These bits control the Zero Code Suppression on the MVID output as follows:

T1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	GTE Zero Code Suppression. The least significant bit (bit 8) of an all zeros channel is forced to a one, except for signaling frames where the second least significant bit is forced to a one.
10	DDS Zero Code Suppression. All zero channel data is replaced with the pattern "10011000"
11	Bell Zero Code Suppression. The second least significant bit (bit 7) of an all zeros channel is forced to a one.

E1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	Jammed bit-8. The least significant bit (bit 8) of an all zeros channel is forced to a one.
10	No Zero Code Suppression
11	Jammed bit-8.

Zero code suppression occurs after data inversion, idle code insertion, digital milliwatt insertion and signaling have occurred.

IDLC:

If this bit is logic 1, the channel/time slot data at the system interface (MVID output) is replaced by the value in the IDLE[7:0] field.

DMW:

If this bit is logic 1, the channel/time slot data at the system interface (MVID output) is replaced by the Digital Milliwatt signal. The encoding of the 1 kHz sine wave is determined by the ALAW context bit.

ALAW:

This bit determines the encoding of the Digital Milliwatt signal. If ALAW is logic 0, μ-law companding is respected. If ALAW is logic 1, A-law companding is respected.

INV[1:0]:

These bits invert the channel/time slot data on the MVID output:

INV[1:0]	T1 Description	E1 Description
00	No inversion (default)	No inversion (default)
01	Only the MSB of the received PCM channel data is inverted (Sign bit inversion)	Invert even bits
10	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)	Invert odd bits
11	Invert all bits	Invert all bits

SIGSRC:

This bit determines the source of signaling presented at the system interface (CASID output). If SIGSRC is logic 1, the signaling is taken from the A',B',C',D' bits. If SIGSRC is logic 0, received signaling is passed through to the system interface (subject to debouncing and bit fixing).

Reserved:

This bit must be logic 0 for correct operation.

A',B',C',D':

These signaling bits are inserted at the system interface (CASID output) when the MSTRK bit is logic 1 or if the SIGSRC bit is logic 1. For the T1 SF frame format, C' and D' must equal A' and B', respectively.

IDLE[7:0]:

This field contains the value inserted at the system interface (MVID output) if the MDTRK or IDLC bit is logic 1.

RPRBS:

If this bit is logic 1, a PRBS is expected in the channel/time slot received from the line side.

TPRBS:

If this bit is logic 1, a PRBS is generated in the channel/time slot destined for the H-MVIP output, MVID.

Register 0x0057: RPCC-MVIP Configuration Bits

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	INTE	0
Bit 3	R/W	Reserved	0
Bit 2	W12C	XFERI	X
Bit 1	R/W	XFERE	0
Bit 0	R/W	PCCE	0

INTE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the RPCCI[44:29,16:1] bits is a logic 1.

Reserved:

This bit must be logic 0 for correct operation.

XFERI:

The XFERI bit indicates that a transfer of accumulated PRBS error data has occurred. A logic 1 in this bit position indicates that the holding registers have been updated. This update is initiated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1.

Logic 1 must be written to this bit to clear it to logic 0.

XFERE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

PCCE:

This global bit enables RPCC-MVIP per-channel/per-timeslot functions if logic 1. The per-tributary PCCE bits set through the RPCC-MVIP Indirect Channel Data Registers must also be set to enable individual tributaries.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

Register 0x0058: RPCC-MVIP Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REGC_DI	X
Bit 4	R	REG9_AI	X
Bit 3	W12C	RPCCI[4]	X
Bit 2	W12C	RPCCI[3]	X
Bit 1	W12C	RPCCI[2]	X
Bit 0	W12C	RPCCI[1]	X

RPCCI[44:29,16:1]:

A logic 1 in these bits indicate a change of PRBS synchronization state on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG9_AI:

This bit is a logic 1 if at least one bit in Register 0x0059 or 0x005A is logic 1.

REGC_DI:

This bit is a logic 1 if at least one bit in Register 0x005C or 0x005D is logic 1.

Register 0x0059: RPCC-MVIP Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[12]	X
Bit 6	W12C	RPCCI[11]	X
Bit 5	W12C	RPCCI[10]	X
Bit 4	W12C	RPCCI[9]	X
Bit 3	W12C	RPCCI[8]	X
Bit 2	W12C	RPCCI[7]	X
Bit 1	W12C	RPCCI[6]	X
Bit 0	W12C	RPCCI[5]	X

Register 0x005A: RPCC-MVIP Interrupt Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	W12C	RPCCI[16]	X
Bit 2	W12C	RPCCI[15]	X
Bit 1	W12C	RPCCI[14]	X
Bit 0	W12C	RPCCI[13]	X

Register 0x005C: RPCC-MVIP Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[36]	X
Bit 6	W12C	RPCCI[35]	X
Bit 5	W12C	RPCCI[34]	X
Bit 4	W12C	RPCCI[33]	X
Bit 3	W12C	RPCCI[32]	X
Bit 2	W12C	RPCCI[31]	X
Bit 1	W12C	RPCCI[30]	X
Bit 0	W12C	RPCCI[29]	X

Register 0x005D: RPCC-MVIP Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[44]	X
Bit 6	W12C	RPCCI[43]	X
Bit 5	W12C	RPCCI[42]	X
Bit 4	W12C	RPCCI[41]	X
Bit 3	W12C	RPCCI[40]	X
Bit 2	W12C	RPCCI[39]	X
Bit 1	W12C	RPCCI[38]	X
Bit 0	W12C	RPCCI[37]	X

Register 0x0063: RPCC-MVIP PRBS Error Insertion

Bit	Type	Function	Default
Bit 7	R/W	TPRBS_ERR_INSERT	X
Bit 6	R/W	TPRBS_ADDR[6]	X
Bit 5	R/W	TPRBS_ADDR[5]	X
Bit 4	R/W	TPRBS_ADDR[4]	X
Bit 3	R/W	TPRBS_ADDR[3]	X
Bit 2	R/W	TPRBS_ADDR[2]	X
Bit 1	R/W	TPRBS_ADDR[1]	X
Bit 0	R/W	TPRBS_ADDR[0]	X

TPRBS_ERR_INSERT:

The TPRBS Error insertion Enable bit causes a single bit error to be inserted in the PRBS pattern for the tributary addressed by TPRBS_ADDR[6:0]. A zero to one transition triggers the error insertion.

TPRBS_ADDR[6:0]:

Indicates the tributary into which a single bit error is to be inserted. TPRBS_ADDR[6:5] is the SPE index and ranges from 1 to 2. TPRBS_ADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x0064: RPCC-MVIP PRBS Error Insert Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	W12C	TPRBS_ERR_INSERTED	X

TPRBS_ERR_INSERTED:

TPRBS_ERR_INSERTED indicates an error has been inserted. This bit is cleared to logic 0 upon writing a logic 1 to the bit position.

10.6 T1/E1 Receive SBI Per-Channel Controller (RPCC-SBI) Registers

Register 0x0068: RPCC-SBI Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers an indirect channel register access to the Receive Per-Channel Controller (RPCC-SBI) context RAM.

TSADDR[4:0]:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RPCC-SBI Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RPCC-SBI Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RPCC-SBI Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0069: RPCC-SBI Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RPCC-SBI context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.
CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Registers 0x006A-0x006E: RPCC-SBI Indirect Channel Data Registers

These registers contain data read from the RPCC-SBI channel context RAM after an indirect read operation or data to be inserted into the RPCC-SBI channel context RAM in an indirect write operation.

The bits to be written to the RPCC-SBI channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All three registers from 0x006A through 0x006C inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the RPCC-SBI Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

TSACCESS=0:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x006A	RPRBSLEN[2:0]			RPRBS UNF	MDTRK	MSTRK	PCCE	Unused	00000000
0x006B	T56K PRBS	TPRBS INV	TPRBSLEN[2:0]			TPRBS UNF	R56K PRBS	RPRBS INV	00000000
0x006C	PRBSERR[2:0]			PSYNCI	PSYNC	Reserved	PSYNCE	INV LAST	XXXXXX00
0x006D	PRBSERR[10:3]								XXXXXXXX
0x006E	Unused			PRBSERR[15:11]					XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x006A	SIGSRC [0]	INV[1:0]		ALAW	DMW	IDLC	ZCS[1:0]		00000000
0x006B	IDLE[2:0]			A’	B’	C’	D’	SIGSRC [1]	000000000
0x006C	Unused	TPRBS	RPRBS	IDLE[7:3]					XX000000
0x006D	Unused								XXXXXXXX
0x006E	Unused								XXXXXXXX

In the following bit descriptions, the system interface refers to the SBI Drop bus. Be aware that the PRBS receiver documented is down stream of the frame slip buffer; therefore, controlled slips will corrupt the bit sequence and result in bit errors and momentary loss of synchronization.

PCCE:

The per-tributary configuration enable bit, PCCE, enables the configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, it enables the both the TSACCESS=0 and TSACCESS=1 Configuration bits. The global PCCE bit of the RPCC-SBI Configuration Bits register must also be logic 1 for this bit to have effect.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

The PCCE context bit must be logic 0 if the tributary is not being used.

MSTRK:

Master Signaling Trunk Conditioning. When this bit is logic 1, signaling substitution at the system interface is performed on all channels/time slots for a tributary. Setting MSTRK is equivalent to setting the SIGSRC[1:0] bits to binary 01 for all channels/timeslots.

MDTRK:

Master Data Trunk Conditioning. When this bit is logic 1, idle code substitution at the system interface is performed on all channels/time slots for a tributary. For E1, this includes overwriting TS0 with its IDLE[7:0] bits. For T1, the F-bit is not altered. Setting MDTRK is equivalent to setting the IDLC Per-Channel context bit to logic 1 for all channels/timeslots.

RPRBSUNF:

If this bit is logic 1, the PRBS is expected to fill all bits in the tributary data stream received from the line side. This bit supercedes the Per-Channel RPRBS context bits and the R56KPRBS context bits.

RPRBSLEN[2:0]:

The Receive PRBS Length field determines the sequence length of the expected bit pattern received from the line side:

RPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

RPRBSINV:

If this bit is logic 1, the logical polarity of the received PRBS is inverted before comparison.

R56KPRBS:

If this bit is logic 1, the PRBS is expected to fill only the first seven bits of the selected channels/time slots. Otherwise, the PRBS is expected to occupy the entire selected channels/time slots.

TPRBSUNF:

If this bit is logic 1, the PRBS fills all bits of the tributary at the system interface (SBI Drop bus). This bit supercedes the Per-Channel TPRBS context bits and the T56KPRBS context bits.

TPRBSLEN[2:0]:

The Transit PRBS Length field determines the sequence length of the generated bit pattern destined to the System Side SBI Drop bus:

TPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

TPRBSINV:

If this bit is logic 1, the logical polarity of the generated PRBS is inverted before transmission.

T56KPRBS

If this bit is logic 1, the generated PRBS fills only the first seven bits of the selected channels/time slots. Otherwise, the PRBS occupies the entire selected channels/time slots.

INVLAST:

If this bit is logic 1, inversion (as controlled by the INV[1:0] Per-Channel context bits) is the last per-channel operation performed on the data. Otherwise, inversion is the first operation performed.

PSYNCE:

If this bit is a logic 1, the associated RPCCI[x] bit is set upon a change in the PSYNC context bit.

PSYNC:

PSYNC is the PRBS synchronization status. PSYNC becomes a logic 1 if the received data matched the expected sequence for the latest four bytes. PSYNC is set to logic 0 only if 3 consecutive bytes are in error.

PSYNCI:

PSYNCI becomes a logic 1 upon a change in the PSYNC context bit. It is cleared upon an indirect read access.

PRBSERR[15:0]:

The PRBS Error holding register contains a count of the discrepancies between the expected PRBS sequence and the receive data that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1. The count saturates at all ones.

ZCS[1:0]:

These bits control the Zero Code Suppression on the System side SBI Drop bus as follows:

T1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	GTE Zero Code Suppression. The least significant bit (bit 8) of an all zeros channel is forced to a one, except for signaling frames where the second least significant bit is forced to a one.
10	DDS Zero Code Suppression. All zero channel data is replaced with the pattern "10011000"
11	Bell Zero Code Suppression. The second least significant bit (bit 7) of an all zeros channel is forced to a one.

E1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	Jammed bit-8. The least significant bit (bit 8) of an all zeros channel is forced to a one.
10	No Zero Code Suppression
11	Jammed bit-8.

Zero code suppression occurs after data inversion, idle code insertion, digital milliwatt insertion and signaling have occurred.

IDLC:

If this bit is logic 1, the channel/time slot data at the system interface is replaced by the value in the IDLE[7:0] field.

DMW:

If this bit is logic 1, the channel/time slot data at the system interface is replaced by the Digital Milliwatt signal. The encoding of the 1 kHz sine wave is determined by the ALAW context bit.

ALAW:

This bit determines the encoding of the Digital Milliwatt signal. If ALAW is logic 0, μ-law companding is respected. If ALAW is logic 1, A-law companding is respected.

INV[1:0]:

These bits invert the channel/time slot data:

INV[1:0]	T1 Description	E1 Description
00	No inversion (default)	No inversion (default)
01	Only the MSB of the received PCM channel data is inverted (Sign bit inversion)	Invert even bits
10	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)	Invert odd bits
11	Invert all bits	Invert all bits

SIGSRC[1:0]:

These bits determine the source of signaling presented at the SBI Drop system interface. If SIGSRC[0] is logic 1, the signaling is taken from the A',B',C',D' bits. If SIGSRC[0] is logic 0, received signaling is passed through to the system interface (subject to debouncing and bit fixing).

SIGSRC[1:0]	Description
00	Extracted signaling is only presented in the "SSSS" bits of the SBI Drop bus.
01	Signaling taken from A', B', C' and D' context bits. May be presented in the robbed bits if the RX_SBI_SIGINS bit of the T1/E1 Master Configuration register is logic 1.
10	Extracted signaling presented in the "SSSS" bits of the SBI Drop bus plus the robbed bits if the RX_SBI_SIGINS bit of the T1/E1 Master Configuration register is logic 1.
11	Reserved.

Reserved:

This bit must be logic 0 for correct operation.

A',B',C',D':

These signaling bits are inserted at the system interface when the MSTRK bit is logic 1 or if the SIGSRC[0] bit is logic 1. For the T1 SF frame format, C' and D' must equal A' and B', respectively.

IDLE[7:0]:

This field contains the value inserted at the system interface if the MDTRK or IDLC bit is logic 1.

RPRBS:

If this bit is logic 1, a PRBS is expected in the channel/time slot received from the line side.

TPRBS:

If this bit is logic 1, a PRBS is generated in the channel/time slot destined to the System Interface SBI Drop bus..

Register 0x006F: RPCC-SBI Configuration Bits

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	INTE	0
Bit 3	R/W	Reserved	0
Bit 2	W12C	XFERI	X
Bit 1	R/W	XFERE	0
Bit 0	R/W	PCCE	0

INTE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the RPCCI[44:29,16:1] bits is a logic 1.

Reserved:

This bit must be logic 0 for correct operation.

XFERI:

The XFERI bit indicates that a transfer of accumulated PRBS error data has occurred. A logic 1 in this bit position indicates that the holding registers have been updated. This update is initiated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1.

Logic 1 must be written to this bit to clear it to logic 0.

XFERE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

PCCE:

This global bit enables RPCC-SBI per-channel/per-timeslot functions if logic 1. The per-tributary PCCE bits set through the RPCC-SBI Indirect Channel Data Registers must also be set to enable individual tributaries.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

Register 0x0070: RPCC-SBI Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REG4_5I	X
Bit 4	R	REG1_2I	X
Bit 3	W12C	RPCCI[4]	X
Bit 2	W12C	RPCCI[3]	X
Bit 1	W12C	RPCCI[2]	X
Bit 0	W12C	RPCCI[1]	X

RPCCI[44:29,16:1]:

A logic 1 in these bits indicate a change of PRBS synchronization state on the associated tributary since this register was last read. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG1_2I:

This bit is a logic 1 if at least one bit in Register 0x0071 or 0x0072 is logic 1.

REG4_5I:

This bit is a logic 1 if at least one bit in Register 0x0074 or 0x0075 is logic 1.

Register 0x0071: RPCC-SBI Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[12]	X
Bit 6	W12C	RPCCI[11]	X
Bit 5	W12C	RPCCI[10]	X
Bit 4	W12C	RPCCI[9]	X
Bit 3	W12C	RPCCI[8]	X
Bit 2	W12C	RPCCI[7]	X
Bit 1	W12C	RPCCI[6]	X
Bit 0	W12C	RPCCI[5]	X

Register 0x0072: RPCC-SBI Interrupt Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	W12C	RPCCI[16]	X
Bit 2	W12C	RPCCI[15]	X
Bit 1	W12C	RPCCI[14]	X
Bit 0	W12C	RPCCI[13]	X

Register 0x0074: RPCC-SBI Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[36]	X
Bit 6	W12C	RPCCI[35]	X
Bit 5	W12C	RPCCI[34]	X
Bit 4	W12C	RPCCI[33]	X
Bit 3	W12C	RPCCI[32]	X
Bit 2	W12C	RPCCI[31]	X
Bit 1	W12C	RPCCI[30]	X
Bit 0	W12C	RPCCI[29]	X

Register 0x0075: RPCC-SBI Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[44]	X
Bit 6	W12C	RPCCI[43]	X
Bit 5	W12C	RPCCI[42]	X
Bit 4	W12C	RPCCI[41]	X
Bit 3	W12C	RPCCI[40]	X
Bit 2	W12C	RPCCI[39]	X
Bit 1	W12C	RPCCI[38]	X
Bit 0	W12C	RPCCI[37]	X

Register 0x007B: RPCC-SBI PRBS Error Insertion

Bit	Type	Function	Default
Bit 7	R/W	TPRBS_ERR_INSERT	X
Bit 6	R/W	TPRBS_ADDR[6]	X
Bit 5	R/W	TPRBS_ADDR[5]	X
Bit 4	R/W	TPRBS_ADDR[4]	X
Bit 3	R/W	TPRBS_ADDR[3]	X
Bit 2	R/W	TPRBS_ADDR[2]	X
Bit 1	R/W	TPRBS_ADDR[1]	X
Bit 0	R/W	TPRBS_ADDR[0]	X

TPRBS_ERR_INSERT:

The TPRBS Error insertion Enable bit causes a single bit error to be inserted in the PRBS pattern for the tributary addressed by TPRBS_ADDR[6:0]. A zero to one transition triggers the error insertion.

TPRBS_ADDR[6:0]:

Indicates the tributary into which a single bit error is to be inserted. TPRBS_ADDR[6:5] is the SPE index and ranges from 1 to 2. TPRBS_ADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x007C: RPCC-SBI PRBS Error Insert Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	W12C	TPRBS_ERR_INSERTED	X

TPRBS_ERR_INSERTED:

TPRBS_ERR_INSERTED indicates an error has been inserted. This bit is cleared to logic 0 upon writing a logic 1 to the bit position.

10.7 T1/E1 Receive H-MVIP Elastic Store (RX-MVIP-ELST) Registers

Register 0x0083: RX-MVIP-ELST Idle Code

Bit	Type	Function	Default
Bit 7	R/W	IDLECODE[7]	1
Bit 6	R/W	IDLECODE[6]	1
Bit 5	R/W	IDLECODE[5]	1
Bit 4	R/W	IDLECODE[4]	1
Bit 3	R/W	IDLECODE[3]	1
Bit 2	R/W	IDLECODE[2]	1
Bit 1	R/W	IDLECODE[1]	1
Bit 0	R/W	IDLECODE[0]	1

IDLECODE[7:0]:

The contents of this register are inserted into each DS0 of tributaries that are out of basic frame alignment (i.e. T1/E1 FRMR INF context bit is logic 0) and the TRKEN T1/E1 FRMR context bit is logic 1.

Register 0x0084: RX-MVIP-ELST Slip Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REG8_9I	X
Bit 4	R	REG5_6I	X
Bit 3	W12C	SLPI[4]	X
Bit 2	W12C	SLPI[3]	X
Bit 1	W12C	SLPI[2]	X
Bit 0	W12C	SLPI[1]	X

SLPI[44:29,16:1]:

A logic 1 in these bits indicate a slip has occurred on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG5_6I:

This bit is a logic 1 if at least one bit in Register 0x0085 or 0x0086 is logic 1.

REG8_9I:

This bit is a logic 1 if at least one bit in Register 0x0088 or 0x0089 is logic 1.

Register 0x0085: RX-MVIP-ELST Slip Status #2

Bit	Type	Function	Default
Bit 7	W12C	SLPI[12]	X
Bit 6	W12C	SLPI[11]	X
Bit 5	W12C	SLPI[10]	X
Bit 4	W12C	SLPI[9]	X
Bit 3	W12C	SLPI[8]	X
Bit 2	W12C	SLPI[7]	X
Bit 1	W12C	SLPI[6]	X
Bit 0	W12C	SLPI[5]	X

Register 0x0086: RX-MVIP-ELST Slip Status #3

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	SLPI[16]	X
Bit 2	W12C	SLPI[15]	X
Bit 1	W12C	SLPI[14]	X
Bit 0	W12C	SLPI[13]	X

Register 0x0087: RX-MVIP-ELST Reserved

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	Reserved	X
Bit 2	W12C	Reserved	X
Bit 1	W12C	Reserved	X
Bit 0	W12C	Reserved	X

Reserved:

In order to prevent the SLPI[44:29,16:1] interrupts being blocked, these bits must be cleared once the device has been initialized. Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

Register 0x0088: RX-MVIP-ELST Slip Status #4

Bit	Type	Function	Default
Bit 7	W12C	SLPI[36]	X
Bit 6	W12C	SLPI[35]	X
Bit 5	W12C	SLPI[34]	X
Bit 4	W12C	SLPI[33]	X
Bit 3	W12C	SLPI[32]	X
Bit 2	W12C	SLPI[31]	X
Bit 1	W12C	SLPI[30]	X
Bit 0	W12C	SLPI[29]	X

Register 0x0089: RX-MVIP-ELST Slip Status #5

Bit	Type	Function	Default
Bit 7	W12C	SLPI[44]	X
Bit 6	W12C	SLPI[43]	X
Bit 5	W12C	SLPI[42]	X
Bit 4	W12C	SLPI[41]	X
Bit 3	W12C	SLPI[40]	X
Bit 2	W12C	SLPI[39]	X
Bit 1	W12C	SLPI[38]	X
Bit 0	W12C	SLPI[37]	X

Register 0x008A-0x008E: RX-MVIP-ELST Reserved

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	Reserved	X
Bit 2	W12C	Reserved	X
Bit 1	W12C	Reserved	X
Bit 0	W12C	Reserved	X

Reserved:

In order to prevent the SLPI[44:29,16:1] interrupts being blocked, these bits must be cleared once the device has been initialized. Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

Register 0x008F: RX-MVIP-ELST Slip Direction #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[4]	X
Bit 2	R	SLPD[3]	X
Bit 1	R	SLPD[2]	X
Bit 0	R	SLPD[1]	X

SLPD[44:29,16:1]:

A logic 1 in these bits indicate the direction of latest slip on the associated tributary. If SLPD[x] is a logic 0, the slip resulted in the repetition of a frame. If SLPD[x] is a logic 1, a frame was lost. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Register 0x0090: RX-MVIP-ELST Slip Direction #2

Bit	Type	Function	Default
Bit 7	R	SLPD[12]	X
Bit 6	R	SLPD[11]	X
Bit 5	R	SLPD[10]	X
Bit 4	R	SLPD[9]	X
Bit 3	R	SLPD[8]	X
Bit 2	R	SLPD[7]	X
Bit 1	R	SLPD[6]	X
Bit 0	R	SLPD[5]	X

Register 0x0091: RX-MVIP-ELST Slip Direction #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[16]	X
Bit 2	R	SLPD[15]	X
Bit 1	R	SLPD[14]	X
Bit 0	R	SLPD[13]	X

Register 0x0093: RX-MVIP-ELST Slip Direction #4

Bit	Type	Function	Default
Bit 7	R	SLPD[36]	X
Bit 6	R	SLPD[35]	X
Bit 5	R	SLPD[34]	X
Bit 4	R	SLPD[33]	X
Bit 3	R	SLPD[32]	X
Bit 2	R	SLPD[31]	X
Bit 1	R	SLPD[30]	X
Bit 0	R	SLPD[29]	X

Register 0x0094: RX-MVIP-ELST Slip Direction #5

Bit	Type	Function	Default
Bit 7	R	SLPD[44]	X
Bit 6	R	SLPD[43]	X
Bit 5	R	SLPD[42]	X
Bit 4	R	SLPD[41]	X
Bit 3	R	SLPD[40]	X
Bit 2	R	SLPD[39]	X
Bit 1	R	SLPD[38]	X
Bit 0	R	SLPD[37]	X

Register 0x009A: RX-MVIP-ELST Slip Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SLPE	0

SLPE:

If this bit is a logic 1, the RXELST bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the SLPI[44:29,16:1] bits is a logic 1.

10.8 T1/E1 Receive SBI Elastic Store (RX-SBI-ELST) Registers

Register 0x00A0: RX-SBI-ELST Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access to the receive SBI elastic store (RX-SBI-ELST) context RAM.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RX-SBI-ELST Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RX-SBI-ELST Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RX-SBI-ELST Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x00A1: RX-SBI-ELST Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RX-SBI-ELST channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x00A2: RX-SBI-ELST Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	SYNCSBI	0
Bit 0	R/W	ELSTBYP	0

This register contains data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Regardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

SYNCSBI:

The Synchronous SBI bit enables the T1/E1 framer to reference the output timing of its elastic store to the SBI bus clock, SREFCLK. When SYNCSBI is a logic 1 the framed T1 or E1 stream is synchronized to the SBI bus so that it can be inserted into the SBI bus with all DS0s or timeslots in fixed locations. The SYNCH_TRIB bit in the System Interface INSBI Tributary Control Indirect Access Data register must be set to logic 1 and the SBI bus must be selected in the SYSOPT[2:0] bits of the Global Configuration register for synchronous SBI operation. When SYNCSBI is a logic 0 then the timing of the elastic store is not referenced to the SBI bus. SYNCSBI should be set to a logic 0 for all modes of operation except for the Synchronous SBI operation as outlined above.

If SYNCSBI is logic 1, ELSTBYP must be logic 0.

ELSTBYP:

If the ELST Bypass bit is logic 1, the receive frame slip buffer is bypassed, thus eliminating a nominal one frame latency. The bypass may only be enabled when the SBI bus interface is enabled and the payload allowed to float, i.e. the SYSOPT[1:0] bits of the Global Configuration register are binary 10 and the per-tributary SYNCH_TRIB bit of the System Interface INSBI Tributary Control Indirect Access Data register is logic 0.

Register 0x00A3: RX-SBI-ELST Idle Code

Bit	Type	Function	Default
Bit 7	R/W	IDLECODE[7]	1
Bit 6	R/W	IDLECODE[6]	1
Bit 5	R/W	IDLECODE[5]	1
Bit 4	R/W	IDLECODE[4]	1
Bit 3	R/W	IDLECODE[3]	1
Bit 2	R/W	IDLECODE[2]	1
Bit 1	R/W	IDLECODE[1]	1
Bit 0	R/W	IDLECODE[0]	1

IDLECODE[7:0]:

The contents of this register are inserted into each DS0 of tributaries that are out of basic frame alignment (i.e. T1/E1 FRMR INF context bit is logic 0) and the TRKEN T1/E1 FRMR context bit is logic 1.

Register 0x00A4: RX-SBI-ELST Slip Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REG8_9I	X
Bit 4	R	REG5_6I	X
Bit 3	W12C	SLPI[4]	X
Bit 2	W12C	SLPI[3]	X
Bit 1	W12C	SLPI[2]	X
Bit 0	W12C	SLPI[1]	X

SLPI[44:29,16:1]:

A logic 1 in these bits indicate a slip has occurred on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG5_6I:

This bit is a logic 1 if at least one bit in Register 0x00A5 or 0x00A6 is logic 1.

REG8_9I:

This bit is a logic 1 if at least one bit in Register 0x00A8 or 0x00A9 is logic 1.

Register 0x00A5: RX-SBI-ELST Slip Status #2

Bit	Type	Function	Default
Bit 7	W12C	SLPI[12]	X
Bit 6	W12C	SLPI[11]	X
Bit 5	W12C	SLPI[10]	X
Bit 4	W12C	SLPI[9]	X
Bit 3	W12C	SLPI[8]	X
Bit 2	W12C	SLPI[7]	X
Bit 1	W12C	SLPI[6]	X
Bit 0	W12C	SLPI[5]	X

Register 0x00A6: RX-SBI-ELST Slip Status #3

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	SLPI[16]	X
Bit 2	W12C	SLPI[15]	X
Bit 1	W12C	SLPI[14]	X
Bit 0	W12C	SLPI[13]	X

Register 0x00A7: RX-SBI-ELST Reserved

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	Reserved	X
Bit 2	W12C	Reserved	X
Bit 1	W12C	Reserved	X
Bit 0	W12C	Reserved	X

Reserved:

In order to prevent the SLPI[44:29,16:1] interrupts being blocked, these bits must be cleared once the device has been initialized. Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

Register 0x00A8: RX-SBI-ELST Slip Status #4

Bit	Type	Function	Default
Bit 7	W12C	SLPI[36]	X
Bit 6	W12C	SLPI[35]	X
Bit 5	W12C	SLPI[34]	X
Bit 4	W12C	SLPI[33]	X
Bit 3	W12C	SLPI[32]	X
Bit 2	W12C	SLPI[31]	X
Bit 1	W12C	SLPI[30]	X
Bit 0	W12C	SLPI[29]	X

Register 0x00A9: RX-SBI-ELST Slip Status #5

Bit	Type	Function	Default
Bit 7	W12C	SLPI[44]	X
Bit 6	W12C	SLPI[43]	X
Bit 5	W12C	SLPI[42]	X
Bit 4	W12C	SLPI[41]	X
Bit 3	W12C	SLPI[40]	X
Bit 2	W12C	SLPI[39]	X
Bit 1	W12C	SLPI[38]	X
Bit 0	W12C	SLPI[37]	X

Register 0x00AA-00AE: RX-SBI-ELST Reserved

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	Reserved	X
Bit 2	W12C	Reserved	X
Bit 1	W12C	Reserved	X
Bit 0	W12C	Reserved	X

Reserved:

In order to prevent the SLPI[44:29,16:1] interrupts being blocked, these bits must be cleared once the device has been initialized. Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

Register 0x00AF: RX-SBI-ELST Slip Direction #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[4]	X
Bit 2	R	SLPD[3]	X
Bit 1	R	SLPD[2]	X
Bit 0	R	SLPD[1]	X

SLPD[44:29,16:1]:

A logic 1 in these bits indicate the direction of latest slip on the associated tributary. If SLPD[x] is a logic 0, the slip resulted in the repetition of a frame. If SLPD[x] is a logic 1, a frame was lost. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Register 0x00B0: RX-SBI-ELST Slip Direction #2

Bit	Type	Function	Default
Bit 7	R	SLPD[12]	X
Bit 6	R	SLPD[11]	X
Bit 5	R	SLPD[10]	X
Bit 4	R	SLPD[9]	X
Bit 3	R	SLPD[8]	X
Bit 2	R	SLPD[7]	X
Bit 1	R	SLPD[6]	X
Bit 0	R	SLPD[5]	X

Register 0x00B1: RX-SBI-ELST Slip Direction #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[16]	X
Bit 2	R	SLPD[15]	X
Bit 1	R	SLPD[14]	X
Bit 0	R	SLPD[13]	X

Register 0x00B3: RX-SBI-ELST Slip Direction #4

Bit	Type	Function	Default
Bit 7	R	SLPD[36]	X
Bit 6	R	SLPD[35]	X
Bit 5	R	SLPD[34]	X
Bit 4	R	SLPD[33]	X
Bit 3	R	SLPD[32]	X
Bit 2	R	SLPD[31]	X
Bit 1	R	SLPD[30]	X
Bit 0	R	SLPD[29]	X

Register 0x00B4: RX-SBI-ELST Slip Direction #5

Bit	Type	Function	Default
Bit 7	R	SLPD[44]	X
Bit 6	R	SLPD[43]	X
Bit 5	R	SLPD[42]	X
Bit 4	R	SLPD[41]	X
Bit 3	R	SLPD[40]	X
Bit 2	R	SLPD[39]	X
Bit 1	R	SLPD[38]	X
Bit 0	R	SLPD[37]	X

Register 0x00BA: RX-SBI-ELST Slip Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SLPE	0

SLPE:

If this bit is a logic 1, the RXELST bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the SLPI[44:29,16:1] bits is a logic 1.

10.9 T1/E1 Transmit Elastic Store (TX-ELST) Registers

Register 0x00C0: TX-ELST Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access to the transmit elastic store (TX-ELST) context RAM.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the TX-ELST Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the TX-ELST Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the TX-ELST Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x00C1: TX-ELST Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the TX-ELST channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x00C2: TX-ELST Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	ELSTBYP	0

This register contains data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Regardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

Reserved:

This bit must be logic 0 for correct operation.

ELSTBYP:

If the ELST Bypass bit is logic 1, the transmit frame slip buffer is bypassed, thus eliminating a nominal one frame latency. The bypass may only be enabled when the System Interface SBI bus interface is enabled and the payload allowed to float, i.e. the SYSOPT[1:0] bits of the Global Configuration register are binary 10.

Register 0x00C4: TX-ELST Slip Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REG8_9I	X
Bit 4	R	REG5_6I	X
Bit 3	W12C	SLPI[4]	X
Bit 2	W12C	SLPI[3]	X
Bit 1	W12C	SLPI[2]	X
Bit 0	W12C	SLPI[1]	X

SLPI[44:29,16:1]:

A logic 1 in these bits indicate a slip has occurred on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG5_6I:

This bit is a logic 1 if at least one bit in Register 0x00C5 or 0x00C6 is logic 1.

REG8_9I:

This bit is a logic 1 if at least one bit in Register 0x00C8 or 0x00C9 is logic 1.

Register 0x00C5: TX-ELST Slip Status #2

Bit	Type	Function	Default
Bit 7	W12C	SLPI[12]	X
Bit 6	W12C	SLPI[11]	X
Bit 5	W12C	SLPI[10]	X
Bit 4	W12C	SLPI[9]	X
Bit 3	W12C	SLPI[8]	X
Bit 2	W12C	SLPI[7]	X
Bit 1	W12C	SLPI[6]	X
Bit 0	W12C	SLPI[5]	X

Register 0x00C6: TX-ELST Slip Status #3

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	SLPI[16]	X
Bit 2	W12C	SLPI[15]	X
Bit 1	W12C	SLPI[14]	X
Bit 0	W12C	SLPI[13]	X

Register 0x00C7: TX-ELST Reserved

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	Reserved	X
Bit 2	W12C	Reserved	X
Bit 1	W12C	Reserved	X
Bit 0	W12C	Reserved	X

Reserved:

In order to prevent the SLPI[44:29,16:1] interrupts being blocked, these bits must be cleared once the device has been initialized. Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

Register 0x00C8: TX-ELST Slip Status #4

Bit	Type	Function	Default
Bit 7	W12C	SLPI[36]	X
Bit 6	W12C	SLPI[35]	X
Bit 5	W12C	SLPI[34]	X
Bit 4	W12C	SLPI[33]	X
Bit 3	W12C	SLPI[32]	X
Bit 2	W12C	SLPI[31]	X
Bit 1	W12C	SLPI[30]	X
Bit 0	W12C	SLPI[29]	X

Register 0x00C9: TX-ELST Slip Status #5

Bit	Type	Function	Default
Bit 7	W12C	SLPI[44]	X
Bit 6	W12C	SLPI[43]	X
Bit 5	W12C	SLPI[42]	X
Bit 4	W12C	SLPI[41]	X
Bit 3	W12C	SLPI[40]	X
Bit 2	W12C	SLPI[39]	X
Bit 1	W12C	SLPI[38]	X
Bit 0	W12C	SLPI[37]	X

Register 0x00CA-0x00CE: TX-ELST Reserved

Bit	Type	Function	Default
Bit 7	W12C	Reserved	X
Bit 6	W12C	Reserved	X
Bit 5	W12C	Reserved	X
Bit 4	W12C	Reserved	X
Bit 3	W12C	Reserved	X
Bit 2	W12C	Reserved	X
Bit 1	W12C	Reserved	X
Bit 0	W12C	Reserved	X

Reserved:

In order to prevent the SLPI[44:29,16:1] interrupts being blocked, these bits must be cleared once the device has been initialized. Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

Register 0x00CF: TX-ELST Slip Direction #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[4]	X
Bit 2	R	SLPD[3]	X
Bit 1	R	SLPD[2]	X
Bit 0	R	SLPD[1]	X

SLPD[44:29,16:1]:

A logic 1 in these bits indicate the direction of latest slip on the associated tributary. If SLPD[x] is a logic 0, the slip resulted in the repetition of a frame. If SLPD[x] is a logic 1, a frame was lost. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Register 0x00D0: TX-ELST Slip Direction #2

Bit	Type	Function	Default
Bit 7	R	SLPD[12]	X
Bit 6	R	SLPD[11]	X
Bit 5	R	SLPD[10]	X
Bit 4	R	SLPD[9]	X
Bit 3	R	SLPD[8]	X
Bit 2	R	SLPD[7]	X
Bit 1	R	SLPD[6]	X
Bit 0	R	SLPD[5]	X

Register 0x00D1: TX-ELST Slip Direction #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[16]	X
Bit 2	R	SLPD[15]	X
Bit 1	R	SLPD[14]	X
Bit 0	R	SLPD[13]	X

Register 0x00D3: TX-ELST Slip Direction #4

Bit	Type	Function	Default
Bit 7	R	SLPD[36]	X
Bit 6	R	SLPD[35]	X
Bit 5	R	SLPD[34]	X
Bit 4	R	SLPD[33]	X
Bit 3	R	SLPD[32]	X
Bit 2	R	SLPD[31]	X
Bit 1	R	SLPD[30]	X
Bit 0	R	SLPD[29]	X

Register 0x00D4: TX-ELST Slip Direction #5

Bit	Type	Function	Default
Bit 7	R	SLPD[44]	X
Bit 6	R	SLPD[43]	X
Bit 5	R	SLPD[42]	X
Bit 4	R	SLPD[41]	X
Bit 3	R	SLPD[40]	X
Bit 2	R	SLPD[39]	X
Bit 1	R	SLPD[38]	X
Bit 0	R	SLPD[37]	X

Register 0x00DA: TX-ELST Slip Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SLPE	0

SLPE:

If this bit is a logic 1, the TXELST bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the SLPI[44:29,16:1] bits is a logic 1.

10.10T1/E1 Transmit Per-Channel Controller (TPCC) Registers

Register 0x0100: TPCC Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers an indirect channel register access to the Transmit Per-Channel Controller (TPCC) context RAM.

TSADDR[4:0]:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the TPCC Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the TPCC Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the TPCC Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0101: TPCC Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the TPCC context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.
CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Registers 0x0102-0x0106: TPCC Indirect Channel Data Registers

These registers contain data read from the TPCC channel context RAM after an indirect read operation or data to be inserted into the TPCC channel context RAM in an indirect write operation.

The bits to be written to the TPCC channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All three registers from 0x0102 through 0x0104 inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the TPCC Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

TSACCESS=0:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0102	RPRBSLEN[2:0]			RPRBS UNF	MDTRK	MSTRK	PCCE	Unused	00000000
0x0103	T56K PRBS	TPRBS INV	TPRBSLEN[2:0]			TPRBS UNF	R56K PRBS	RPRBS INV	00000000
0x0104	PRBSERR[2:0]			PSYNCI	PSYNC	Reserved	PSYNCE	INV LAST	XXXXXX00
0x0105	PRBSERR[10:3]								XXXXXXXX
0x0106	Unused			PRBSERR[15:11]					XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0102	SIGC[0]	INV[1:0]		ALAW	DMW	IDLC	ZCS[1:0]		00000000
0x0103	IDLE[2:0]			A’	B’	C’	D’	SIGC[1]	000000000
0x0104	Unused	TPRBS	RPRBS	IDLE[7:3]					X0000000
0x0105	Unused								XXXXXXXX
0x0106	Unused								XXXXXXXX

In the following bit descriptions, the system interface refers to either the SBI Add bus or the Egress H-MVIP Interface. Be aware that the PRBS receiver documented is down stream of the frame slip buffer; therefore, controlled slips will corrupt the bit sequence and result in bit errors and momentary loss of synchronization.

PCCE:

The per-tributary configuration enable bit, PCCE, enables the per-timeslot configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, it enables the both the TSACCESS=0 and TSACCESS=1 Configuration bits. The global PCCE bit of the TPCC Configuration Bits register must also be logic 1 for this bit to have effect.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

The PCCE context bit must be logic 0 if the tributary is not being used. This is the case when the ENBL bit programmed through the EXSBI Tributary Control Indirect Access Data register is logic 0.

MSTRK:

Master Signaling Trunk Conditioning. When this bit is logic 1, signaling substitution is performed on all channels/time slots for a tributary. Setting MSTRK is equivalent to setting the SIGC[1:0] bits to binary 01 for all channels/timeslots.

MDTRK:

Master Data Trunk Conditioning. When this bit is logic 1, idle code substitution is performed on all channels/time slots for a tributary. Setting MDTRK is equivalent to setting the IDLC Per-Channel context bit to logic 1 for all channels/timeslots.

RPRBSUNF:

If this bit is logic 1, the PRBS is expected to fill all bits in the tributary data stream received from the system interface (SBI Add bus or H-MVIP). This bit supercedes the Per-Channel RPRBS context bits and the R56KPRBS context bits.

RPRBSLEN[2:0]:

The Receive PRBS Length field determines the sequence length of the expected bit pattern received from the system interface (SBI Add bus or H-MVIP):

RPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

RPRBSINV:

If this bit is logic 1, the logical polarity of the received PRBS is inverted before comparison.

R56KPRBS:

If this bit is logic 1, the PRBS is expected to fill only the first seven bits of the selected channels/time slots. Otherwise, the PRBS is expected to occupy the entire selected channels/time slots.

TPRBSUNF:

If this bit is logic 1, the PRBS fills all bits of the of the mapped or multiplexed tributary. This bit supercedes the Per-Channel TPRBS context bits and the T56KPRBS context bits. If TPRBSUNF is logic 1, the FDIS and CASDIS bits must be set to logic 1 through the T1/E1 Transmitter Indirect Channel Data registers. Common channel signaling must also be disabled.

TPRBSLEN[2:0]:

The Transit PRBS Length field determines the sequence length of the generated bit pattern destined for the line side:

TPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

TPRBSINV:

If this bit is logic 1, the logical polarity of the generated PRBS is inverted before transmission.

T56KPRBS:

If this bit is logic 1, the generated PRBS fills only the first seven bits of the selected channels/time slots. Otherwise, the PRBS occupies the entire selected channels/time slots.

INVLAST:

If this bit is logic 1, inversion (as controlled by the INV[1:0] Per-Channel context bits) is the last per-channel operation performed on the data. Otherwise, inversion is the first operation performed.

PSYNCE:

If this bit is a logic 1, the associated TPCCI[x] bit is set upon a change in the PSYNC context bit.

PSYNC:

PSYNC is the PRBS synchronization status. PSYNC becomes a logic 1 if the received data matched the expected sequence for the latest four bytes. PSYNC is set to logic 0 only if 3 consecutive bytes are in error.

PSYNCI:

PSYNCI becomes a logic 1 upon a change in the PSYNC context bit. It is cleared upon an indirect read access.

PRBSERR[15:0]:

The PRBS Error holding register contains a count of the discrepancies between the expected PRBS sequence and the receive data that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1. The count saturates at all ones.

ZCS[1:0]:

These bits control the Zero Code Suppression in the transmitted tributary as follows:

T1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	GTE Zero Code Suppression. The least significant bit (bit 8) of an all zeros channel is forced to a one, except for signaling frames where the second least significant bit is forced to a one.
10	DDS Zero Code Suppression. All zero channel data is replaced with the pattern "10011000"
11	Bell Zero Code Suppression. The second least significant bit (bit 7) of an all zeros channel is forced to a one.

E1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	Jammed bit-8. The least significant bit (bit 8) of an all zeros channel is forced to a one.
10	No Zero Code Suppression
11	Jammed bit-8.

Zero code suppression occurs after data inversion, idle code insertion, digital milliwatt insertion and signaling have occurred.

IDLC:

If this bit is logic 1, the channel/time slot data is replaced by the value in the IDLE[7:0] field.

DMW:

If this bit is logic 1, the channel/time slot data is replaced by the Digital Milliwatt signal. The encoding of the 1 kHz sine wave is determined by the ALAW context bit.

ALAW:

This bit determines the encoding of the Digital Milliwatt signal. If ALAW is logic 0, μ-law companding is respected. If ALAW is logic 1, A-law companding is respected.

INV[1:0]:

These bits invert the channel/time slot data:

INV[1:0]	T1 Description	E1 Description
00	No inversion (default)	No inversion (default)
01	Only the MSB of the received PCM channel data is inverted (Sign bit inversion)	Invert even bits
10	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)	Invert odd bits
11	Invert all bits	Invert all bits

Signaling is not subjected to inversion.

SIGC[1:0]:

These bits determine the source of inserted signaling:

SIGC[1:0]	Description
00	No signaling insertion.
01	Signaling taken from A', B', C' and D' context bits.
10	Signaling taken from system interface.
11	Reserved.

The SIGC bits should be “00” if the INBANDCTL bit of the TPCC Configuration register is logic 1.

A’,B’,C’,D’:

These signaling bits are inserted at the system interface when the MSTRK bit is logic 1 or if the SIGC[1:0] bits are binary 01. For the T1 SF frame format, C’ and D’ must equal A’ and B’, respectively.

IDLE[7:0]:

This field contains the value inserted if the MDTRK or IDLC bit is logic 1.

RPRBS:

If this bit is logic 1, a PRBS is expected in the channel/time slot received from the system interface (SBI Add bus or H-MVIP).

TPRBS:

If this bit is logic 1, a PRBS is generated in the channel/time slot destined for the line side.

Register 0x0107: TPCC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	INTE	0
Bit 3	R/W	INBANDCTL	0
Bit 2	W12C	XFERI	X
Bit 1	R/W	XFERE	0
Bit 0	R/W	PCCE	0

INTE:

If this bit is a logic 1, the TPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the TPCCI[44:29,16:1] bits is a logic 1.

INBANDCTL:

This bit enables the control of the signaling insertion via an inband mechanism. If INBANDCTL is logic 1, the robbed bit signaling insertion is controlled by the third and fourth bits in each octet received on CASED[1:21]. If INBANDCTL is logic 0, robbed bit signaling is strictly controlled by the TPCC SIGC[1:0] context bits.

INBANDCTL only has effect for T1 tributaries and only if the CAS source is H-MVIP (i.e. SYSOPT[1:0] register bits are 01 or 11).

XFERI:

The XFERI bit indicates that a transfer of accumulated PRBS error data has occurred. A logic 1 in this bit position indicates that the holding registers have been updated. This update is initiated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1.

Logic 1 must be written to this bit to clear it to logic 0.

XFERE:

If this bit is a logic 1, the TPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

PCCE:

This global bit enables per-channel/per-timeslot functions in the transmit direction if logic 1. The per-tributary PCCE bits set through the TPCC Indirect Channel Data Registers must also be set to enable individual tributaries.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

Register 0x0108: TPCC Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REGC_DI	X
Bit 4	R	REG9_AI	X
Bit 3	R	TPCCI[4]	X
Bit 2	R	TPCCI[3]	X
Bit 1	R	TPCCI[2]	X
Bit 0	R	TPCCI[1]	X

TPCCI[44:29,16:1]:

A logic 1 in these bits indicate indicate a change of PRBS synchronization state on the associated tributary since this register was last read. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG9_AI:

This bit is a logic 1 if at least one bit in Register 0x0109 or 0x010A is logic 1.

REGC_DI:

This bit is a logic 1 if at least one bit in Register 0x010C or 0x010D is logic 1.

Register 0x0109: TPCC Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	TPCCI[12]	X
Bit 6	R	TPCCI[11]	X
Bit 5	R	TPCCI[10]	X
Bit 4	R	TPCCI[9]	X
Bit 3	R	TPCCI[8]	X
Bit 2	R	TPCCI[7]	X
Bit 1	R	TPCCI[6]	X
Bit 0	R	TPCCI[5]	X

Register 0x010A: TPCC Interrupt Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	TPCCI[16]	X
Bit 2	R	TPCCI[15]	X
Bit 1	R	TPCCI[14]	X
Bit 0	R	TPCCI[13]	X

Register 0x010C: TPCC Interrupt Status #4

Bit	Type	Function	Default
Bit 7	R	TPCCI[36]	X
Bit 6	R	TPCCI[35]	X
Bit 5	R	TPCCI[34]	X
Bit 4	R	TPCCI[33]	X
Bit 3	R	TPCCI[32]	X
Bit 2	R	TPCCI[31]	X
Bit 1	R	TPCCI[30]	X
Bit 0	R	TPCCI[29]	X

Register 0x010D: TPCC Interrupt Status #5

Bit	Type	Function	Default
Bit 7	R	TPCCI[44]	X
Bit 6	R	TPCCI[43]	X
Bit 5	R	TPCCI[42]	X
Bit 4	R	TPCCI[41]	X
Bit 3	R	TPCCI[40]	X
Bit 2	R	TPCCI[39]	X
Bit 1	R	TPCCI[38]	X
Bit 0	R	TPCCI[37]	X

Register 0x0113: TPCC PRBS Error Insertion

Bit	Type	Function	Default
Bit 7	R/W	TPRBS_ERR_INSERT	X
Bit 6	R/W	TPRBS_ADDR[6]	X
Bit 5	R/W	TPRBS_ADDR[5]	X
Bit 4	R/W	TPRBS_ADDR[4]	X
Bit 3	R/W	TPRBS_ADDR[3]	X
Bit 2	R/W	TPRBS_ADDR[2]	X
Bit 1	R/W	TPRBS_ADDR[1]	X
Bit 0	R/W	TPRBS_ADDR[0]	X

TPRBS_ERR_INSERT:

The TPRBS Error insertion Enable bit causes a single bit error to be inserted in the PRBS pattern for the tributary addressed by TPRBS_ADDR[6:0]. A zero to one transition triggers the error insertion.

TPRBS_ADDR[6:0]:

Indicates the tributary into which a single bit error is to be inserted. TPRBS_ADDR[6:5] is the SPE index and ranges from 1 to 2. TPRBS_ADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x0114: TPCC PRBS Error Insert Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	W12C	TPRBS_ERR_INSERTED	X

TPRBS_ERR_INSERTED:

TPRBS_ERR_INSERTED indicates an error has been inserted. This bit is cleared to logic 0 upon writing a logic 1 to the bit position.

10.11 T1/E1 Receive HDLC Controller (RHDL) Registers

Register 0x0118: RHDL Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access.

An indirect write access is illegal when the FACCESS bit of the RHDL Indirect Channel Address Register is logic 1. The result would be that CBUSY would remain logic 1 until this register is written again.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. The data to be written must be set up in the RHDL Indirect Channel Data registers (0x011A - 0x011D) before setting CRWB=0.Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0119: RHDL Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7	R/W	FACCESS	0
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

FACCESS:

If FACCESS is logic 1, the indirect access will be to the packet FIFO. If FACCESS is logic 0, the indirect access will be to the configuration data.

Registers 0x011A – 0x011D: RHDL Indirect Channel Data Registers

This registers contain data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. All four registers from 0x011A through 0x011D inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write (One need not write 0x011B through 0x011D if MEN is logic 0). The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

FACCESS = 0:

Bit Range	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default ('b)
0x011A	Unused	MEN	MM	INVERT	CRC[1:0]		DELIN	EN	X0000000
0x011B	PA[7:0]								00000000
0x011C	SA[7:0]								00000000
0x011D	TA[7:0]								00000000

FACCESS = 1:

Bit Range	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default ('b)
0x011A	HDLCDATA[7:0]								XXXXXXXX
0x011B	CBUSY	Unused	FE	OVR	PKIN	PBS[2:0]			XXXXXXXX
0x011C	Unused								XXXXXXXX
0x011D	Unused								XXXXXXXX

EN:

The enable (EN) bit controls the overall operation of the receive HDLC processor. When EN is logic 1, receive HDLC processor is enabled to identify and buffer packets. When EN is logic 0, the FIFO buffer and interrupts are all cleared.

DELIN:

The indirect delineate enable bit (DELIN) configures the receive HDLC processor to perform flag sequence delineation and bit de-stuffing on the incoming data stream. The delineate enable bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DELIN is set to logic 1, flag sequence delineation and bit de-stuffing is performed on the incoming data stream. When DELIN is set to logic 0, the HDLC does not perform any processing (flag sequence delineation, bit de-stuffing nor CRC verification) on the incoming stream. DELIN reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1:0]:

The CRC algorithm (CRC[1:0]) configures the HDLC processor to perform CRC verification on the incoming data stream. The value of CRC[1:0] to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. The value of CRC[1:0] is ignored when DELIN is low. CRC[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1]	CRC[0]	Operation
0	0	No Verification
0	1	CRC-CCITT
1	0	CRC-32
1	1	Illegal

INVERT:

The HDLC data inversion bit (INVERT) configures the HDLC processor to logically invert the incoming HDLC stream before processing it. When INVERT is set to logic 1, the HDLC stream is logically inverted before processing. When INVERT is set to logic 0, the HDLC stream is not inverted before processing. INVERT reflects the value written until the completion of a subsequent indirect channel read operation.

HDLCDATA[7:0]:

This is the data link byte that has been read from the 127 byte FIFO by the indirect read. It's significance is indicated PBS[2:0] bits. The entire packet including the frame check sequence, but excluding delimiting flags is available to be read from the FIFO except when the DELIN bit is logic 0, in which case the entire data stream is available to be read.

When the REVERSE bit of the RHDL Interrupt Control register is set to logic 0, the least significant bit of each byte of the data bus (HDLCDATA[0]) is the first HDLC bit received (datacom standard). When REVERSE is set to logic 1, HDLCDATA[7] is the first HDLC bit received (telecom standard).

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match field, the SA[1:0] bits of the Secondary Address Match field, the TA[1:0] bits of the Tertiary Address Match field and the two least significant bits of the universal all ones address when performing the address comparison.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the FIFO of only those packets whose first data byte matches either of the bytes written to the Primary, Secondary or Tertiary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the FIFO.

PA[7:0]:

If MEN is logic 1, the first byte received after a flag character is compared against the Primary Address, PA[7:0]. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[7] corresponds to the first bit of the packet. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

SA[7:0]:

If MEN is logic 1, the first byte received after a flag character is compared against the Secondary Address, SA[7:0]. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[7] corresponds to the first bit of the packet. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

TA[7:0]:

If MEN is logic 1, the first byte received after a flag character is compared against the Tertiary Address, TA[7:0]. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. TA[7] corresponds to the first bit of the packet. The MM bit in the Configuration Register is used mask off TA[1:0] during the address comparison.

PBS[2:0]:

The packet byte status (PBS[2:0]) bits indicate the status of the data read concurrently from the FIFO.

PBS[2:0]	Description
000	The data byte read from the FIFO is not special. This code is used for every byte when the DELIN bit is logic 0.
001	Unused
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive. An abort may occur on the initiation of a bit oriented code.
011	Unused
100	The previous data byte read from the FIFO was the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes. The current HDLCDATA[7:0] value contains no valid data.
101	The previous data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet. The current HDLCDATA[7:0] value contains no valid data.
110	The previous data byte read from the FIFO was the last byte of a normally terminated packet with a CRC error. The packet was received in error. The current HDLCDATA[7:0] value contains no valid data.
111	Unused.

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a packet has been written into the FIFO or an abort has occurred. The appropriate RHDLI[44:29,16:1] bit will be set coincidentally. The PKIN bit is cleared to logic 0 after an indirect read.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the FIFO buffer. The appropriate RHDLI[44:29,16:1] bit will be set coincidentally. This bit is not reset to logic 0 until an indirect read. Upon an overflow the contents of the FIFO are emptied.

Because the integrity of the HDLC data is suspect upon a FIFO overflow, it is recommended the FIFO be flushed through indirect reads until an end-of-packet indication is read.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

CBUSY:

This bit is identical to the CBUSY bit of the RHDL Indirect Status register.

Register 0x011E: RHDL Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	REVERSE	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[5:0]:

The FIFO Interrupt Controls determine the FIFO threshold at which an interrupt event is generated. When the number of bytes in the FIFO increases above the binary value of INTC[5:0], the appropriate RHDLI[44:29,16:1] bit is set. Only the crossing of the threshold causes the event. The RHDLI[44:29,16:1] bits will also be set upon a complete packet.

REVERSE:

The REVERSE bit controls the bit ordering of the HDLC data transferred to the microprocessor port. When REVERSE is set to logic 0, the least significant bit of each byte of the data bus (HDLCDATA[0]) is the first HDLC bit received and the most significant bit of each byte (HDLCDATA[7]) is the last HDLC bit received (datacom standard). When REVERSE is set to logic 1, HDLCDATA[0] is the last HDLC bit received while HDLCDATA[7] is the first HDLC bit received (telecom standard).

INTE:

If this bit is logic 1, the INTB output becomes asserted low if any of the RHDLI[44:29,16:1] bits are logic 1.

Register 0x011F: RHDL Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REG3_4I	X
Bit 4	R	REG0_1I	X
Bit 3	W12C	RHDLI[4]	X
Bit 2	W12C	RHDLI[3]	X
Bit 1	W12C	RHDLI[2]	X
Bit 0	W12C	RHDLI[1]	X

RHDLI[44:29,16:1]:

A logic 1 in these bits indicate a change in link status, reception of a complete packet, a FIFO overflow or the crossing if the programmed FIFO fill level on the associated tributary since this register was last read. The associated SPE index is equal to the trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position. The associated RHDLI bit is also cleared to logic 0 upon an indirect read that returns the FE (FIFO empty) bit as a logic 1.

REG0_1I:

This bit is a logic 1 if at least one bit in Register 0x0120 or 0x0121 is logic 1.

REG3_4I:

This bit is a logic 1 if at least one bit in Register 0x0123 or 0x0124 is logic 1.

Register 0x0120: RHDL Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[12]	X
Bit 6	W12C	RHDLI[11]	X
Bit 5	W12C	RHDLI[10]	X
Bit 4	W12C	RHDLI[9]	X
Bit 3	W12C	RHDLI[8]	X
Bit 2	W12C	RHDLI[7]	X
Bit 1	W12C	RHDLI[6]	X
Bit 0	W12C	RHDLI[5]	X

Register 0x0121: RHDL Interrupt Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	W12C	RHDLI[16]	X
Bit 2	W12C	RHDLI[15]	X
Bit 1	W12C	RHDLI[14]	X
Bit 0	W12C	RHDLI[13]	X

Register 0x0123: RHDL Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[36]	X
Bit 6	W12C	RHDLI[35]	X
Bit 5	W12C	RHDLI[34]	X
Bit 4	W12C	RHDLI[33]	X
Bit 3	W12C	RHDLI[32]	X
Bit 2	W12C	RHDLI[31]	X
Bit 1	W12C	RHDLI[30]	X
Bit 0	W12C	RHDLI[29]	X

Register 0x0124: RHDL Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[44]	X
Bit 6	W12C	RHDLI[43]	X
Bit 5	W12C	RHDLI[42]	X
Bit 4	W12C	RHDLI[41]	X
Bit 3	W12C	RHDLI[40]	X
Bit 2	W12C	RHDLI[39]	X
Bit 1	W12C	RHDLI[38]	X
Bit 0	W12C	RHDLI[37]	X

10.12T1/E1 Transmit HDLC Controller (THDL) Registers

Register 0x0130: THDL Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	HDLC_PROV_DIS	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

HDLC_PROV_DIS:

The channel indirect access control bit (HDLC_PRV_DIS) disables a configure (write) or interrogate (read) access to the HDLC context bits (as opposed to the FIFO configuration). Writing a logic 1 to HDLC_PRV_DIS, indicates that only the LFILLE, UDRE, OVRE, FULLE, FIFOCLR, LINT, UTHR, SW_ABT and REVERSE bits are updated by a configuration (faccess = 0) indirect write operation. Writing a logic 0 to HDLC_PRV_DIS enables configuration writes to the HDLC processor context bits (DELIN, IDLE, CRC[1:0], DCRC and INVERT) as well as the FIFO configuration during an indirect write operation. When an indirect write is performed when HDLC_PROV_DIS is logic 1, the HDLC processor is reset and an abort is always issued.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB configures an indirect write operation. A write to the first Indirect Channel Data register triggers the actual write access. Data to be written is taken from the Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register or the first THDL Indirect Channel Data register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the THDL Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0131: THDL Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7	R/W	FACCESS	0
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

FACCESS:

If FACCESS is logic 1, the indirect access will be to the packet FIFO. If FACCESS is logic 0, the indirect access will be to the configuration data.

Register 0x0132 – 0x0136: THDL Indirect Channel Data Registers

This registers contain data read from the THDL channel context or FIFO RAM after an indirect read operation or data to be inserted into the THDL channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All five registers from 0x0132 through 0x0136 inclusive must be written prior to each indirect write with FACCESS=0 unless one desires the same configuration as the latest indirect write. Only 0x0132 and 0x0133 need to be written if FACCESS=1. The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

An indirect write can be initiated by the act of writing to 0x0132. The CRWB must be logic 0 for the indirect write to occur. If one is streaming in a packet, one need only set up the channel address (CADDR[6:0]) at the beginning and perform consecutive writes to 0x0132.

Note: The THDL can transmit a minimum packet size is 2 bytes.

FACCESS=0:

Bit Index	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0132	INVERT	DCRC	CRC[1:0]		IDLE	DELIN	Unused	Unused	000000XX
0x0133	Unused	Unused	ABT	FIFOCLR	FULLE	OVRE	UDRE	LFILLE	XX000000
0x0134	Unused	Unused	Unused	Unused	Unused	INTE*	FLG SHARE*	REVERSE	XXXXX000
0x0135	Unused	UTHR[6:0]							X0000000
0x0136	Unused	LINT[6:0]							X0000000

* These are global bits that affect all tributaries immediately upon a write. An indirect write operation is not required.

FACCESS=1:

	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default ('b)
0x0132	HDLCDATA[7:0]								XXXXXXXX
0x0133	EMPTY	FULL	BLFILL	FULLI	OVRI	UDRI	LFILLI	EOM	XXXXXXX0
0x0134	Unused								XXXXXXXX
0x0135	Unused								XXXXXXXX
0x0136	Unused								XXXXXXXX

FIFOCLR:

The FIFOCLR bit resets the FIFO. When set to logic 1, FIFOCLR will cause the FIFO to be cleared.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the FIFO is transmitted. The FIFO is then reset. All data in the FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

Note: PRM insertion takes precedence over the ABT register bit. When a PRM frame is available, the 2 flag sequences before will be transmitted before and 1 or 2 flag sequences (depending on the FLGSHARE bit setting) after the PRI frame. If the ABT bit is still set, the transmit the Abort sequence will be transmitted again.

DELIN:

The indirect delineate enable bit (DELIN) configures the HDLC processor to perform flag sequence insertion and bit stuffing on the outgoing data stream. The delineate enable bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DELIN is set high, flag sequence insertion, bit stuffing and, optionally, CRC generation is performed on the outgoing HDLC data stream. When DELIN is set low, the HDLC does not perform any processing (flag sequence insertion, bit stuffing nor CRC generation) on the outgoing stream. DELIN reflects the value written until the completion of a subsequent indirect channel read operation. When setting DELIN = 0, care should be taken in the bit order in which the HDLC packet is inserted, especially as it relates to the REVERSE bit setting within this register.

The option to set DELIN to logic 0 is provided to support clear channel applications on the data link. When DELIN is logic 0, it is assumed the process writing to the FIFO will prevent it from becoming empty. Failure to do so will result in a bit sequence that resembles an HDLC abort followed by HDLC flags.

IDLE:

The interframe time fill bit (IDLE) configures the HDLC processor to use flag bytes or HDLC idle as the interframe time fill between HDLC packets. The value of IDLE to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When IDLE is set low, the HDLC processor uses flag bytes as the interframe time fill. When IDLE is set high, the HDLC processor uses HDLC idle (all one's bit with no bit-stuffing pattern is transmitted) as the interframe time file. IDLE reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1:0]:

The CRC algorithm (CRC[1:0]) configures the HDLC processor to perform CRC generation on the outgoing HDLC data stream. The value of CRC[1:0] to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. The value of CRC[1:0] is ignored when DELIN is low. CRC[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1]	CRC[0]	Operation
0	0	No Generation
0	1	CRC-CCITT Generated
1	0	CRC-32 Generated
1	1	Reserved

DCRC:

The HDLC diagnostic CRC bit (DCRC) configures the HDLC processor to logically invert the inserted FCS on the outgoing HDLC stream for diagnostic purposes. The value of DCRC to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DCRC is set high, the FCS value inserted by the HDLC processor is logically inverted. The inserted FCS is not inverted when DCRC are set low. DCRC is ignore when DELIN is set low or CRC[1:0] is equal to "00". DCRC reflects the value written until the completion of a subsequent indirect channel read operation.

INVERT:

The HDLC data inversion bit (INVERT) configures the HDLC processor to logically invert the outgoing HDLC stream on TXDAT[7:0]. The value of INVERT to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When INVERT is set to one, the outgoing HDLC stream is logically inverted. The outgoing HDLC stream is not inverted when INVERT is set to zero. INVERT reflects the value written until the completion of a subsequent indirect channel read operation.

LFILLE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the LFILLI bit transitioning to logic 1.

UDRE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the UDRI bit transitioning to logic 1.

OVRE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the OVRI bit transitioning to logic 1.

FULLE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the FULLI bit transitioning to logic 1.

HDLCDATA[7:0]:

Data to be transmitted on the channel.

When the REVERSE bit is logic 0, the least significant bit (HDLCDATA[0]) is the first HDLC bit transmitted. When REVERSE is logic 1, HDLCDATA[0] is the last HDLC bit transmitted.

HDLCDATA[7:0] is write-only. Arbitrary data is returned upon an indirect read.

EOM:

The EOM bit indicates that the current byte of data is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated.

EOM is write-only. An arbitrary value is returned upon an indirect read.

LFILLI:

The LFILLI bit will transition to logic 1 when the THDL FIFO level transitions to empty or falls below the programmed LINT[6:0] value. This flag is also asserted after an overflow condition has occurred. LFILLI is cleared upon an indirect read access.

UDRI:

The UDRI bit will transition to 1 when the THDL FIFO underruns. That is, the THDL was in the process of transmitting a packet when it ran out of data to transmit. UDRI is cleared upon an indirect read access.

OVRI:

The OVRI bit will transition to 1 when the THDL FIFO overruns. That is, the THDL FIFO was already full when another data byte was written via an indirect write. OVRI is cleared upon an indirect read access.

FULLI:

The FULLI bit will transition to logic 1 when the THDL FIFO is full. FULLI is cleared upon an indirect read access.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty. This flag is also asserted after an overflow condition has occurred.

FULL:

The FULL bit reflects the current condition of the FIFO. If FULL is a logic 1, the THDL FIFO already contains 128-bytes of data and can accept no more.

EMPTY:

The status of the addressed channel's FIFO empty flag. When logic 1, the FIFO is empty. This flag is also asserted after an overflow condition has occurred. When logic 0, the FIFO contains data.

INTE:

If this bit is logic 1, the INTB output becomes asserted low if any of the THDLI[44:29,16:1] bits are logic 1.

FLGSHARE:

The FLGSHARE bit configures the HDLC transmitter to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, then separate closing and opening flags are inserted between successive frames.

REVERSE:

The REVERSE bit controls the bit ordering of the HDLC data transferred from the microprocessor port. When REVERSE is logic 0, the least significant bit of the data bus (HDLCDATA[0]) is the first HDLC bit transmitted and the most significant bit (HDLCDATA[7]) is the last HDLC bit transmitted (datacom standard). When REVERSE is logic 1, HDLCDATA[0] is the last HDLC bit transmitted and HDLCDATA[7] is the first HDLC bits transmitted (telecom standard).

UTHR[6:0]:

The UTHR[6:0] bits define the FIFO fill level which will automatically cause the bytes stored in the FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 0x7F. If UTHR is 0x7F, transmission of packets only occurs upon writing an end-of-message byte to the FIFO.

LINT[6:0]:

The LINT[6:0] bits define the FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the FIFO level decrements to empty or to a value less than LINT[6:0], the LFILLI context bit will be set to logic 1. LFILLI will cause an interrupt on INT if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 0x00.

Register 0x0137: THDL Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REGB_CI	X
Bit 4	R	REG8_9I	X
Bit 3	W12C	THDLI[4]	X
Bit 2	W12C	THDLI[3]	X
Bit 1	W12C	THDLI[2]	X
Bit 0	W12C	THDLI[1]	X

THDLI[44:29,16:1]:

A logic 1 in these bits indicate a change of FIFO state (eg. threshold crossing, full, underflow) on the associated tributary since this register was last read. The associated SPE index is equal to the trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG8_9I:

This bit is a logic 1 if at least one bit in Register 0x0138 or 0x0139 is logic 1.

REGB_CI:

This bit is a logic 1 if at least one bit in Register 0x013B or 0x013C is logic 1.

Register 0x0138: THDL Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	THDLI[12]	X
Bit 6	W12C	THDLI[11]	X
Bit 5	W12C	THDLI[10]	X
Bit 4	W12C	THDLI[9]	X
Bit 3	W12C	THDLI[8]	X
Bit 2	W12C	THDLI[7]	X
Bit 1	W12C	THDLI[6]	X
Bit 0	W12C	THDLI[5]	X

Register 0x0139: THDL Interrupt Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	W12C	THDLI[16]	X
Bit 2	W12C	THDLI[15]	X
Bit 1	W12C	THDLI[14]	X
Bit 0	W12C	THDLI[13]	X

Register 0x013B: THDL Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	THDLI[36]	X
Bit 6	W12C	THDLI[35]	X
Bit 5	W12C	THDLI[34]	X
Bit 4	W12C	THDLI[33]	X
Bit 3	W12C	THDLI[32]	X
Bit 2	W12C	THDLI[31]	X
Bit 1	W12C	THDLI[30]	X
Bit 0	W12C	THDLI[29]	X

Register 0x013C: THDL Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	THDLI[44]	X
Bit 6	W12C	THDLI[43]	X
Bit 5	W12C	THDLI[42]	X
Bit 4	W12C	THDLI[41]	X
Bit 3	W12C	THDLI[40]	X
Bit 2	W12C	THDLI[39]	X
Bit 1	W12C	THDLI[38]	X
Bit 0	W12C	THDLI[37]	X

10.13T1/E1 Signaling Extractor Registers

Register 0x0150: SIGX Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers a SIGX indirect channel register access.

TSADDR[4:0]:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the SIGX Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the SIGX Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the SIGX Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0151: SIGX Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Registers 0x0152-0x0156: SIGX Indirect Channel Data Registers

These registers contain data read from the SIGX channel context RAM after an indirect read operation or data to be inserted into the SIGX channel context RAM in an indirect write operation.

The bits to be written to the SIGX channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All five registers from 0x0152 through 0x0156 inclusive must be written prior to each indirect write with TSACCESS=0 unless one desires the same configuration as the latest indirect write. Only 0x0152 needs to be written if TSACCESS=1. The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the SIGX Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

TSACCESS=0:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0152	COSS[5:1]					Reserved	SIGE	PCCE	XXXXX000
0x0153	COSS[13:6]								XXXXXXXX
0x0154	COSS[21:14]								XXXXXXXX
0x0155	COSS[29:22]								XXXXXXXX
0x0156	Unused						COSS[31:30]		XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0152	A	B	C	D	Unused	FIX	POL	DEBE	XXXXXXXX
0x0153	Unused								XXXXXXXX
0x0154	Unused								XXXXXXXX
0x0155	Unused								XXXXXXXX
0x0156	Unused								XXXXXXXX

Reserved:

This bit must be set to logic 0 for correct operation.

PCCE:

The per-timeslot configuration enable bit, PCCE, enables the configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, the Per-Timeslot Configuration bits are enabled. Refer to the Per-timeslot Configuration descriptions for configuration bit details.

SIGE:

When logic 1, the SIGE bit enables a change of signaling state in any one of the 24 timeslots (T1 mode) or 30 timeslots for (E1 mode) to set the associated COSSI[x] bit in the Change of Signaling Status registers.

COSS[31:1]

The change of signaling state (COSS) bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 or T1 timeslot. The COSS bits are cleared upon an indirect read access. Although there are only 30 signalling timeslots for E1, the maintenance information from timeslot 16 is extracted by SIGX. Hence there are 31 COSS bits.

DEBE:

The DEBE bit enables debouncing of timeslot/channel signaling bits. A logic 1 in this bit position enables signaling debouncing while a logic 0 disables it. When debouncing is selected, per-timeslot/per-channel signaling transitions are ignored until two consecutive, equal values are sampled. Debouncing is performed on the entire signaling state.

FIX, POL:

In T1 mode, if the FIX bit is a logic 1, the signaling bit position in the PCM data stream is forced to the value of the POL bit. The substitution occurs during signaling frames only.

A,B,C,D:

This is the extracted, optionally debounced, signaling state. For the T1 SF framing format, the A and B bits are the signaling bits for every even superframe, and the C and D bits are the signaling bits every odd superframe. This presentation allows the representation of the SLC-96 nine-state signaling. The associated COSS[x] bit is set of logic 1 whenever the state of these bits changes.

Register 0x0157: SIGX Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	GPCCE	0

GPCCE:

This bit globally enables per-channel/per-timeslot functions. This global enable and the per-channel PCCE bit must be both to set to logic 1 for the POL and FIX per-timeslot bits to have any effect.

Register 0x0158: Change of Signaling Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REGC_DI	X
Bit 4	R	REG9_AI	X
Bit 3	R	COSSI[4]	X
Bit 2	R	COSSI[3]	X
Bit 1	R	COSSI[2]	X
Bit 0	R	COSSI[1]	X

COSSI[44:29,16:1]:

A logic 1 in these bits indicate a change of signaling state on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon an indirect read of the associated SIGX Indirect Channel Data Registers.

REG9_AI:

This bit is a logic 1 if at least one bit in Register 0x0159 or 0x015A is logic 1.

REGC_DI:

This bit is a logic 1 if at least one bit in Register 0x015C or 0x015D is logic 1.

Register 0x0159: Change of Signaling Status #2

Bit	Type	Function	Default
Bit 7	R	COSSI[12]	X
Bit 6	R	COSSI[11]	X
Bit 5	R	COSSI[10]	X
Bit 4	R	COSSI[9]	X
Bit 3	R	COSSI[8]	X
Bit 2	R	COSSI[7]	X
Bit 1	R	COSSI[6]	X
Bit 0	R	COSSI[5]	X

Register 0x015A: Change of Signaling Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	COSSI[16]	X
Bit 2	R	COSSI[15]	X
Bit 1	R	COSSI[14]	X
Bit 0	R	COSSI[13]	X

Register 0x015C: Change of Signaling Status #4

Bit	Type	Function	Default
Bit 7	R	COSSI[36]	X
Bit 6	R	COSSI[35]	X
Bit 5	R	COSSI[34]	X
Bit 4	R	COSSI[33]	X
Bit 3	R	COSSI[32]	X
Bit 2	R	COSSI[31]	X
Bit 1	R	COSSI[30]	X
Bit 0	R	COSSI[29]	X

Register 0x015D: Change of Signaling Status #5

Bit	Type	Function	Default
Bit 7	R	COSSI[44]	X
Bit 6	R	COSSI[43]	X
Bit 5	R	COSSI[42]	X
Bit 4	R	COSSI[41]	X
Bit 3	R	COSSI[40]	X
Bit 2	R	COSSI[39]	X
Bit 1	R	COSSI[38]	X
Bit 0	R	COSSI[37]	X

Register 0x0163: Change of Signaling Status Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	COSSE	0

COSSE:

If this bit is a logic 1, the SIGX bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the COSSI[44:29,16:1] bits is a logic 1.

10.14T1/E1 Transmitter Registers

Register 0x0168: T1/E1 Transmitter Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the T1/E1 Transmitter channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the T1/E1 Transmitter Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the T1/E1 Transmitter Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the T1/E1 Transmitter Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0169: T1/E1 Transmitter Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the T1/E1 Transmitter channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Registers 0x016A-0x016F: T1/E1 Transmitter Indirect Channel Data Registers

These registers contain data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All six registers from 0x016A through 0x016F inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the associated E1/T1B bits in the SPE Configuration registers. If The E1/T1B bit associated with a tributary is logic 1, the E1 bit descriptions hold; otherwise, the T1 bit descriptions are valid.

T1 Bit Map:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default ('b)
0x016A	FDIS	XAIS	XYEL	CCSEN	JPN	FMS[1:0]		ESF	00000000
0x016B	IBC[4:0]					IBCL[1:0]		XIBC	00000000
0x016C	BC[3:0]				XBOC	IBC[7:5]			00000000
0x016D	Unused			AISCI	RAICI	T1_FDL_DIS	BC[5:4]		XXXXX000
0x016E	Unused	DL_TS[4:0]					DL_ODD	DL_EVEN	00000000
0x016F	DL_EN[7:0]								00000000

E1 Bit Map:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default ('b)
0x016A	XDIS	CASDIS	TS16AIS	FEBEDIS	GENCRC	INDIS	FDIS	AIS	00000000
0x016B	SPATINV	SPLRINV	FPATINV	RMA	RAI	CCS31EN	CCS15EN	CCS16EN	00000000
0x016C	SaX[4]	SaX_EN[1:4]				SaSEL[2:0]			00000000
0x016D	X[1]	X[3]	X[4]	Si[1:0]		SaX[1:3]			00000000
0x016E	DL_EN[0]	DL_TS[4:0]					DL_ODD	DL_EVEN	00000000
0x016F	Unused	DL_EN[7:1]							00000000

T1 Bit Descriptions

ESF:

A logic 0 selects the SF frame format. A logic 1 selects the ESF frame format.

FMS[1:0]:

These bits determine the format of the facility datalink:

ESF	FMS[1:0]	Facility Datalink
0	00	No datalink; standard SF
0	01	Reserved
0	10	Reserved
0	10	Reserved
1	00	4 kbit/s data link
1	01	2 kbit/s data link (frames 3, 7, 11, 15, 19, 23)
1	10	2 kbit/s data link (frames 1, 5, 9, 13, 17, 21)
1	11	4 kbit/s data link

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the F-bits are included in the CRC-6 calculation, instead of replacing them with ones. If the JPN bit is a logic 1 and the SF format is selected, the framing bit of frame 12 is forced to logic 1 when a Yellow alarm is declared. Otherwise, bit 2 in all of the channels is forced to logic 0 to indicate Yellow alarm. Framing insertion must be enabled (the FDIS bit must be logic 0) in order to transmit the alternate SF Yellow alarm.

CCSEN:

If this bit is logic 1, Channel 24 data is taken from the CCSED[1] input; otherwise, it is derived from the PCM data stream.

This bit must be set to a 0 when using the unframed tributary type with the System Interface SBI bus.

XYEL:

The XYEL bit controls the transmission of the Yellow Alarm signal (a.k.a. RAl). In SF mode, a logic 1 in the XYEL bit causes bit 2 of all channels to be forced to logic 0. If forcing bit 2 would otherwise result in all zeros in a channel, bit 7 is forced to logic 1. In Japanese SF mode, a logic 1 in the XYEL bit causes the F-bit of the twelth frame of the superframe to be forced to logic 1. In ESF mode, a logic 1 in the XYEL bit causes the pattern "0000000011111111" to be repeated in the facility datalink.

If the AUTOYELLOW T1/E1 Framer context bit is a logic 1, a Yellow Alarm is also inserted if the T1/E1 Framer is out-of-frame.

XAIS:

The active high transmit alarm indication (XAIS) signal is used to initiate transmission of an alarm indication signal (all ones).

XAIS supercedes all other configuration bits.

FDIS:

The framing disable (FDIS) bit is used to disable framing of the PCM data stream. When FDIS is logic 0, PCM data is framed; when FDIS is logic 1, insertion of framing into the F-bit position is disabled. Setting this bit allows transmission of unframed Inband Loopback Codes.

This bit must be set to a 1 when using the unframed tributary type with the System Interface SBI bus.

XIBC:

The transmit inband code (XIBC) bit is used to enable the transmission of inband codes. When XIBC is logic 1, the repetitive code defined by the IBC[7:0] bits occupies the entire data stream except the F-bit position if FDIS is logic 0. If FDIS is logic 0, the framing bits simply supercede the inband code bits.

IBCL[1:0]:

The inband code length indicates the length of the inband loopback code sequence, as follows:

IBCL[1:0]	Code Length
00	5
01	6
10	7
11	8

Codes of three or four bits in length may be accommodated by treating them as half of a double-sized code.

IBC[7:0]:

Bits IBC[7:0] contain the inband loopback code pattern to be transmitted. Since IBC[7] is the first bit transmitted, followed by IBC[6], the code should always be aligned with the MSB in the Bit 7 position (for example, a 5-bit code would occupy positions Bit 7 through Bit 2).

Note: 3 or 4-bit patterns must be paired to form a double-sized code (for example, the 3-bit code '011' would be entered as the 6-bit code '011011').

XBOC:

The XBOC bit enables the transmission of bit oriented codes (BOCs) in the facility datalink. If XBOC is logic 1, the sixteen bit sequence of 8 ones, 1 zero, BC[0] to BC[5], and 1 trailing zero is repeated in the facility datalink if the ESF bit is logic 1. XBOC has no effect if ESF is logic 0 or FDIS is logic 1. The XYEL bit takes precedence in that it forces transmission of a "1111111100000000" BOC.

BC[5:0]:

These bits select the 6-bit BOC to be transmitted. To enable these bits to be transmitted as a BOC, the XBOC bit must be logic 1. BC[0] is the first bit transmitted.

The latest code is transmitted at least 10 times. If a second code is written before ten repetitions of the first have been transmitted, the second code will be transmitted immediately after the tenth transmission of the first code. If a third consecutive code is desired, its write must be delayed until the transmission of the second code has started, lest the third code over write the second.

RAICI:

When this bit is logic 1 and the selected frame format is ESF, the RAI-CI alarm is transmitted in the facility data link. RAI-CI is a repetitive pattern within the ESF data link with a period of 1.08 seconds. It consists of sequentially interleaving 0.99 seconds of 00000000 11111111 (right-to-left) with 90 ms of 00111110 11111111.

AISCI:

When this bit is a logic 1, AIS-CI is transmitted. AIS-CI is a repetitive pattern of 1.26 seconds. It consists of 1.11 seconds of an unframed all ones pattern and 0.15 seconds of all ones modified by the AIS-CI signature. The AIS-CI signature is a repetitive pattern 6176 bits in length in which, if the first bit is numbered bit 0, bits 3088, 3474 and 5790 are logical zeros and all other bits in the pattern are logical ones.

T1_FDL_DIS:

The T1 data link disable bit allows the generation of the ESF data links when in T1 mode. If T1_FDL_DIS is a logic 0, the ESF and FMS[1:0] context bits determine the bit locations into which the data link is inserted. When the T1_FDL_DIS bit is a logic 0, the values of the DL_CH[4:0], DL_EVEN and DL_ODD bits are irrelevant. When T1_FDL_DIS is logic 1, the value transmitted in the Facility Data Link bit positions is that received from the system interface.

DL_EVEN:

DL_EVEN controls whether or not the data link is inserted into even numbered frames. If DL_EVEN is a logic 1, then the data link is inserted into even numbered frames. If DL_EVEN is a logic 0, then the data link is not inserted into even numbered frames. For T1 tributaries, the frames in a superframe are considered to be numbered from 1 to 12 or 24.

DL_ODD:

DL_ODD controls whether or not the data link is inserted into odd numbered frames. If DL_ODD is a logic 1, then the data link is inserted into odd numbered frames. If DL_ODD is a logic 0, then the data link is not inserted into odd numbered frames. For T1 tributaries, the frames in a superframe are considered to be numbered from 1 to 12 or 24.

DL_TS[4:0]:

DL_TS gives a binary representation of the time slot into which the data link is to be inserted.

Note: T1 channels 1 to 24 are mapped to values 0 to 23. The DL_TS[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

DL_EN[7:0]:

DL_EN controls which bits of the time slot indicated by DL_TS are to be written with the data link. If DL_EN[X] is a logic 1, then the data link will be inserted into bit X, with bit 7 being the first transmitted.. To insert the data link into the entire time slot, all eight DL_EN bits must be a logic 1.

E1 Bit Descriptions

AIS:

AIS controls the transmission of the alarm indication signal (unframed all-ones). When AIS is a logic 1 the transmit data is forced to all ones. The AIS will be looped back if a diagnostic loopback is enabled.

FDIS:

FDIS controls the generation of the framing alignment signal. When FDIS is a logic 1, generation of the framing pattern in TS0 is disabled. When FDIS is a logic 0, generation of the framing pattern in TS0 is enabled; the contents of TS0 is determined by the INDIS, GENCRC, FEBEDIS, SaSEL[1:4], SaEN[1:4], SaX[1:4], and Si[1:0] bits.

This bit must be set to a 1 when using the unframed tributary type with the System Interface SBI bus.

INDIS:

INDIS controls the insertion of the international and national bits into TS0. When INDIS is set to logic 0, the international and national bits are inserted. The bit values used for the international bits are dependent upon the GENCRC, FEBEDIS, and Si[1:0] context bits. The bit values used for the national bits are dependent upon SaSEL[2:0], Sax_EN[1:4], and SaX[1:4]. When INDIS is a logic 1, the international and national bits are taken directly from the system interface.

GENCRC:

GENCRC controls the generation of the CRC multiframe bits. When GENCRC is a logic 1, the CRC multiframe alignment signal is generated. The CRC bits are calculated and inserted, and the E bits are inserted according to FEBEDIS. The CRC bits transmitted during the first sub-multiframe (SMF) are indeterminate and should be ignored. The CRC bits calculated during the transmission of the nth SMF (SMF n) are transmitted in the following SMF (SMF n+1). When GENCRC is a logic 0, CRC insertion is disabled. The international bitsof FAS frames are set to Si[1] and the international bit of NFAS frames are set to Si[0].

FEBEDIS:

FEBEDIS controls the 'E' bits of a multiframe. If FEBEDIS is logic 1, the 'E' bits are encoded with the contents of the Si[1:0] context bits. If FEBEDIS is logic 0, each 'E' bit is encoded with a 0 when a FEBE is present and a 1 when a FEBE is not present.

TS16AIS:

TS16AIS controls the transmission of the TS16 alarm indication signal. When TS16AIS is a logic 1, TS16 of all frames is forced to all-ones.

CASDIS:

CASDIS controls the generation of the channel associated signaling multiframe formatting. When CASDIS is a logic 0, the CAS framing overhead is inserted into TS16 of frame 0. When CASDIS is a logic 1, the CAS framing overhead is not inserted.

This bit must be set to a 1 for unframed data.

XDIS:

XDIS controls the insertion of the extra bits in TS16 of frame 0 of the signaling multiframe as follows. When XDIS is set to a logic 0, the contents of the X[1], X[3] and X[4] context bits are inserted into TS16, frame 0. When XDIS is a logic 1, the values for those bits positions are taken from the system interface.

CCS16EN:

CCS16EN controls the insertion of Common Channel Signaling (CCS) into TS16. When CCS16EN is a logic 1, TS16 CCS is enabled. TS16 data is taken directly from the CCSED[1] input. When CCS16EN is a logic 0, TS16 CCS is disabled.

CCS15EN:

CCS15EN controls the insertion of CCS into TS15. When CCS15EN is a logic 1, TS15 CCS is enabled. TS15 data is taken directly from the CCSED[2] input. When CCS15EN is a logic 0, TS15 CCS is disabled.

CCS31EN:

CCS31EN controls the insertion of CCS into TS31. When CCS31EN is a logic 1, TS31 CCS is enabled. TS31 data is taken directly from the CCSED[3] input. When CCS31EN is a logic 0, TS31 CCS is disabled.

RAI:

RAI controls the transmission of the remote alarm indication. A logic 1 in the RAI bit position causes bit 3 of NFAS frames to be forced to logic 1. Logic 0 in the RAI bit position causes the transmission of the RAI to be controlled exclusively by the AUTOYELLOW T1/E1 Framer context bit and the alarm state of the framer.

If the AUTOYELLOW T1/E1 Framer context bit is a logic 1, RAI is also inserted if the T1/E1 Framer is out-of-frame or AIS has been declared.

RMA:

RMA controls the transmission of the signaling multiframe remote alarm indication. A logic 1 in the RMA bit position causes the y-bit (bit 6) of TS16 of frame 0 of the signaling multiframe to be forced to logic 1. Logic 0 in the RMA bit position causes the transmission of the signaling multiframe remote alarm to be controlled exclusively by the AUTOYELLOW T1/E1 Framer context bit and the alarm state of the framer..

If the AUTOYELLOW T1/E1 Framer context bit is a logic 1, multiframe remote alarm is also inserted if the T1/E1 Framer is out-of-frame.

FPATINV:

FPATINV is a diagnostic control bit. When set to logic 1, FPATINV forces the frame alignment signal (FAS) written into TS0 to be inverted (i.e., the correct FAS, 0011011, is substituted with 1100100); when set to logic 0, the FAS is unchanged.

SPLRINV:

SPLRINV is a diagnostic control bit. When set to logic 1, SPLRINV forces the "spoiler bit" written into bit 2 of TS0 of NFAS frames to be inverted (i.e., the spoiler bit is forced to 0); when set to logic 0, the spoiler bit is unchanged.

SPATINV:

SPATINV is a diagnostic control bit. When set to logic 1, SPATINV forces the signaling multiframe alignment signal written into bits 1-4 of TS16 of frame 0 of the signaling multiframe to be inverted (i.e., the correct signaling multiframe alignment signal 0000 is substituted with 1111); when set to logic 0, the signaling multiframe alignment signal is unchanged.

The SPATINV still has effect if the CASDIS bit is logic 1. In this case, four TS16 bits are inverted every 16 frames.

SaSEL[2:0]:

SaSEL[2:0] selects which national bit codeword is present in the SaX[1:4] bits. These bits map to the codeword selection as follows:

SaSEL[2:0]	National Bit Codeword
000	Undefined
001	Undefined
010	Undefined
011	Sa4
100	Sa5
101	Sa6
110	Sa7
111	Sa8

SaX_EN[1:4]:

SaX_EN[1:4] enables the bits SaX[1:4] (where X = 4, 5, 6, 7 or 8) respectively. If bits SaX_EN[1: 4] are set to logic 1, then the contents of bits SaX[1:4] are substituted into bit X of TS0 of NFAS frames 1, 3, 5, and 7 of SMF I, or into NFAS frames 9, 11, 13, and 15 of SMF II. If any one or more of the SaX_EN[1:4] bits are set to logic 0, the respective SaX[1:4] register bit is disabled and will not be written into the G.704 CRC multiframe (i.e. the SaX bit that has been disabled will pass through transparently).

SaX[1:4]:

The code word SaX[1:4], (where X = 4, 5, 6, 7, or 8) appears in bit X of TS0 in frames 1, 3, 5 and 7 respectively (SMF I) and in frames 9, 11, 13 and 15 respectively (SMF II) of a G.704 CRC-4 multiframe. If X = 4, the Sa4[1:4] bits appear in bit 4 of frames 1, 3, 5, and 7 respectively (SMF I) and in bit 4 of frames 9, 11, 13, and 15 respectively (SMF II) of a G.704 CRC-4 multiframe. If X = 8, the codeword is inserted into bit 8 of TS 0 in frames 1, 3, 5 and 7 respectively (SMF I), and in frames 9, 11, 13 and 15 respectively (SMF II) of a G.704 CRC-4 multiframe.

The code word written in bits SaX[1:4] is latched internally and is updated every sub-multiframe. Therefore, if the code word is written during SMF I of a G.704 CRC-4 multiframe, it will appear in the SaX[1:4] bits of SMF II of the same multiframe. If the code word is written during SMF II of a multiframe, its contents will be latched internally and will appear in SMF I of the next multiframe.

Si[1:0]:

Si[1] and Si[0] correspond to the international bits and can be programmed to any value. When GENCRC = 0, Si[1] is inserted into bit 1 of TS0 of FAS frames and Si[0] is inserted into bit 1 of TS0 of NFAS frames. When GENCRC is logic 1 and FEBEDIS of logic 1, Si[1] will be inserted into the E bit position of frame 13 and Si[0] will be inserted into the E bit position of frame 15.

The Si[1] and Si[0], bits should be programmed to a logic 1 when not being used to carry information.

X[1], X[3], X[4]:

X[1], X[3], and X[4] control the value programmed in the X[1], X[3], and X[4] bit locations (bits 5, 7, and 8) in TS16 of frame 0 of the signaling multiframe. X[1], X[3], and X[4] should be programmed to a logic 1 when not being used to carry information.

DL_EVEN:

DL_EVEN controls whether or not the data link is inserted into even numbered frames. If DL_EVEN is a logic 1, then the data link is inserted into even numbered frames. If DL_EVEN is a logic 0, then the data link is not inserted into even numbered frames. For E1 tributaries, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15.

DL_ODD:

DL_ODD controls whether or not the data link is inserted into odd numbered frames. If DL_ODD is a logic 1, then the data link is inserted into odd numbered frames. If DL_ODD is a logic 0, then the data link is not inserted into odd numbered frames. For E1 tributaries, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15.

DL_TS[4:0]:

DL_TS gives a binary representation of the time slot into which the data link is to be inserted. The DL_TS[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

DL_EN[7:0]:

DL_EN controls which bits of the time slot indicated by DL_TS are to be written with the data link. If DL_EN[X] is a logic 1, then the data link will be inserted into bit X, with bit 7 being the first transmitted. To insert the data link into the entire time slot, all eight DL_EN bits must be a logic 1.

10.15T1/E1 Framer Registers

Register 0x0170: T1/E1 Framer Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	DIS_R2C	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect T1/E1 Framer channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the T1/E1 Framer channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the T1/E1 Framer Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the T1/E1 Framer Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the T1/E1 Framer Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

DIS_R2C:

The disable read-to-clear bit (DIS_R2C) allows the clearing of interrupt status bits to be suppressed upon an indirect read access. Writing a logic 0 to DIS_R2C indicates that the indirect read access will cause a clear of the channel interrupt status bits. Writing a logic 1 indicates that as a result of the indirect read access the interrupts will not be cleared. The DIS_R2C has no effect on an indirect write access.

Register 0x0171: T1/E1 Framer Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the T1/E1 Framer channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 2. CADDR[4:0] is the tributary index and ranges from 1 to 16.

Register 0x0172 – 0x0186: T1/E1 Framer Indirect Channel Data Registers

These registers contain data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the T1/E1 Framer channel context RAM in an indirect channel write operation must be set up in these registers before triggering the write. All twelve registers from 0x0172 through 0x017B inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Regardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

T1 Bit Map:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default ('b)
0x0172	DL_ODD	DL_EVEN	T1_FDL _DIS	DL_CH[4:0]					00000000
0x0173	DL_BIT[7:0]								00000000
0x0174	FASTD	M2O[1:0]		ESFFA	ESF	FMS[1:0]		JPN	00000000
0x0175	LBACT[5:0]						LBASEL[1:0]		00000000
0x0176	LBDACT[3:0]				LBDSEL[1:0]		LBACT[7:6]		00000000
0x0177	BOCE	CR	PRMEN	CCOFA	LBDACT[7:4]				00000000
0x0178	REDE	YELE	COFAE	FERE	BEEE	SEFE	INFE	IDLE	00000000
0x0179	TRKEN	RAIS	OFFLINE	LBDE	LBAE	AISCIE	RAICIE	AISE	00000000
0x017A	DISFREZ	Unused	Unused	IOOFEN	IREDEN	AUTO OOF	AUTORED	AUTO YELLOW	00000000
0x017B	ALMDE	CONNOUT[6:0]							00000000
0x017C	LBA	AISCI	RAICI	AIS	RED	YEL	INF	OVR	00000000
0x017D	REDI	YELI	COFAI	FERI	BEEI	SEFI	INFI	LBD	00000000
0x017E	BOC[0]	LBDI	LBAI	BOCI	IDLEI	AISCII	RAICII	AISI	00000000
0x017F	BEE[2:0]			BOC[5:1]					00000000
0x0180	FER[1:0]		BEE[8:3]						00000000
0x0181	AISD	Unused	OOF[2:0]			FER[4:2]			00000000
0x0182	Unused								00000000
0x0183	Unused								00000000
0x0184	Unused								00000000
0x0185	AISDI	YELD	LBDD	LBAD	Unused				00000000
0x0186	Unused					YELDI	LBDDI	LBADI	00000000

E1 Bit Map:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default ('b)
0x0172	DL_BIT [0]	DL_ODD	DL_ EVEN	DL_TS[4:0]					00000000
0x0173	UN FRAME D	DL_BIT[7:1]							00000000
0x0174	SMFAS C	BIT2C	REFRDI S	REF CRCEN	REFR	C2NC IWCK	CASDIS	CRCEN	00000000
0x0175	CNT NFAS	OOSMF AIS	SaSEL[2:0]			AISC	RAIC	TS16C	00000000
0x0176	SMFER E	FERE	COFAE	INCMFE	INSMFE	INFE	C2NC IWE	WORD ERR	00000000
0x0177	FEBEE	TS16 AISDE	AISE	REDE	AISDE	RMAIE	RAIE	CMFER E	00000000
0x0178	ICMFPE	ICSMFP E	IFPE	V52 LINKE	CFEBE E	RAIC CRCE	OOOFE	CRCEE	00000000
0x0179	RAIS	OFFLINE	Sa8E	Sa7E	Sa6E	Sa5E	Sa4E	ISMFPE	00000000
0x017A	G706AN NBRAI	OOCMF E0	IOOFE N	IREDEN	AUTO OOF	AUTO RED	AUTO YELLO W	TRKEN	00000000
0x017B	Unused							DISFRE Z	00000000
0x017C	CMFERI	SMFERI	FERI	COFAI	INCMFI	INSMFI	INFI	C2NCIW I	00000000
0x017D	CRCEI	FEBEI	TS16 AISDI	AISI	REDI	AISDI	RMAII	RAII	00000000
0x017E	ISMFPI	ICMFPI	ICSMFP I	IFPI	V52 LINKI	CFEBEI	RAIC CRCI	OOOFI	00000000
0x017F	INSMF	INF	C2NCI W	Sa8I	Sa7I	Sa6I	Sa5I	Sa4I	00000000
0x0180	AISD	RMAI	RAI	V52LIN K	CFEBE	RAIC CRC	OOOF	INCMF	00000000
0x0181	Sa[5:4]		A	Si[2:1]		TS16 AISD	AIS	RED	00000000
0x0182	EXCRC ERR	X[3]	Y	X[1]	X[0]	Sa[8:6]			00000000
0x0183	CRCERR[2:0]			OVR	SaX[4:1]				00000000
0x0184	FER[0]	CRCERR[9:3]							00000000
0x0185	FEBE[1:0]		FER[6:1]						00000000
0x0186	FEBE[9:2]								00000000

OFFLINE:

When a logic 1, the OFFLINE bit suppresses frame realignments at the system interface such that the data is carried clear channel. The frame still attempts to find frame, extract a HDLC datalink, accumulate performance data and to maintain alarm status. This is in contrast with the unframed modes where all maintenance activity is suppressed.

RAIS:

When a logic 1, the RAIS bit forces all ones into the ingress data stream. The current signaling will be frozen if DISFREZ is logic 0.

TRKEN:

The TRKEN bit enables receive trunk conditioning upon an out-of-frame condition. If TRKEN is logic 1, the contents of the RX-ELST Idle Code register are inserted into all time slots (including TS0 and TS16) of the ingress data when the framer is out-of-basic frame (i.e. the INF context bit is logic 0). The TRKEN bit has no effect in System Interface SBI async mode since the receive elastic store is bypassed in this mode. If TRKEN is a logic 0, receive trunk conditioning can still be performed on a per-timeslot basis via the RPCC MSTRK and MDTRK context bits.

AUTOYELLOW:

In T1 mode, when the AUTOYELLOW bit is set to logic 1, whenever the alarm integrator declares a Red alarm in the receive direction, Yellow alarm will be transmitted to the far end. When AUTOYELLOW is set to logic 0, Yellow alarm will only be transmitted when the XYEL bit of T1/E1 Transmitter bit is set.

Note: The Red alarm is not deasserted on detection of AIS.

In E1 mode, when the AUTOYELLOW bit is set to logic 1, the RAI bit in the transmit stream is set to a logic 1 for the duration of a loss of frame alignment or AIS, and the Remote Multiframe Alarm bit (a.ka. 'Y' bit) in the transmit stream is set to a logic 1 for the duration of a loss of signaling multiframe alignment. The G706ANNBRAI bit optionally also allows for the transmission of RAI when CRC-to-non-CRC interworking has been established. When AUTOYELLOW is set to logic 0, RAI will only be transmitted when the RAI bit of T1/E1 Transmitter bit is set and RMA will only be transmitted when the RMA bit of T1/E1 Transmitter bit is set.

AUTORED:

The AUTORED bit allows global trunk conditioning to be applied to the ingress data and signaling streams immediately upon declaration of Red carrier failure alarm. When AUTORED is set to logic 1, the ingress data and signaling for each channel is replaced with the data programmed into the IDLE[7:0] and A'B'C'D' fields of the Receive Per-Channel Controller (RPCC) while Red CFA is declared. When AUTORED is set to logic 0, the ingress data is not automatically conditioned when Red CFA is declared.

AUTOOOF:

The AUTOOOF bit allows global trunk conditioning to be applied to the ingress data stream immediately upon declaration of out of frame (OOF). When AUTOOOF is set to logic 1, while OOF is declared, the ingress data on each channel is replaced with the data programmed into the IDLE[7:0] and A'B'C'D' fields of the Receive Per-Channel Controllers (RPCC-SBI and RPCC-MVIP). When AUTOOOF is set to logic 0, the ingress data is not automatically conditioned by RPCC when OOF is declared. However, if the RX-ELST is not bypassed, the RX-ELST trouble code will still be inserted in channel data while OOF is declared if the TRKEN register bit is logic 1.

Note: RPCC data and signaling trunk conditioning overwrites the RX-ELST trouble code.

IREDEN:

The IREDEN bit enables a received RED alarm to generate an ingress alarm indication onto the System Interface SBI bus. When IREDEN is a logic 1, a received RED alarm will force an alarm indication onto the System Interface SBI bus. When IREDEN is a logic 0, a received RED alarm will not force an alarm indication onto the System Interface SBI bus.

IOOFEN:

The IOOFEN bit enables a received Out Of Frame condition to generate an ingress alarm indication onto the System Interface SBI bus. When IOOFEN is a logic 1, an out of frame condition will force an alarm indication onto the System Interface SBI bus. When IOOFEN is a logic 0, a received out of frame will not force an alarm indication onto the System Interface SBI bus.

OOCMFE0:

When in E1 mode, the OOCMFE0 bit selects between two modes of operation concerning the transmission of E-bits when the E1 framer is out of CRC-4 multiframe. When OOCMFE0 is logic 0, the E1 framer transmits ones for the E-bits while out of CRC-4 multiframe. When OOCMFE0 is logic 1, the E1 framer transmits zeroes for the E-bits while out of CRC-4 multiframe. The option to transmit zeroes as E-bits while out of CRC-4 multiframe is provided to allow compliance with the CRC-4 to non-CRC-4 interworking procedure in Annex B of G.706.

This bit only has effect in E1 mode.

G706ANNBRAI:

When in E1 mode, the G.706 Annex B RAI bit, G706ANNBRAI, selects between two modes of operation concerning the transmission of RAI when the E1 framer is out of CRC-4 multiframe. When G706ANNBRAI is logic 1, the behavior of RAI follows Annex B of G.706, i.e., RAI is transmitted only when out of basic frame, not when CRC-4-to-non-CRC-4 interworking is declared, nor when the offline framer is out of frame. When G706ANNBRAI is logic 0, the behavior of RAI follows ETSI standards, i.e., RAI is transmitted when out of basic frame, when CRC-4-to-non-CRC-4 interworking is declared, and when the offline framer is out of frame.

This bit only has effect in E1 mode.

DISFREZ:

A logic 1 in this bit location will disables signal freezing that normally occurs upon an out-of-frame condition.

DL_CH[4:0]/DL_TS[4:0]:

The data link time slot (DL_CH[4:0]) bits gives a binary representation of the channel from which the data link is to be extracted.

Note: T1 channels 1 to 24 are mapped to values 0 to 23. The DL_CH[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

T1_FDL_DIS:

The T1 data link disable bit allows the termination of the ESF data links when in T1 mode. If T1_FDL_DIS is a logic 0, the ESF and FMS[1:0] context bits determine the bit locations from which the data link is extracted. When the T1_FDL_DIS bit is a logic 0, the value of the DL_CH[4:0], DL_EVEN and DL_ODD bits is irrelevant. When T1_FDL_DIS is logic 1, a data link may be extracted from any one of the 24 DS0s as determined by the DL_CH[4:0], DL_EVEN and DL_ODD bits.

DL_EVEN:

The data link even select (DL_EVEN) bit controls whether or not the data link is extracted from the even frames of the receive data stream. If DL_EVEN is a logic 0, the data link is not extracted from the even frames. If DL_EVEN is a logic 1, the data link is extracted from the even frames. For T1, the frames in a superframe are numbered from 1 to 12 (or 1 to 24 in an extended superframe). For E1, the frames within a CRC multiframe are numbered from 0 to 15. If both DL_EVEN and DL_ODD are logic 1, then the datalink is extracted from all frames. If both DL_EVEN and DL_ODD are logic 0 (and T1_FDL_DIS is logic 1 for T1s), no data link is extracted.

DL_ODD:

The data link odd select (DL_ODD) bit controls whether or not the data link is extracted from the odd frames of the receive data stream. If DL_ODD is a logic 0, the data link is not extracted from the odd frames. If DL_ODD is a logic 1, the data link is extracted from the odd frames. If both DL_EVEN and DL_ODD are logic 1, then the datalink is extracted from all frames. If both DL_EVEN and DL_ODD are logic 0 (and T1_FDL_DIS is logic 1 for T1s), no data link is extracted.

DL_BIT[7:0]:

The data link bit select (DL_BIT[7:0]) bits controls which bits of the time slot/channel are to be extracted and passed to the HDLC controller. If DL_BIT[x] is a logic 1, that bit is extracted as part of the data link. To extract the data link from the entire time slot, all eight DL_BIT[x] bits must be set to a logic 1. DL_BIT[7] corresponds to the most significant bit (bit 1, the first bit received) of the time slot and DL_BIT[0] corresponds to the least significant bit (bit 8, the last bit received) of the time slot. The DL_BIT[7:0] bits have no effect when the DL_EVEN and DL_ODD bits are both logic 0.

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the CRC-6 is calculated using the F-bits as received, instead of replacing them with ones (as would be the case for ESF = logic 1 and JPN = logic 0). If the JPN bit is a logic 1 and a non-ESF format is selected (ESF bit is logic 0), it is assumed that the 12^{th} F-bit of the superframe carries a far end receive failure alarm. The alarm is extracted and the framing is modified to be robust (12^{th} F-bit is X in framing sequence) when the alarm is active.

ESF, FMS[1:0]:

The ESF bit selects ESF framing format, and determines the function of the frame mode select (FMS[1:0]) bits. When the ESF bit set to logic 1, the FMS[1:0] bits select the data rate and the source channel for the facility data link (FDL) data. The framer may receive FDL data at the full 4 kHz rate from every odd frame, at a 2 kHz rate from frames 3, 7, 11, 15, 19, and 23, or at a 2 kHz rate from frames 1, 5, 9, 13, 17, and 21. When the ESF bit is set to logic 0, the FMS[1:0] bits select either SF or transparent framing modes.

The valid combinations of the ESF, and FMS[1:0] bits are summarized in the table below:

ESF	FMS[1]	FMS[0]	Mode
0	0	0	Select SF framing format
0	0	1	Transparent – no attempt is made to frame
0	1	0	SLC-96
0	1	X	Reserved
1	0	0	Select ESF framing format and 4 kHz FDL data rate
1	0	1	Select ESF framing format and 2 kHz FDL data rate using frames 3, 7, 11,15,19, 23
1	1	0	Select ESF framing format and 2 kHz FDL data rate using frames 1, 5, 9, 13, 17, 21
1	1	1	Select ESF framing format and default to 4 kHz FDL data rate

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns. A logic 0 selects an ESF algorithm where the framer does not set INF high while more than one framing bit candidate is following the framing pattern in the PCM stream. A logic 1 selects an ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared to the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

Under most situations, it is recommended that ESFFA be set to logic 1. Setting ESFFA to logic 1 reduces the probability f framing to a mimic framing pattern at the expense of a slightly longer average time to frame. ESFFA logic 1 is more robust at dealing the special situation where a repetitive payload pattern results in a persistent mimic.

M2O[1:0]:

The M2O[1:0] bits are used to set the error threshold for declaring out-of-frame (OOF). For SF and ESF framing formats:

M2O[1]	M2O[0]	OOF Threshold
0	0	2-of-4 framing bits in error
0	1	2-of-5 framing bits in error
1	0	2-of-6 framing bits in error

1	1	Locked in-frame

While locked in-frame criteria is selected, OOF is never declared, regardless of the number of framing bit errors.

FASTD:

Enables the fast deassertion of the Red alarm within 120 ms, the AIS alarm within 180 ms and the AIS-CI alarm within two seconds. A logic 1 in the FASTD bit position enables the fast deassertion mode; a logic 0 disables the fast deassertion mode.

LBASEL[1:0]:

The Loopback Activate Select bits allow for the selection of a loopback code length from three bits to eight bits long as follows:

LBASEL[1]	LBASEL[0]	Code Length
0	0	5 bits
0	1	6 (or 3*) bits
1	0	7 bits
1	1	8 (or 4*) bits

LBACT[7:0]:

This 8-bit field allows the selection of the activate code sequence that is to be detected. If the code is less than 8 bits long, the first 8 bits of the repeated sequence must be used to fill the field. For example, if the code sequence is '00001', the first 8 bits of '0000100001...' are '00001000').

Note: Bit 7 is the first code bit received.

LBDSEL[1:0]:

The Loopback Deactivate Select bits allow for the selection of a loopback code length from three bits to eight bits long as follows:

LBDSEL[1]	LBDSEL[0]	Code Length
0	0	5 bits
0	1	6 (or 3*) bits
1	0	7 bits
1	1	8 (or 4*) bits

LBDACT[7:0]:

This 8-bit field allows the selection of the deactivate code sequence that is to be detected. If the code is less than 8 bits long, the first 8 bits of the repeated sequence must be used to fill the field. For example, if the code sequence is '10011', the first 8 bits of '1001110011...' are '10011100').

Note: Bit 7 is the first code bit received.

CCOFA:

The CCOFA bit determines whether Change-of-Frame Alignment (COFA) events or out-of-frame (OOF) events are counted and stored in the OOF[2:0] context bits. If CCOFA is a logic 1, COFA events are counted.

PRMEN:

When logic 1, the Performance Report Message Enable (PRMEN) bit enables the generation of PRMs upon counter transfers. This bit only has effect in ESF mode.

CR:

The value of this bit is copied into the C/R bit position of each performance reporting message transferred.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt when a valid BOC is detected or removed. A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the BOCI context bit.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code (defined as the bit sequence 1111111101111110). A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the IDLEI context bit.

INFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INF context bit.

SEFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the SEFI bit becoming logic 1.

BEEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the BEEI bit becoming logic 1.

FERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the FERI bit becoming logic 1.

COFAE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the COFAI bit becoming logic 1.

YELE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the YEL context bit.

REDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RED context bit.

AISE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the AIS context bit.

RAICIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RAICI context bit.

AISCIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the AISCI context bit.

LBAE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the LBA context bit.

LBDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the LBD context bit.

ALMDI:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in any one of the AISD, LBAD, LBDD or YELD context bits.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred, and that the contents of the holding registers have been overwritten. OVR is set to logic 0 when this bit is accessed by an indirect read.

If the DIS_R2C bit is a logic 1 when an indirect read occurs, OVR will not accurately reflect that the holding registers have been read.

INF:

INF is the inframe status. In E1 mode, INF indicates basic alignment, as opposed to CRC-4 or signaling multiframe alignment.

YEL:

YEL is the integrated T1 Yellow Alarm status. YEL becomes logic 1 when a Yellow alarm has persisted for 400 ms (±50 ms). YEL becomes logic 0 when the alarm has been absent for 400 ms (±50 ms).

RED:

RED is the integrated RED Alarm status.

T1: The RED bit is a logic 1 if an out of frame condition has persisted for 2.55 s (±40 ms). The RED bit returns to a logic 0 when an out of frame condition has been absent for 16.6 s (±500 ms).

E1: The RED bit is a logic 1 if an out of frame condition has persisted for 100 ms. The RED bit returns to a logic 0 when an out of frame condition has been absent for 100 ms.

AIS:

AIS is the integrated AIS Alarm status.

T1: The AIS bit is a logic 1 when an out of frame all-ones condition has persisted for 2.55 s (±100 ms). The AIS bit returns to a logic 0 when the AIS condition has been absent for 16.6 s (±500 ms).

E1: The AIS bit is a logic 1 when an out of frame all-ones condition has persisted for 100 ms. The AIS bit returns to a logic 0 when the AIS condition has been absent for 100 ms.

RAICI:

RAICI is the integrated RAICI Alarm status.

AISCI:

AISCI is the integrated AIS-CI Alarm status.

LBA:

This bit is set if the inband code programmed by the LBASEL[1:0] and LBACT[7:0] fields have persisted for a minimum of 5.08 seconds (± 40 ms).

The bit is cleared if the code has been absent for 5.08 seconds (± 40 ms).

LBD:

This bit is set if the inband code programmed by the LBDSEL[1:0] and LBDACT[7:0] fields have persisted for a minimum of 5.08 seconds (± 40 ms).

The bit is cleared if the code has been absent for 5.08 seconds (± 40 ms).

INFI:

INFI becomes a logic 1 upon a change in the INF context bit. It is cleared upon an indirect read access.

SEFI:

SEFI becomes a logic 1 upon a severely errored frame event. It is cleared upon an indirect read access.

A Severely Errored Frame (SEF) event is defined as follows:

- SF - 2 or more F_t or F_s bits are in error during a 1.5 ms interval, as delimited by the 12 frame superframe boundary.
- SLC96 - 2 or more F_t or F_s bits are in error during a 1.5 ms interval, as delimited by the 12 frame superframe boundary.
- ESF - 2 or more F_e bits are in error during a 3 ms interval, as delimited by the 24 frame superframe boundary.

BEEI:

BEEI becomes a logic 1 upon a bit error event. It is cleared upon an indirect read access. A bit error event (BEE) is defined as an F-bit error for SF and SLC®96 framing format or a CRC-6 error for ESF framing format.

FERI:

T1: FERI becomes a logic 1 upon a framing error event. It is cleared upon an indirect read access. A framing bit error (FER) is defined as an F_s or F_t error for SF and SLC®96 and an F_e error for ESF framing format.

E1: FERI becomes a logic 1 upon an error in the FAS or NFAS bit positions. It is cleared upon an indirect read access.

COFAI:

COFAI becomes a logic 1 upon a change of frame alignment. It is cleared upon an indirect read access. A change of frame alignment is declared upon frame acquisition (i.e. upon INF becoming logic 1) if the new F-bit's location is different from the previously established frame alignment. The position within the superframe/multiframe is relevant as well as the location within the 193 bit T1 or 256 bit E1 frame.

YELI:

YELI becomes a logic 1 upon a change in the YEL context bit. It is cleared upon an indirect read access.

REDI:

REDI becomes a logic 1 upon a change in the RED context bit. It is cleared upon an indirect read access.

AISI:

AISI becomes a logic 1 upon a change in the AIS context bit. It is cleared upon an indirect read access.

RAICII:

RAICII becomes a logic 1 upon a change in the RAICI context bit. It is cleared upon an indirect read access.

AISCII:

AISCII becomes a logic 1 upon a change in the AISCI context bit. It is cleared upon an indirect read access.

IDLEI:

IDLEI becomes a logic 1 upon validation of an idle bit oriented code (defined as the bit sequence 1111111101111110). It is cleared upon an indirect read access.

BOCI:

BOCI becomes a logic 1 upon validation or removal of a bit oriented code. It is cleared upon an indirect read access.

Note: The transition from one validated code to another will produce two indications. The first will be upon recognizing the first code has been removed (BOC bits will be "111111") and the second will be after the third repetition of the new code. With a 4kHz datalink, these two interrupts will be 8ms apart.

LBAI:

LBAI becomes a logic 1 upon a change in the LBA context bit. It is cleared upon an indirect read access.

LBDI:

LBDI becomes a logic 1 upon a change in the LBD context bit. It is cleared upon an indirect read access.

BOC[5:0]:

These six bits contain the latest validated bit oriented code. BOC[0] is the first bit received. An update of these bits is accompanied by an assertion of the BOCI bit. If no code has been validated or an idle code (defined as the bit sequence 1111111101111110) is being received, these bits are all ones.

BEE[8:0]:

The Bit Error Event holding register contains the count of bit error events that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

A bit error event (BEE) is defined as an F-bit error for SF and SLC®96 framing format or a CRC-6 error for ESF framing format.

FER[4:0]:

The Framing Error Event holding register contains the count of framing bit error events that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

A framing bit error (FER) is defined as an F_s or F_t error for SF and SLC®96 and an F_e error for ESF framing format.

OOF[2:0]:

The Out of Frame Event holding register contains the count of logic 1 to logic 0 transitions on the INF bit that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

AISD:

This bit is set if AIS condition has been detected over a 40ms period. The bit is cleared if the tributary becomes in frame or has sufficient number of zeros within a 40ms period for AIS.

LBAD:

This bit is set if the inband code programmed by the LBASEL[1:0] and LBACT[7:0] fields have been detected over a 40 ms period. The bit is cleared if the code has been absent over a 40 ms period.

LBDD:

This bit is set if the inband code programmed by the LBDSEL[1:0] and LBDACT[7:0] fields have been detected over a 40 ms period. The bit is cleared if the code has been absent over a 40 ms period.

YELD:

This bit is set if Yellow alarm has been detected over a 40ms period. The bit is cleared upon the failure to detect the yellow alarm over a 40ms period or the framer drops out of frame.

AISDI:

AISDI becomes a logic 1 upon a change in the AISD context bit. It is cleared upon an indirect read access.

LBADI:

LBADI becomes a logic 1 upon a change in the LBAD context bit. It is cleared upon an indirect read access.

LBDDI:

LBDDI becomes a logic 1 upon a change in the LBDD context bit. It is cleared upon an indirect read access.

YELDI:

YELDI becomes a logic 1 upon a change in the YELD context bit. It is cleared upon an indirect read access.

UNFRAMED:

If this bit is a logic 1, the framer will not attempt to find frame. The data is passed through transparently with no channel alignment.

CRCEN:

The CRCEN bit enables framing to the CRC multiframe. When the CRCEN bit is logic 1, the framer searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables searching for multiframe and suppresses the INCMF, CRCEI, CMFERI, FEBE, CFEBE, RAICCRC and C2NCIW statuses, forcing them to logic 0.

CASDIS:

The CASDIS bit enables framing to the Channel Associated Signaling multiframe when set to a logic 0. When CAS is enabled, the framer searches for signaling multiframe alignment and monitors for errors in the alignment. A logic 1 in the CASDIS bit position disables searching for multiframe and suppresses the INSMF and the SMFER bits, forcing them to logic 0.

C2NCIWCK:

The C2NCIWCK bit enables the continuous checking for CRC multiframe while in the CRC to non-CRC interworking mode. If this bit is a logic 0, the framer will cease searching for CRC multiframe alignment once in CRC to non-CRC interworking mode. If this bit is a logic 1, the framer will continue searching for CRC multiframe alignment, even if CRC to non-CRC interworking has been declared.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronizations.

REFCRCEN:

The REFCRCEN bit enables excessive CRC errors (≥ 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCEN bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCEN bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the framer to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc.).

Note: Whilst the framer remains locked in frame due to REFRDIS=1, a received AIS will not be detected since the framer must be out-of-frame to detect AIS.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in time slot 0 of NFAS frames has been received in error on 3 consecutive occasions. A logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the absence of FAS frames only.

SMFASC:

The SMFASC bit selects the criterion used to declare loss of signaling multiframe alignment. A logic 0 in the SMFASC bit position enables declaration of loss of signaling multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error. A logic 1 in the SMFASC bit position enables declaration of loss of signaling multiframe when 2 consecutive multiframe alignment patterns have been received in error or when time slot 16 contains logic 0 in all bit positions for 1 or 2 multiframes based on the criterion selected by TS16C.

TS16C:

The TS16C bit selects the criterion used to declare loss of signaling multiframe alignment signal when enabled by the SMFASC. A logic 0 in the TS16C bit position enables declaration of loss of signaling multiframe alignment when time slot 16 contains logic 0 in all bit positions for 1 multiframe. A logic 1 in the TS16C bit position enables declaration of loss of signaling multiframe when time slot 16 contains logic 0 in all bit positions for 2 consecutive signaling multiframes.

RAIC:

The RAIC bit selects criterion used to declare a Remote Alarm Indication (RAI). If RAIC is logic 0, the RAI indication is asserted upon reception of any A=1 (A is bit 3 of NFAS frames) and is deasserted upon reception of any A=0. If RAIC is logic 1, the RAI indication is asserted if A=1 is received on 4 or more consecutive occasions, and is cleared upon reception of any A=0.

AISC:

The AISC bit selects the criterion used for determining AIS alarm indication. If AISC is logic 0, AIS is declared if there is a loss of frame (LOF) indication and a 512 bit period is received with less than 3 zeros. If AISC is a logic 1, AIS is declared if less than 3 zeros are detected in each of 2 consecutive 512 bit periods and is cleared when 3 or more zeros are detected in each of 2 consecutive 512 bit intervals.

EXCRCERR:

The EXCRCERR bit is an active high status bit indicating that excessive CRC evaluation errors (i.e. ≥ 915 error in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCEN bit of the Frame Alignment Options register. The EXCRCERR bit is reset to logic 0 after an indirect read access.

SaSEL[2:0]:

The SaSEL[2:0] bits select which National Bit Codeword appears in the SaX[1:4] bits of the National Bit Codeword register. These bits map to the codeword selection as follows:

SaSEL[2:0]	National Bit Codeword
001	Undefined
010	Undefined
011	Undefined
100	Sa4
101	Sa5
110	Sa6
111	Sa7
000	Sa8

OOSMFAIS:

This bit controls the signaling trunk conditioning in an out of signaling multiframe (OOSMF) condition. If OOSMFAIS is logic 1, an OOSMF indication will cause the CASID[x] or the SBI CAS fields to be set to all 1's.

CNTNFAS:

When CNTNFAS is logic 1, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits consisting of the seven bit FAS pattern and bit 2 of time slot 0 of the next NFAS frame. When CNTNFAS is logic 0, only errors in the FAS affect the framing error count.

WORDERR:

The WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

C2NCIWE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the C2NCIW context bit.

INFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INF context bit.

INSMFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INSMF context bit.

INCMFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INCMF context bit.

COFAE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in basic frame alignment.

FERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon an error in the FAS or NFAS bit positions.

SMFERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon an error in the signaling multiframe alignment pattern.

CMFERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon an error in the CRC multiframe alignment pattern.

RAIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RAI context bit.

RMAIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RMAI context bit.

AISDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the AISD context bit.

TS16AISDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the TS16AISD context bit.

FEBEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set when a logic zero is received in the Si bits (bit 1; E bits) of frames 13 or 15.

CRCEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set when the calculated CRC differs from the received CRC remainder.

OOOFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the OOOF context bit.

RAICRCE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RAICCRC context bit.

CFEBEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the CFEBE context bit.

V52LINKE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the V52LINK context bit.

IFPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each frame.

ICSMPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each CRC sub-multiframe.

ICMFPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each CRC multiframe.

ISMFPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each signaling multiframe.

Sa4E, Sa5E, Sa6E, Sa7E, Sa8E:

The National Use interrupt enables allow changes in Sa code word values to generate an interrupt. If SaNE is a logic 1, a logic 1 in the SaNI bit of the International Bits/National Interrupt Status register will result in the assertion the associated FRMRI[x] bit.

C2NCIWI:

C2NCIWI becomes a logic 1 upon a change in the C2NCIW context bit. It is cleared upon an indirect read access.

INFI:

INFI becomes a logic 1 upon a change in the INF context bit. It is cleared upon an indirect read access.

INSMFI:

INSMFI becomes a logic 1 upon a change in the INSMF context bit. It is cleared upon an indirect read access.

INCMFI:

INCMFI becomes a logic 1 upon a change in the INCMF context bit. It is cleared upon an indirect read access.

SMFERI:

SMFERI becomes a logic 1 upon an error in the signaling multiframe alignment pattern. It is cleared upon an indirect read access.

CMFERI:

CMFERI becomes a logic 1 upon an error in the CRC multiframe alignment pattern. It is cleared upon an indirect read access.

RAII:

RAII becomes a logic 1 upon a change in the RAI context bit. It is cleared upon an indirect read access.

RMAII:

RMAII becomes a logic 1 upon a change in the RMAI context bit. It is cleared upon an indirect read access.

AISDI:

AISDI becomes a logic 1 upon a change in the AISD context bit. It is cleared upon an indirect read access.

REDI:

REDI becomes a logic 1 upon a change in the RED context bit. It is cleared upon an indirect read access.

AISI:

AISI becomes a logic 1 upon a change in the AIS context bit. It is cleared upon an indirect read access.

TS16AISDI:

TS16AISDI becomes a logic 1 upon a change in the TS16AISD context bit. It is cleared upon an indirect read access.

FEBEI:

FEBEI becomes a logic 1 when a logic zero is received in the Si bits of frames 13 or 15. It is cleared upon an indirect read access.

CRCEI:

CRCEI becomes a logic 1 when the calculated CRC differs from the received CRC remainder. It is cleared upon an indirect read access.

OOOFI:

OOOFI becomes a logic 1 upon a change in the OOOF context bit. It is cleared upon an indirect read access.

RAICRCI:

RAICCRCI becomes a logic 1 upon a change in the RAICCRC context bit. It is cleared upon an indirect read access.

CFEBEI:

CFEBEI becomes a logic 1 upon a change in the CFEBE context bit. It is cleared upon an indirect read access.

V52LINKI:

V52LINKI becomes a logic 1 upon a change in the V52LINK context bit. It is cleared upon an indirect read access.

IFPI:

IFPI becomes a logic 1 upon the first bit of each frame. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

ICSMFPI:

ICSMFPI becomes a logic 1 upon the first bit of each CRC sub-multiframe. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

ICMFPI:

ICMFPI becomes a logic 1 upon the first bit of each CRC multiframe. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

ISMFPI:

ISMFPI becomes a logic 1 upon the first bit of each signaling multiframe. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

Sa4I, Sa5I, Sa6I, Sa7I, Sa8I

The National Use interrupt status bits indicate if the debounced version of the individual bits has changed since the last indirect read access. A logic 1 in one of the bit positions indicates a new nibble codeword is available in the associated SaN[1:4] bits, where N is 4 through 8.

C2NCIW:

The C2NCIW bit is set to logic 1 while the framer is operating in CRC to non-CRC interworking mode. The C2NCIW bit is set to a logic zero while the framer is not operating in CRC to non-CRC interworking mode.

INF:

The INF bit is a logic 0 when basic frame alignment has been lost. The INF bit goes to a logic 1 once frame alignment has been regained.

INSMF:

The INSMF bit is a logic 0 when signaling multiframe alignment has been lost. The INSMF bit goes to a logic 1 once signaling multiframe alignment has been regained.

INCMF:

The INCMF bit is a logic 0 when CRC multiframe alignment has been lost. The INCMF bit goes to a logic 1 once CRC multiframe alignment has been regained.

OOOF:

This bit indicates the current state of the out of offline frame (OOOF) indicator. OOOF is asserted when the offline framer in the CRC multiframe find procedure is searching for frame alignment.

RAICCRC:

This bit indicates the current state of the RAI and continuous CRC indicator. RAICCRC is asserted when the remote alarm (A bit) is set to logic 1 and the CRC error (E bit) is set to logic 0 for a period of 10 ms.

CFEBE:

This bit indicates the current state of the continuous FEBE indicator. CFEBE is asserted when the CRC error (E bit) is set to logic 1 on more than 990 occasions in each second (out of 1000 possible occasions) for the last 5 consecutive seconds.

V52LINK:

This bit indicates the current state of the V5.2 link identification signal indicator. V52LINK will be asserted if 2 out of last 3 Sa7 bits are received as a logic 0.

RAI:

The RAI bit indicates the remote alarm indication (RAI) value. The RAI bit is set to logic one when the "A" bit (bit 3 in time slot 0 of the non-frame alignment signal frame) has been logic one for an interval specified by the RAIC bit. When the RAIC bit is a logic 1, RAI is set when A=1 for 4 or more consecutive intervals, and is cleared upon reception of any A=0. When the RAIC bit is a logic 0, RAI is set upon reception of any A=1, and is cleared upon reception of any A=0. The RAI output is updated every two frames.

RMAI:

The RMAI bit indicates the remote multiframe alarm indication (RMAI) value. The RMAI bit is set to logic one when the "Y" bit (bit 6 in time slot 16 in frame 0 of the signaling multiframes) has been a logic one for 3 consecutive signaling multiframes, and is cleared upon reception of any Y=0. The RMAI bit is updated every 16 frames.

AISD:

The AISD bit indicates the alarm indication signal (AIS) defect value. The AISD bit is set to logic one when the incoming data stream has a low zero-bit density for an interval specified by the AISC bit. When the AISC bit is a logic 0, AISD is asserted when 512 bit periods have been received with 2 or fewer zeros. The indication is cleared when a 512 bit period is received with 3 or more zeros. When the AISC bit is a logic 1, AISD is asserted when two consecutive 512 bit periods have been received with 2 or fewer zeros. The indication is cleared when 2 consecutive 512 bit periods are received, with each period containing 3 or more zeros. The AISD bit is updated once every 512-bit period.

TS16AISD:

The time slot 16 Alarm Indication Signal detect (TS16AISD) signal goes high to indicate that the incoming TS 16 data stream has a low zero-bit density. TS16AISD is detected when the incoming TS16 signal has 3 or less zeroes in each of 2 consecutive multi-frames. The indication is cleared when 4 or more zeros are detected in each of two consecutive multi-frame periods, or when the signaling multi-frame signal has been found, or when basic frame alignment is lost.

Si[2:1]:

The Si[1] bit contains the International bit in the last received FAS frame. The Si[2] bit contains the International bit in the last received NFAS frame (note that this does not necessarily refer to a CRC bit).

A:

The A bit position contains the Remote Alarm Indication (RAI) bit in the last received NFAS frame.

Sa[4:8]:

These bits contain the National bit values in the last received NFAS frame.

Note: The contents of this field are not updated while out of CRC multiframe.

X[3], Y, X[1], X[0]:

These bits contain the value of the Extra bits (X[3], X[1] and X[0]) and the Remote Signaling Multiframe Alarm bit (Y) in frame 0, timeslot 16 of the last received signaling multiframe.
Note: The contents of this field are not updated while out of signaling multiframe.

SaX[4:1]:

These bits contain the SaX nibble code word extracted from the sub-multiframe., where 'X' corresponds to the National bit selected by the SaSEL[2:0] bits. SaX[1] is from the first SaX bit of the sub-multiframe; SaX[4] is from the last. A change in these bit values sets the SaI[X] bit.

CRCERR[9:0]

The CRC Error holding register contains the count of CRC-4 errors that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

FER[6:0]:

The Framing Error holding register contains the count of framing bit errors that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

FEBE[9:0]:

The Far End Block Error holding register contains the count of number of zero E-bits during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

Register 0x0187: T1/E1 Framer Configuration and Status

Bit	Type	Function	Default
Bit 7	W12C	XFERI	X
Bit 6	R/W	XFERE	0
Bit 5	R/W	INTE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	AUTOUPDATE	0

AUTOUPDATE:

If this bit is logic 1, the transfer of performance counts to holding registers is initiated every 19440000 SREFCLK cycles if S77 is low or 77760000 SREFCLK cycles if S77 is high, which is nominally one second. Upon a transfer, the associated internal counters are reset to begin a new cycle of error accumulation. The T1 transmitter also sends an ANSI T1.403-formatted performance report message (PRM) on the T1 facility data link. The XFERI status bit is set to logic 1 upon completion of the transfer.

Regardless of the state of AUTOUPDATE, transfers and PRMs may be initiated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1.

INTE:

If this bit is a logic 1, the FRMR bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the FRMRI[44:29,16:1] bits is a logic 1.

XFERE:

If this bit is a logic 1, the FRMR bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

XFERI:

Subsequent to a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomous update, the XFERI status bit is set to logic 1 when the counter transfers have been completed for all 32 links. This bit is cleared upon writing a logic 1 to the bit position.

Reserved:

This bit must be set to its default value for correct operation.

Register 0x0188: T1/E1 Framer Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REGC_DI	X
Bit 4	R	REG9_AI	X
Bit 3	W12C	FRMRI[4]	X
Bit 2	W12C	FRMRI[3]	X
Bit 1	W12C	FRMRI[2]	X
Bit 0	W12C	FRMRI[1]	X

FRMRI[44:29,16:1]:

A logic 1 in these bits indicate framing events on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG9_AI:

This bit is a logic 1 if at least one bit in Register 0x0189 or 0x018A is logic 1.

REGC_DI:

This bit is a logic 1 if at least one bit in Register 0x018C or 0x018D is logic 1.

Register 0x0189: T1/E1 Framer Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[12]	X
Bit 6	W12C	FRMRI[11]	X
Bit 5	W12C	FRMRI[10]	X
Bit 4	W12C	FRMRI[9]	X
Bit 3	W12C	FRMRI[8]	X
Bit 2	W12C	FRMRI[7]	X
Bit 1	W12C	FRMRI[6]	X
Bit 0	W12C	FRMRI[5]	X

Register 0x018A: T1/E1 Framer Interrupt Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	W12C	FRMRI[16]	X
Bit 2	W12C	FRMRI[15]	X
Bit 1	W12C	FRMRI[14]	X
Bit 0	W12C	FRMRI[13]	X

Register 0x018C: T1/E1 Framer Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[36]	X
Bit 6	W12C	FRMRI[35]	X
Bit 5	W12C	FRMRI[34]	X
Bit 4	W12C	FRMRI[33]	X
Bit 3	W12C	FRMRI[32]	X
Bit 2	W12C	FRMRI[31]	X
Bit 1	W12C	FRMRI[30]	X
Bit 0	W12C	FRMRI[29]	X

Register 0x018D: T1/E1 Framer Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[44]	X
Bit 6	W12C	FRMRI[43]	X
Bit 5	W12C	FRMRI[42]	X
Bit 4	W12C	FRMRI[41]	X
Bit 3	W12C	FRMRI[40]	X
Bit 2	W12C	FRMRI[39]	X
Bit 1	W12C	FRMRI[38]	X
Bit 0	W12C	FRMRI[37]	X

10.16 System Side SBI (Scaleable Bandwidth Interconnect) Master Configuration Register

Register 0x01C0: System Side SBI Master Reset / Bus Signal Monitor

Bit	Type	Function	Default
Bit 7	R	SDC1FPA	X
Bit 6	R	SAC1FPA	X
Bit 5	R	SADA	X
Bit 4	R	SAV5A	X
Bit 3	R	SAPLA	X
Bit 2	R	SBIDET1A	X
Bit 1	R	SBIDET0A	X
Bit 0	R/W	RESET	0

When a monitored System Side SBI Bus signal makes a low to high transition, the corresponding register bit is set to logic 1. The bit will remain high until this register is read, at which point all the bits in this register (except RESET) are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

RESET:

The RESET bit forces a software reset of all the System Side SBI blocks. This will force all direct and indirect registers to their default values. When the RESET bit is set to a logic 1 the System Side SBI blocks are held reset which is also the low power state. When RESET is set to logic 0 the System Side SBI is operational. The System Side SBI blocks are operational by default.

SBIDET0A:

The SBIDET0 active, SBIDET0A, bit monitors for low to high transitions on the SBIDET0 input. SBIDET0A is set to logic 1 on a rising edge of SBIDET0, and is set to logic 0 when this register is read.

SBIDET1A:

The SBIDET1 active, SBIDET1A, bit monitors for low to high transitions on the SBIDET1 input. SBIDET1A is set to logic 1 on a rising edge of SBIDET1, and is set to logic 0 when this register is read.

SAPLA:

The SAPL active, SAPLA, bit monitors for low to high transitions on the SAPL input. SAPLA is set to logic 1 on a rising edge of SAPL, and is set to logic 0 when this register is read.

SAV5A:

The SAV5 active, SAV5A, bit monitors for low to high transitions on the SAV5 input. SAV5A is set to logic 1 on a rising edge of SAV5, and is set to logic 0 when this register is read.

SADA:

The SADATA bus active, SADA, bit monitors for low to high transitions on the least significant data bit of the System Side SBI Add bus, SADATA[0], as an indication of bus activity on the System Side SBI Add bus data and parity signals. SADA is set to logic 1 when a rising edge has been observed on SADATA[0], and is set to logic 0 when this register is read.

SAC1FPA:

The SAC1FP active, SAC1FPA, bit monitors for low to high transitions on the SAC1FP input. SAC1FPA is set to logic 1 on a rising edge of SAC1FP, and is set to logic 0 when this register is read.

SDC1FPA:

The SDC1FP active, SDC1FPA, bit monitors for low to high transitions on the SDC1FP input. SDC1FPA is set to logic 1 on a rising edge of SDC1FP, and is set to logic 0 when this register is read.

Register 0x01C1: System Side SBI Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SDC1FPMSTR	0
Bit 5	R/W	MFSDC1FP	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

MFSDC1FP:

The multiframe SDC1FP alignment bit, MFSDC1FP, enables the TE-32 for signaling multiframe alignment on the System Side SBI Drop bus. When the TE-32 is enabled to generate the SDC1FP signal via setting SC1FPMSTR to logic 1, it will generate SDC1FP either every 4 System Side SBI frames if MFSDC1FP is logic 0 or every 48 System Side SBI frames if MFSDC1FP is logic 1. MFSDC1FP must be set to logic 1 if SC1FPMSTR is logic 0, the bus is configured for 77.76MHz operation (i.e. S77 input is high) and at least one T1/E1 tributary is configured in synchronous mode (i.e INSBI SYNCH_TRIB register bit is logic 1).

SDC1FPMSTR:

The SDC1FP master mode bit, SDC1FPMSTR, enables the TE-32 to be the SDC1FP master in an System Side SBI system. Only one device per System Side SBI bus can be SDC1FP master. When SDC1FPMSTR is high the TE-32 will generate the SDC1FP pulse at a period set by the MFSDC1FP register bit. When SDC1FPMSTR is low the TE-32 will listen to the SDC1FP pulse which is generated elsewhere. SC1FPMSTR must be set to logic 0 when the system side SBI bus is configured for 77.76MHz operation (i.e. S77 input is high).

Register 0x01C2: System Side SBI Bus Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	BUSMASTER	0

BUSMASTER:

This System Side SBI Bus Master bit, BUSMASTER, enables the TE-32 to drive the System Side SBI Drop bus whenever no other System Side SBI device is driving the bus. When BUSMASTER is set to 0, the TE-32 drives the System Side SBI Drop bus only during links that are enabled for this device. During all other links or System Side SBI overhead bytes, the TE-32 will tri-state the System Side SBI Drop bus signals. When BUSMASTER is logic 1 and S77 is low, the TE-32 will drive the System Side SBI Drop bus during all links and SBI overhead bytes except when it detects other SBI devices are driving the bus when the SBIDET[1:0] signals are high. When BUSMASTER is logic 1 and S77 is high, the TE-32 will drive the SBI Drop bus during all SBI overhead bytes for the configured STS-3 (via the SSTM[1:0] configuration bits in the Bus Configuration register 0x0006); individual links will be driven only when enabled.

Register 0x01C4: System Side SBI Bus DLL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R.W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL. This register is only available when the System SBI bus is configured for 77.76MHz (i.e., S77 is set to logic 1).

ERRORE:

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, the INTB output is asserted low upon assertion of the ERROR bit of the DLL Control Status register. When ERRORE is set low, changes in the ERROR bit does not generate an interrupt.

Reserved:

The reserved bits must be set to logic 0 for correct operation.

Register 0x01C6: System Side SBI Bus DLL Tap Status

Bit	Type	Function	Default
Bit 7	R	TAP[7]	X
Bit 6	R	TAP[6]	X
Bit 5	R	TAP[5]	X
Bit 4	R	TAP[4]	X
Bit 3	R	TAP[3]	X
Bit 2	R	TAP[2]	X
Bit 1	R	TAP[1]	X
Bit 0	R	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock. This register is only available when the System SBI bus is configured for 77.76MHz (i.e., S77 is set to logic 1).

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 SREFCLK cycles for the DLL to regain lock. During this time the SBI output propagation delays may vary.

TAP[7:0]:

The tap status register bits (TAP[7:0]) specifies the delay line tap the DLL is using to generate its outgoing clock. When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is equal to 255, the DLL is using the delay line tap with maximum phase delay.

Register 0x01C7: System Side SBI Bus DLL Control Status

Bit	Type	Function	Default
Bit 7	R	SRERCLKI	X
Bit 6	R	DLLCLKI	X
Bit 5	R	ERRORI	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1		Unused	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation. This register is only available when the System SBI bus is configured for 77.76MHz (i.e., S77 is set to logic 1). Refer to Operations Section 12.14 to avoid DLL lock-up.

RUN:

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the variable delay clock and the rising edge of SREFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1. The RUN register bit is cleared only by a hardware or a software reset.

ERROR:

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. ERROR is set low when the DLL captures lock again.

When this bit is a logic 1, it is recommended the DLL be re-initialized by writing any value to the DLL Delay Tap Status register.

ERRORI:

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one and is cleared upon read.

DLLCLKI:

The reference clock event register bit DLLCLKI provides a method to monitor activity on the variable delay clock. When the internal DLLCLK changes from a logic zero to a logic one, the DLLCLKI register bit is set to logic one and cleared upon read.

In the unlikely event this bit is logic 0, the DLL shall be re-initiated by writing any value to the DLL Delay Tap Status register.

SREFCLKI:

The system clock event register bit SREFCLKI provides a method to monitor activity on the SREFCLK input clock. When the SREFCLK primary input changes from a logic zero to a logic one, the SREFCLKI register bit is set to logic one. The SREFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

10.17 System Side EXSBI (Extract Scaleable Bandwidth Interconnect) Registers

Register 0x01D0: System Side EXSBI Control

Bit	Type	Function	Default
Bit 7	R/W	APAGE	0
Bit 6	R/W	DC_RSTEN	1
Bit 5	R/W	DC_RESYNCE	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	TS_EN	0
Bit 1	R/W	SBI_PERR_EN	0
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the parity mode for the checking of the SBI parity signal, SADP. When SBI_PAR_CTL is a logic 0 parity will be even. When SBI_PAR_CTL is a logic 1 parity will be odd.

SBI_PERR_EN:

The SBI_PERR_EN bit is used to enable the SBI Parity Error interrupt generation. When SBI_PERR_EN is a logic 1 SBI parity errors will result in the assertion low of the INTB output.

TS_EN:

The TS_EN bit is used to enable the tributary to internal link mapping capability.

When TS_EN is a '0' mapping will be fixed to a one to one mapping and will not be programmable. The 1st 16 T1/E1 data streams are mapped to tributaries 1 to 16 of SPE #1 and the 2nd 16 T1/E1 data streams are mapped to tributaries 1 to 16 of SPE #2, within the SPE structure.

When TS_EN is a '1' tributary to internal link mapping is enabled and is specified by the contents of the System Side EXSBI Tributary Mapping RAM.

FIFO_UDRE:

This bit is set to enable the assertion low of the INTB output when a FIFO under-run is detected.

FIFO_OVRE:

This bit is set to enable the assertion low of the INTB output when a FIFO over-run is detected.

DC_RESYNCE:

This depth check and bus resynchronization interrupt enable bit, DC_RESYNCE, enables the generation of an interrupt when either a Depth Check error or an external resynchronization event occurs on either the SAC1FP or internal synchronization signals. When DC_RESYNCE is logic 1 the INTB output is asserted low when one of the depth check or resynchronization errors occur. When DC_RESYNCE is a logic 0 INTB will not be asserted due to these events.

Depth check events should only happen when the System Side SBI bus is misconfigured and will reset the link. SAC1FP resynchronization events will reset the entire System Side SBI bus interface and are reported by the SAC1FP_SYNCI. Internal synchronization errors should only occur during configuration and are reported by the SBIIP_SYNCI.

DC_RSTEN:

The Depth check automatic reset enable bit, DC_RSTEN, allows the System Side EXSBI to automatically reset a link if it underruns or overruns. When DC_RSTEN is a 1 the link will automatically reset when a depth check error is detected. When DC_RSTEN is a 0 the link must be reset manually when a depth check error is detected and reported via the depth check error interrupt, DC_ERRI bit in the System Side EXSBI Depth Check Interrupt Status register.

When DC_RSTEN is a logic 0, interrupts must be enabled via the DC_RESYNCE interrupt enable bit. When DC_RSTEN is a 1 and depth check interrupts are enabled via DC_RESYNCE, multiple interrupts can be expected until the link FIFO is at the correct operating level.

APAGE:

The tributary mapping and control configuration RAMs active page select bit (APAGE) controls the selection of one of two pages in the tributary mapping and control configuration RAMs to be the active page. When APAGE is set high, the configuration in page 1 of the tributary mapping and control configuration RAMs is used to associate incoming tributaries to internal links. When APAGE is set low, the configuration in page 0 of the tributary mapping and control configuration RAMs is used to associate incoming tributaries to internal links. Changes of the active page as a result of write accesses to APAGE will be synchronized to SBI multi-frame boundaries at C1FP.

Register 0x01D1: System Side EXSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	X

This register is cleared when read.

Back to back reads of this register must be at least 250 ns apart.

This Underrun interrupt register is the output of a priority encoder of the underrun history of all links. The most significant links have the highest priority and will be reported first if underruns simultaneously occur on multiple links.

If bit 0 is zero, no links have entered underrun since the last read, and all pending underrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has entered underrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently enters underrun, the reporting of the multiple underruns can prevent the reporting of underrun on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete underrun history.

FIFO_UDRI:

This bit is set when a FIFO under-run is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the System Side SBI link associated with the FIFO buffer in which the over-run was detected.

Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

Register 0x01D2: System Side EXSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_OVRI	X

This register is cleared when read.

Back to back reads of this register must be at least 250 ns apart.

This Overrun interrupt register is the output of a priority encoder of the overrun history of all links. The most significant links have the highest priority and will be reported first if overruns simultaneously occur on multiple links.

If bit 0 is zero, no links have overrun since the last read, and all pending overrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has overrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently overruns, the reporting of the multiple overruns can prevent the reporting of overruns on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete overrun history.

FIFO_OVRI:

This bit is set when a FIFO over-run is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the System Side SBI link associated with the FIFO buffer in which the over-run was detected.

Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

Register 0x01D3: System Side EXSBI Tributary RAM Indirect Access Address

Bit	Type	Function	Default
Bit 7	R/W	MAP_REG	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify which SBI tributary the Control register write or read operation will apply. TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

MAP_REG:

MAP_REG specifies whether the System Side EXSBI Tributary Mapping Registers or System Side EXSBI Tributary Control Registers are to be addressed by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '1' the System Side EXSBI Tributary Mapping Registers are addressed by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '0' the System Side EXSBI Tributary Control Registers are addressed by the SPE[1:0] and TRIB[4:0] fields.

Register 0x01D4: System Side EXSBI Tributary RAM Indirect Access Control

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	PAGE	0

PAGE:

The indirect page select bit (PAGE) selects between the two pages in the tributary mapping configuration RAMs.

RWB:

The indirect access control bit, RWB selects between a configure (write) or interrogate (read) access to the tributary mapping or control configuration RAM. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken from the System Side EXSBI Tributary Mapping Indirect Access Data Register or System Side EXSBI Tributary Control Indirect Access Data Register. Writing a logic 1 to RWB triggers an indirect read operation. The data read can be found in the System Side EXSBI Tributary Mapping Indirect Access Data Register or System Side EXSBI Tributary Control Indirect Access Data Register.

BUSY:

The indirect access status bit, BUSY reports the progress of an indirect access. BUSY is set to logic 1 when a write to this register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. If SREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x01D5: System Side EXSBI Tributary Mapping RAM Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	See Note below
Bit 5	R/W	SPE[0]	See Note below
Bit 4	R/W	LINK[4]	See Note below
Bit 3	R/W	LINK[3]	See Note below
Bit 2	R/W	LINK[2]	See Note below
Bit 1	R/W	LINK[1]	See Note below
Bit 0	R/W	LINK[0]	See Note below

LINK[4:0] and SPE[1:0]

The LINK[4:0] and SPE[1:0] fields are used to specify the internal link to SBI tributary mapping.

LINK[4:0] specifies the SBI link number within the SPE as specified by the SPE[1:0] field that should be used as the destination for data received from the SBI tributary associated with the System Side EXSBI Tributary Control and Status Register.

Note: The default mapping is straight through i.e. 1:1. Therefore, SPE1, LINK 1 will be mapped by default to SPE1, LINK 1 on the SBI side and so on up to SPE2, LINK 16.

Register 0x01D6: System Side EXSBI Tributary Control Indirect Access Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CLK_MSTR	0
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ENBL	0

ENBL:

The ENBL bit is used to enable the Tributary. Writing to the System Side EXSBI Tributary RAM Indirect Access Control Register with the ENBL bit set enables the System Side EXSBI to transmit tributary data from an SBI tributary.

If ENBL is logic 0, it is recommended the egress tributary rate be locked to CTCLK and that AIS or trunk conditioning be inserted into the data stream.

TRIB_TYP[1:0]

The TRIB_TYP[1:0] field is used to specify the characteristics of the SBI tributary as shown in Table 3.

Table 3 System Side EXSBI TRIB_TYP Encoding

TRIB_TYP	Description	CAS Enabled	Framed
00	Framed with CAS	True	True
01	Framed without CAS	False	True
10	Unframed	False	False
11	Reserved	X	X

The Reserved value for TRIB_TYP must not be used for proper operation of the TE-32.

CLK_MSTR:

The CLK_MSTR bit is used to specify whether the Extract block tributary functions as a clock master or a clock slave. When this bit is a logic 1, the TE-32 is the clock master for the selected tributary and will use the SAJUST_REQ SBI signal to speed-up or slow-down SBI slaves connected to that tributary. When this bit is a logic 0, the TE-32 is a clock slave for the selected tributary and will adapt to the incoming tributary rate.

Reserved:

These bits must be set to their default values for correct operation.

Register 0x01D7: System Side SBI Parity Error Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	TRIB[4]	X
Bit 4	R	TRIB[3]	X
Bit 3	R	TRIB[2]	X
Bit 2	R	TRIB[1]	X
Bit 1	R	TRIB[0]	X
Bit 0	R	PERRI	X

PERRI:

When set PERRI indicates that an SBI parity error has been detected. This bit is cleared when read.

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] field are used to specify the SBI tributary for which a parity error was detected. These fields are only valid only when PERRI is set.

Register 0x01D8: System Side EXSBI MIN_DEPTH for T1 and E1 Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_DEP_E1[3]	0
Bit 6	R/W	MIN_DEP_E1[2]	1
Bit 5	R/W	MIN_DEP_E1[1]	1
Bit 4	R/W	MIN_DEP_E1[0]	1
Bit 3	R/W	MIN_DEP_T1[3]	0
Bit 2	R/W	MIN_DEP_T1[2]	1
Bit 1	R/W	MIN_DEP_T1[1]	1
Bit 0	R/W	MIN_DEP_T1[0]	1

MIN_DEP_T1[3:0]:

Used to modify the MIN_DEPTH for T1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

MIN_DEP_E1[3:0]:

Used to modify the MIN_DEPTH for E1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

Register 0x01DA: System Side EXSBI T1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	0
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	0
Bit 0	R/W	MAX_THR_T1[0]	1

MAX_THR_T1[3:0]:

Used to modify the Maximum Threshold for T1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request, in clock master mode.

MIN_THR_T1[3:0]:

Used to modify the Minimum Threshold for T1 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated, in clock master mode.

Register 0x01DB: System Side EXSBI E1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E1[3]	0
Bit 6	R/W	MIN_THR_E1[2]	0
Bit 5	R/W	MIN_THR_E1[1]	1
Bit 4	R/W	MIN_THR_E1[0]	0
Bit 3	R/W	MAX_THR_E1[3]	1
Bit 2	R/W	MAX_THR_E1[2]	1
Bit 1	R/W	MAX_THR_E1[1]	0
Bit 0	R/W	MAX_THR_E1[0]	1

MAX_THR_E1[3:0]:

Used to modify the Maximum Threshold for E1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request, in clock master mode.

MIN_THR_E1[3:0]:

Used to modify the Minimum Threshold for E1 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated, in clock master mode.

Register 0x01DE: System Side EXSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	DC_ERRI	X

DC_ERRI:

This bit is set when a Depth Check error is detected. Reading this register clears this bit unless another Depth Check Interrupt is pending. Pending interrupts can occur when many links are reset simultaneously due to a reconfiguration or SBI bus resynchronization. Multiple pending interrupts can also occur on a single link when the DC_RSTEN bit is set, persisting until the link FIFO is stable.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected. Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. When an over run has not been detected the LINK field may contain an out of range link value. Values in these fields are only valid when DC_ERRI is a '1'.

Register 0x01DF: System Side EXSBI FIFO Control Register

Bit	Type	Function	Default
Bit 7	R/W	FI_EMPTY_ENBL	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	X
Bit 0	R	SAC1FP_SYNCI	X

SAC1FP_SYNCI:

This bit is set when a SAC1FP realignment has been detected. Reading this register clears this interrupt source.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected. Reading this register clears this interrupt source.

FI_EMPTY_ENBL:

If FI_EMPTY_ENBL is logic 1, no data bytes are emitted when a link FIFO empties. If FI_EMPTY_ENBL is logic 0, stuff bytes are generated when a FIFO is empty, thus causing slips. This bit is used globally to control the behavior for all T1/E1 links.

Note: This bit should be set to logic 1 for correct operation.

Reserved:

This bit must be set to logic 0 for correct operation.

10.18 System Side INSBI (Insert Scaleable Bandwidth Interconnect) Registers

Register 0x01E0: System Side INSBI Control

Bit	Type	Function	Default
Bit 7	R/W	APAGE	0
Bit 6	R/W	DC_RSTEN	1
Bit 5	R/W	DC_RESYNCE	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	TS_EN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for generation of the SBI data parity signal, SDDP. When SBI_PAR_CTL is a logic 0 parity will be even. When SBI_PAR_CTL is a logic 1 parity will be odd.

TS_EN:

The TS_EN bit is used to enable the tributary to internal link mapping capability.

When TS_EN is a '0' mapping will be fixed to a one to one mapping and will not be programmable. The 1st 16 T1/E1 data streams are mapped to tributaries 1 to 16 of SPE #1 and the 2nd 16 T1/E1 data streams are mapped to tributaries 1 to 16 of SPE #2, within the SPE structure.

When TS_EN is a '1' tributary to internal link mapping is enabled and is specified by the contents of the System Side INSBI Tributary Mapping RAM.

FIFO_UDRE:

The FIFO_UDRE bit is used to enable/disable the generation of an interrupt when a FIFO underrun is detected. When FIFO_UDRE is a logic 1, the INTB output is asserted low when the SBI Add bus FIFO underruns.

FIFO_OVRE:

The FIFO_OVRE bit is used to enable/disable the generation of an interrupt when a FIFO overrun is detected. When FIFO_OVRE is a logic 1, the INTB output is asserted low when the SBI Add bus FIFO overruns.

DC_RESYNCE:

This DC_RESYNCE bit enables the generation of an interrupt when either a Depth Check error or an external resynchronization event occurs on either the SDC1FP or internal synchronization signals. When DC_RESYNCE is a 1 interrupts will be generated when one of the depth check or resynchronization errors occur. When DC_RESYNCE is a logic 0, the INTB output will not be asserted due to these events.

Depth check events should only happen when the System Side SBI bus is misconfigured and will reset the link. SDC1FP resynchronization events will reset the entire System Side SBI bus interface and are reported by the SDC1FP_SYNCI bit. Internal synchronization errors should only occur during configuration and are reported by the SBIIP_SYNCI.

DC_RSTEN:

The Depth check automatic reset enable bit, DC_RSTEN, allows the System Interface INSBI to automatically reset a link if it underruns or overruns. When DC_RSTEN is a 1 the link will automatically reset when a depth check error is detected. When DC_RSTEN is a 0 the link must be reset manually when a depth check error is detected and reported via the depth check error interrupt, DC_ERRI bit in the System Interface INSBI Depth Check Interrupt Status register.

When DC_RSTEN is a logic 0 interrupts must be enabled via the DC_RESYNCE interrupt enable bit. When DC_RSTEN is a 1 and depth check interrupts are enabled via DC_RESYNCE, multiple interrupts can be expected until the link FIFO is at the correct operating level.

APAGE:

The tributary mapping and control configuration RAMs active page select bit (APAGE) controls the selection of one of two pages in the tributary mapping and control configuration RAMs to be the active page. When APAGE is set high, the configuration in page 1 of the tributary mapping and control configuration RAMs is used to associate incoming tributaries to internal links. When APAGE is set low, the configuration in page 0 of the tributary mapping and control configuration RAMs is used to associate incoming tributaries to internal links. Changes of the active page as a result of write accesses to APAGE will be synchronized to SBI multi-frame boundaries at C1FP.

Reserved:

This bit must be set to logic 0 for correct operation.

Register 0x01E1: System Side INSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	X

This interrupt status register is cleared when read.

If an underrun condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

Back to back reads of this register must be at least 250 ns apart.

This Underrun interrupt register is the output of a priority encoder of the underrun history of all links. The most significant links have the highest priority and will be reported first if underruns simultaneously occur on multiple links.

If bit 0 is zero, no links have entered underrun since the last read, and all pending underrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has entered underrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently enters underrun, the reporting of the multiple underruns can prevent the reporting of underrun on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete underrun history.

FIFO_UDRI:

This bit is set when a FIFO underrun is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the underrun was detected. Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. LINK[4:0] and SPE[1:0] are invalid unless FIFO_UDRI is set.

Register 0x01E2: System Side INSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_OVRI	X

This interrupt status register is cleared when read.

If an overflow condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

Back to back reads of this register must be at least 250 ns apart.

This Overrun interrupt register is the output of a priority encoder of the overrun history of all links. The most significant links have the highest priority and will be reported first if overruns simultaneously occur on multiple links.

If bit 0 is zero, no links have overrun since the last read, and all pending overrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has overrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently overruns, the reporting of the multiple overruns can prevent the reporting of overruns on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete overrun history.

FIFO_OVRI:

This bit is set when a FIFO overrun is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the overrun was detected. Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. LINK[4:0] and SPE[1:0] are invalid unless FIFO_OVRI is set.

Register 0x01E3: System Side INSBI Tributary Register Indirect Access Address

Bit	Type	Function	Default
Bit 7	R/W	MAP_REG	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify for which SBI tributary the Control register write or read operation will apply. TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

MAP_REG:

MAP_REG specifies whether the System Side INSBI Tributary Mapping Registers or System Side INSBI Tributary Control Registers are to be addressed by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '1' the System Side INSBI Tributary Mapping Registers are addressed by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '0' the System Side INSBI Tributary Control Registers are addressed by the SPE[1:0] and TRIB[4:0] fields.

Register 0x01E4: System Side INSBI Tributary Register Indirect Access Control

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	PAGE	0

PAGE:

The indirect page select bit (PAGE) selects between the two pages in the tributary mapping RAMs.

RWB:

The indirect access control bit, RWB selects between a configure (write) or interrogate (read) access to the tributary mapping or control configuration RAM. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken from the System Side INSBI Tributary Mapping Indirect Access Data Register or System Side INSBI Tributary Control Indirect Access Data Register. Writing a logic 1 to RWB triggers an indirect read operation. The data read can be found in the System Side INSBI Tributary Mapping Indirect Access Data Register or System Side INSBI Tributary Control Indirect Access Data Register

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to this register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. The BUSY bit is asserted for up to 4.32us after a page switch. If SREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x01E5: System Side INSBI Tributary Mapping RAM Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	See Note below
Bit 5	R/W	SPE[0]	See Note below
Bit 4	R/W	LINK[4]	See Note below
Bit 3	R/W	LINK[3]	See Note below
Bit 2	R/W	LINK[2]	See Note below
Bit 1	R/W	LINK[1]	See Note below
Bit 0	R/W	LINK[0]	See Note below

LINK[4:0] and SPE[1:0]

The LINK[4:0] and SPE[1:0] fields are used to specify the internal link to SBI tributary mapping.

LINK[4:0] specifies the SBI link number within the SPE as specified by the SPE[1:0] field that should be used as the source for data transmitted to the SBI tributary associated with the System Side INSBI Tributary Control and Status Register.

Note: The default mapping is straight through i.e. 1:1. Therefore, SPE1, LINK 1 will be mapped by default to SPE1, LINK 1 on the SBI side and so on up to SPE2, LINK 16.

Register 0x01E6: System Side INSBI Tributary Control Indirect Access Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SYNCH_TRIB	0
Bit 4		Unused	X
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ENBL	0

ENBL:

The ENBL bit is used to enable the Tributary. Writing to the System Side INSBI Tributary Register Indirect Access Control Register with the ENBL bit set to a logic 1 enables the System Side INSBI to take tributary data from an internal link and transmit that data to the SBI tributary mapped to that link.

If ENBL is logic 0, the System Interface SBI DROP bus is high impedance.

TRIB_TYP[1:0]:

The TRIB_TYP[1:0] field is used to specify the characteristics of the SBI tributary as shown in Table 4.

Table 4 System Interface INSBI TRIB_TYP Encoding

TRIB_TYP	Description	CAS Enabled	Framed
00	Framed with CAS	True	True
01	Framed without CAS	False	True
10	Unframed	False	False
11	Reserved	X	X

The Reserved value for TRIB_TYP must not be used for proper operation of the TE-32.

SYNCH_TRIB:

The Synchronous Tributary mode select bit, SYNCH_TRIB, sets the tributary to operate in synchronous mode on the System Interface SBI DROP bus. When SYNCH_TRIB is logic 1, the selected framed tributary DS0s or timeslots are locked in a fixed location within the SBI structure. In this mode the, corresponding T1/E1 framer must be operating synchronously to the System Interface SBI bus; therefore, the tributary must pass through the elastic store with its output timed to the System Interface SBI bus clock, SREFCLK. When SYNCH_TRIB is set to logic 1, the RX-SBI-ELST SYNCSBI bit for the tributary must also be set to logic 1 to ensure the elastic store is timed from the System Interface SBI bus clock. When SYNCH_TRIB is logic 0, the tributary is allowed to float within the SBI structure and there is no need for the elastic store.

Note: This bit must be set before the tributary is enabled and should only be changed when the tributary is disabled.

Reserved:

This bit must be set to its default value for correct operation.

Register 0x01E7: System Side INSBI MIN_DEPTH for T1 and E1 Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_DEP_E1[3]	0
Bit 6	R/W	MIN_DEP_E1[2]	1
Bit 5	R/W	MIN_DEP_E1[1]	1
Bit 4	R/W	MIN_DEP_E1[0]	1
Bit 3	R/W	MIN_DEP_T1[3]	0
Bit 2	R/W	MIN_DEP_T1[2]	1
Bit 1	R/W	MIN_DEP_T1[1]	1
Bit 0	R/W	MIN_DEP_T1[0]	1

MIN_DEP_E1[3:0]:

Used to modify the MIN_DEPTH for E1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

MIN_DEP_T1[3:0]:

Used to modify the MIN_DEPTH for T1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

Register 0x01E9: System Side INSBI T1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	1
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	1
Bit 0	R/W	MAX_THR_T1[0]	0

MIN_THR_T1[3:0]:

Used to modify the Minimum Threshold for T1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed in clock master mode.

MAX_THR_T1[3:0]:

Used to modify the Maximum Threshold for T1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification in clock master mode.

MAX_THR_T1 should be set to 1100 to guarantee correct operation.

Register 0x01EA: System Side INSBI E1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E1[3]	0
Bit 6	R/W	MIN_THR_E1[2]	0
Bit 5	R/W	MIN_THR_E1[1]	1
Bit 4	R/W	MIN_THR_E1[0]	0
Bit 3	R/W	MAX_THR_E1[3]	1
Bit 2	R/W	MAX_THR_E1[2]	1
Bit 1	R/W	MAX_THR_E1[1]	1
Bit 0	R/W	MAX_THR_E1[0]	0

MIN_THR_E1[3:0]:

Used to modify the Minimum Threshold for E1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed in clock master mode.

MIN_THR_E1 should be set to 0110 to guarantee correct operation.

MAX_THR_E1[3:0]:

Used to modify the Maximum Threshold for E1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification in clock master mode.

MAX_THR_E1 should be set to 1100 to guarantee correct operation.

Register 0x01F1: System Side INSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	DC_ERRI	X

DC_ERRI:

This bit is set when a Depth Check error is detected. Reading this register clears this bit unless another Depth Check Interrupt is pending. Pending interrupts can occur when many links are reset simultaneously due to a reconfiguration or SBI bus resynchronization. Multiple pending interrupts can also occur on a single link when the DC_RSTEN bit is set, persisting until the link FIFO is stable.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected. Legal values for LINK[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'. When an over run has not been detected the LINK field may contain an out of range link value. Values in these fields are only valid when DCR_INTI is a '1'.

Register 0x01F2: System Side INSBI External ReSynch Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	X
Bit 0	R	SDC1FP_SYNCI	X

SDC1FP_SYNCI:

This bit is set when a SDC1FP realignment has been detected. Reading this register clears this interrupt source.

When operating with a 77.76MHz bus (i.e. the S77 input is high), this SDC1FP_SYNCI may not be asserted if the new alignment is within four SREFCLK cycles of the old alignment.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected. Reading this register clears this interrupt source.

10.19 Full Featured T1/E1 Pattern Generators and Receivers

Each of the six (N = 0 to 5) T1/E1 pattern generator and receiver pairs may be associated with a specific tributary via the T1/E1 PRGD Tributary Select registers (0x0042 to 0x0047).

The pattern receiver analyzes the data after the frame alignment block, but before the elastic store so it is not subject to frame slips.

The pattern generator inserts its data after the TPCC (thus overwrites signaling, DMW, trunk conditioning) and before the frame insertion. To transmit unframed patterns the FDIS context bit of the transmitter must be logic 1.

10.20 T1/E1 Pattern Generator and Detector Registers

Register 0x0500 + 0x20*N: T1/E1 Pattern Generator and Detector Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

PDR[1:0]:

The PDR[1:0] bits select the content of the four pattern detector register to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

QRSS:

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDAT stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PS:

The PS bit selects the generated pattern. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

RINV:

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted.

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 6 or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTOSYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 0x0501 + 0x20*N: T1/E1 Pattern Generator and Detector Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the INTB output is asserted low if the SYNCI bit is logic 1.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the INTB output is asserted low if the BEI bit is logic 1.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the INTB output is asserted low if the XFERI bit is logic 1.

SYNCV:

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing a logic 1 to the E1T1_PRBS bit of the Global Performance Monitor Update register. XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0x0502 + 0x20*N: T1/E1 Pattern Generator and Detector Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]:

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 0x0503 + 0x20*N: T1/E1 Pattern Generator and Detector Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]:

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 0x0504 + 0x20*N: T1/E1 Pattern Generator and Detector Error Insertion

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT:

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]:

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in the following table:

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

Register 0x0508 + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 0x0509 + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 0x050A + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 0x050B + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]:

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written. When a repetitive pattern is transmitted, PI[31], the MSB, contains the first bit transmitted, PI[0], the LSB, contains the last bit transmitted.

Note: The PI[31:0] value has no effect on the pattern detection. If a repetitive pattern is selected, the receiver will synchronize to any bit sequence that repeats with the programmed periodicity.

Register 0x050C + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 0x050D + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 0x050E + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 0x050F + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]:

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the PRGD Control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0]. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval.

Note: Bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval.

The PRGD Pattern Detect registers for a single tributary are updated by writing to any one of the associated Pattern Detect registers when the PDR[1:0] bits are 11. Alternatively, the Pattern Detect registers are updated globally with all other TE-32 counter registers by writing to the Global Performance Monitor Update register (address 0x0007) with the E1T1_PRBS bit set to logic 1.

Registers 0x0510 + 0x20*N: Generator Controller Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Generator Controller.

Reserved:

The Reserved bit must be logic 0 for normal operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TE-32 is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the generator when set to a logic 1. DS0s must also be enabled individually.

Registers 0x0511 + 0x20*N: Generator Controller µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 0x0512 + 0x20*N: Generator Controller Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register allows the µP to access the internal Generator Controller registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal Generator Controller register is requested; when R/WB is set to a logic 0, a write to the internal RPSC register is requested.

This register address is only valid when the IND bit of the associated Generator Controller Configuration register is logic 1.

Registers 0x0513 + 0x20*N: Generator Controller Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains either the data to be written into the internal Generator Controller registers when a write request is initiated or the data read from the internal Generator Controller registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The functions are allocated within the registers shown in Table 5.

Table 5 Generator Controller Indirect Register Map

Addr	Register
20H	DDS Control byte for Timeslot 0
21H	DDS Control byte for Channel 1/Timeslot 1
22H	DDS Control byte for Channel 2/Timeslot 2
•	•
•	•
37H	DDS Control byte for Channel 23/Timeslot 23
38H	DDS Control byte for Channel 24/Timeslot 24
39H	DDS Control byte for Timeslot 25
•	•
•	•
3EH	DDS Control byte for Timeslot 30
3FH	DDS Control byte for Timeslot 31
40H	Bit Enable byte for Timeslot 0
41H	Bit Enable byte for Channel 1/Timeslot 1
42H	Bit Enable byte for Channel 2/Timeslot 2
• •	• •
57H	Bit Enable byte for Channel 23/Timeslot 23
58H	Bit Enable byte for Channel 24/Timeslot 24
59H	Bit Enable byte for Timeslot 25
• •	• •
5EH	Bit Enable byte for Timeslot 30
5FH	Bit Enable byte for Timeslot 31

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

Table 6 Generator Controller Indirect Registers 0x20-0x3F DDS Control byte

Bit	Type	Function	Default
Bit 7	R/W	Unused	X
Bit 6	R/W	Unused	X
Bit 5	R/W	Unused	X
Bit 4	R/W	SIXBITS	X
Bit 3	R/W	DDS4	X
Bit 2	R/W	DDS3	X
Bit 1	R/W	DDS2	X
Bit 0	R/W	DDS1	X

SIXBITS:

When the SIXBITS bit is set to a logic 1, the DDS pattern is placed in the second through the seventh bit of the DS0. When the SIXBITS bit is set to a logic 0, the DDS pattern is placed in the first through the seventh bit of the DS0.

DDS4:

When set to logic 1, 01000000 is continuously repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

DDS3:

When set to logic 1, 00110010 is continuously repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

This bit supercedes DDS4.

DDS2:

When set to logic 1, 100 octets of 01111110 followed by 100 octets of 00000000 are repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

This bit supercedes DDS3 and DDS4.

DDS1:

When set to logic 1, 100 octets of 11111111 followed by 100 octets of 00000000 are repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

This bit supercedes DDS2, DDS3 and DDS4.

Table 7 Generator Controller Indirect Registers 0x40-0x5F Bit Enable byte

Bit	Type	Function	Default
Bit 7	R/W	BE[7]	X
Bit 6	R/W	BE[6]	X
Bit 5	R/W	BE[5]	X
Bit 4	R/W	BE[4]	X
Bit 3	R/W	BE[3]	X
Bit 2	R/W	BE[2]	X
Bit 1	R/W	BE[1]	X
Bit 0	R/W	BE[0]	X

BE[7:0]:

These bits determine which individual bits are used by the Pattern Generator. If a BE bit is logic one, the corresponding bit in the T1/E1 tributary is expected to contain a bit in the sequence being analyzed.

These bits only control PRBS and fixed pattern insertion; the DDS codes occupy an entire DS0 regardless of the state of these bits.

BE[7] corresponds to the first bit transmitted. All channels/timeslots must be programmed before the PCCE bit is set to logic 1.

Registers 0x0514 + 0x20*N: Receiver Controller Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Receiver Controller.

Reserved:

The Reserved bit must be logic 0 for normal operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TE-32 is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the Pattern Receiver when set to a logic 1. DS0s must also be enabled individually.

Registers 0x0515 + 0x20*N: Receiver Controller µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 0x0516 + 0x20*N: Receiver Controller Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register allows the µP to access the internal Receiver Controller registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal Receiver Controller register is requested; when R/WB is set to a logic 0, an write to the internal Receiver Controller register is requested.

This register address is only valid when the IND bit of the associated Receiver Controller Configuration register is logic 1.

Registers 0x0517 + 0x20*N: Receiver Controller Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains either the data to be written into the internal Receiver Controller registers when a write request is initiated or the data read from the internal Receiver Controller registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The functions are allocated within the registers shown in Table 5:

Table 8 Receiver Controller Indirect Register Map

Addr	Register
40H	Bit Enable byte for Timeslot 0
41H	Bit Enable byte for Channel 1/Timeslot 1
42H	Bit Enable byte for Channel 2/Timeslot 2
• •	• •
57H	Bit Enable byte for Channel 23/Timeslot 23
58H	Bit Enable byte for Channel 24/Timeslot 24
59H	Bit Enable byte for Timeslot 25
• •	• •
5EH	Bit Enable byte for Timeslot 30
5FH	Bit Enable byte for Timeslot 31

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

Table 9 Receiver Controller Indirect Registers 0x40-0x5F Bit Enable byte

Bit	Type	Function	Default
Bit 7	R/W	BE[7]	X
Bit 6	R/W	BE[6]	X
Bit 5	R/W	BE[5]	X
Bit 4	R/W	BE[4]	X
Bit 3	R/W	BE[3]	X
Bit 2	R/W	BE[2]	X
Bit 1	R/W	BE[1]	X
Bit 0	R/W	BE[0]	X

BE[7:0]:

These bits determine whether individual bits are overwritten by the Pattern Receiver. If a BE bit is logic one, the corresponding bit in the T1/E1 tributary is replaced by a bit in the sequence generated by the Pattern Generator.

BE[7] corresponds to the first bit transmitted. All channels/timeslots must be programmed before the PCCE bit is set to logic 1.

10.21 Line Side SBI Master Configuration Registers

Register 0x0700: Line Side SBI Master Reset

Bit	Type	Function	Default
Bit 7	R/W	SBIBUS	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold the entire line side SBI Interface in a reset condition. When RESET is a logic 1, the line side SBI Interface will be held in a reset state which is also a low power state. This will force all registers to their default state with the exception of this register, which is not reset when this RESET bit is a logic 1. While in reset the clocks can not be guaranteed accurate or existing. When RESET is a logic 0 the line side SBI Interface is in normal operating mode. The line side SBI Interface is by default in the operational state. This register is only reset by the hardware device reset and not by this RESET register bit.

SBIBUS:

SBIBUS enables the line side SBI interface. This bit must set to logic 1 for correct operation.

Reserved:

These bits must be set to their default values for correct operation.

Register 0x0702: Line Side SBI Master Egress Configuration

Bit	Type	Function	Default
Bit 7	R/W	LATOHEN	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DLOOP2	0
Bit 4	R/W	DLOOP1	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	LAOP	0
Bit 0	R/W	Reserved	0

This register configures the TE-32 functionality that are related to the egress data stream.

LAOP:

The LAOP bit controls the parity placed on the egress parity signal LADP. When LAOP is set to logic 0, the parity of outgoing data streams LADATA[7:0], LAPL and LAV5 together with LADP is even. When LAOP is set to logic 1, the parity is odd.

DLOOP1:

DLOOP1 (and DLOOP2) must be set to logic 1 when the DLOOP bit (Register 0x070A: Line Side SBI Master Loopback Control) is set to logic 1. This enables diagnostic loopback at the line side SBI bus interface, where the entire egress SBI bus is looped back to the ingress data path.

DLOOP2:

DLOOP2 (and DLOOP1) must be set to logic 1 when the DLOOP bit (Register 0x070A: Line Side SBI Master Loopback Control) is set to logic 1. This enables diagnostic loopback at the line side SBI bus interface, where the entire egress SBI bus is looped back to the ingress data path.

LAOHEN

The line side SBI Add bus Overhead Enable register bit, LAOHEN, controls whether the Line Add bus is driven during the overhead columns of the SBI frame. When LAOHEN is set to 1, the line side SBI Add bus signals, LADP, LAPL, LADATA, and LAV5, are all driven during the overhead columns. When LAOHEN is logic 0, the Line Add bus signals are held in tristate during the overhead columns (the LADDOE bit, when asserted, has precedence over this bit).

Reserved:

These bits must be set to their default values for correct operation.

Register 0x0703: Line Side SBI Master Ingress Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	DLOOP3	0

This register configures the TE-32 functionality that are related to the ingress data stream.

DLOOP3:

DLOOP3 must be set to logic 1 when the DLOOP bit (Register 0x070A: Line Side SBI Master Loopback Control) is set to logic 1. This enables diagnostic loopback at the line side SBI bus interface, where the entire egress SBI bus is looped back to the ingress data path.

Reserved:

These bits must be set to their default values for correct operation.

Register 0x0704: Line Side DLOOP Enable

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	DLOOP5	0
Bit 2	R/W	DLOOP4	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

These bits must be set to zero for correct operation.

DLOOP4:

DLOOP4 (and DLOOP5) must be set to logic 1 when the DLOOP bit (Register 0x070A: Line Side SBI Master Loopback Control) is set to logic 1. This enables diagnostic loopback at the line side SBI bus interface, where the entire egress SBI bus is looped back to the ingress data path.

DLOOP5:

DLOOP5 (and DLOOP4) must be set to logic 1 when the DLOOP bit (Register 0x070A: Line Side SBI Master Loopback Control) is set to logic 1. This enables diagnostic loopback at the line side SBI bus interface, where the entire egress SBI bus is looped back to the ingress data path.

Register 0x070A: Line Side SBI Master Loopback Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	DLOOP	0
Bit 0	R/W	Reserved	0

DLOOP:

The DLOOP bit enables a diagnostic loopback at the line side SBI bus interface. When DLOOP is a logic 1 then entire egress SBI bus is looped back to the ingress data path. When DLOOP is a logic 0, no diagnostic loopback will be performed.

Note: DLOOP1, DLOOP2 (in register 0x0702), DLOOP3 (in register 0x0703), DLOOP4 and DLOOP5 (in register 0x0704), must also be set to logic 1 to enable diagnostic loopback.

Reserved:

These bits must be logic 0 for correct operation of the TE-32.

Register 0x070B: Line Side SBI Bus Signal Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LAC1FPA	X
Bit 4	R	LDDA	X
Bit 3	R	LDV5A	X
Bit 2	R	LDPLA	X
Bit 1		Unused	X
Bit 0	R	LDC1FPA	X

When a monitored line side SBI Bus signal makes a low to high transition, the corresponding register bit is set to logic 1. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

LDC1FPA:

The LDC1FP active, LDC1FPA, bit monitors for low to high transitions on the LDC1FP input. LDC1FPA is set to logic 1 on a rising edge of LDC1FP, and is set to logic 0 when this register is read.

LDPLA:

The LDPL active, LDPLA, bit monitors for low to high transitions on the LDPL input. LDPLA is set to logic 1 on a rising edge of LDPL, and is set to logic 0 when this register is read.

LDV5A:

The LDV5 active, LDV5A, bit monitors for low to high transitions on the LDV5 input. LDV5A is set to logic 1 on a rising edge of LDV5, and is set to logic 0 when this register is read.

LDDA:

The LDDATA bus active, LDDA, bit monitors for low to high transitions on the LDDATA[7:0] bus. LDDA is set to logic 1 when a rising edge has been observed on each signal on the LDDATA [7:0] bus with no intervening reads of this register. LDDA is set to logic 0 when this register is read.

LAC1FPA:

The LAC1FPI active, LAC1FPA, bit monitors for low to high transitions on the LAC1FPI input. LAC1FPA is set to logic 1 on a rising edge of LAC1FPI, and is set to logic 0 when this register is read.

Register 0x0900, 0x0902, 0x0904, 0x0906, 0x0908, 0x090A, 0x090C, 0x0940, 0x0942, 0x0944, 0x0946, 0x0948, 0x094A, 0x094C: T1/E1 Mode Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	T1/E1B	1
Bit 5	R/W	Reserved	0
Bit 4	R	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

These bits must remain in their default state for correct operation.

T1/E1B:

The T1/E1B configures the device for T1 or E1 operation. If T1/E1B is logic 1, T1 mode is selected. If T1/E1B is logic 0, E1 mode is selected.

Note: All T1/E1 configuration registers must be programmed to either T1 or E1 operation. Mixed-modes are not supported.

10.22 Line Side INSBI Registers

Register 0x09C0: Line Side INSBI Control Register

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DC_ENBL	1
Bit 5	R/W	DC_INT_EN	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

Reserved:

The reserved bits must be set to the default for correct operation.

FIFO_UDRE:

The FIFO_UDRE bit is used to enable/disable the generation of an interrupt when a FIFO underrun is detected.

When FIFO_UDRE is a ‘0’ underrun interrupt generation is disabled.

When FIFO_UDRE is a ‘1’ underrun interrupt generation is enabled.

FIFO_OVRE:

The FIFO_OVRE bit is used to enable/disable the generation of an interrupt when a FIFO overrun is detected.

When FIFO_OVRE is a ‘0’ overrun interrupt generation is disabled.

When FIFO_OVRE is a ‘1’ overrun interrupt generation is enabled.

DC_INT_EN:

This bit is set to enable the generation of an interrupt when either of the following events occurs:

A Depth Check error (DC_ERRI).

An external resynchronization event occurs on either the LAC1FPI (LAC1FP_SYNCI) or the internal SBI bus (SBIIP_SYNCI) signals.

DC_ENBL:

This bit enables the Depth Check logic. When asserted high the depth checker logic will periodically monitor the Data/Framing FIFO Depth and compare it against the write and read pointers. If there is a discrepancy the tributary is reset by the depth checker.

Register 0x09C1: Line Side INSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	X

This interrupt status register is cleared when read.

If an underrun condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

Back to back reads of this register must be at least 250 ns apart.

This Underrun interrupt register is the output of a priority encoder of the underrun history of all links. The most significant links have the highest priority and will be reported first if underruns simultaneously occur on multiple links.

If bit 0 is zero, no links have entered underrun since the last read, and all pending underrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has entered underrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently enters underrun, the reporting of the multiple underruns can prevent the reporting of underrun on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete underrun history.

FIFO_UDRI:

This bit is set when a FIFO underrun is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the underrun was detected. Legal values for LINK[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'. LINK[4:0] and SPE[1:0] are invalid unless FIFO_UDRI is set.

Register 0x09C2: Line Side INSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_OVRI	X

This interrupt status register is cleared when read.

If an overflow condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

Back to back reads of this register must be at least 250 ns apart.

This Overrun interrupt register is the output of a priority encoder of the overrun history of all links. The most significant links have the highest priority and will be reported first if overruns simultaneously occur on multiple links.

If bit 0 is zero, no links have overrun since the last read, and all pending overrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has overrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently overruns, the reporting of the multiple overruns can prevent the reporting of overruns on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete overrun history.

FIFO_OVRI:

This bit is set when a FIFO overrun is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the overrun was detected. Legal values for LINK[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'. LINK[4:0] and SPE[1:0] are invalid unless FIFO_OVRI is set.

Register 0x09C3: Line Side INSBI Tributary Register Indirect Access Address Register

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify for which tributary the Mapping or Control RAM write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'.

Reserved:

This bit must always be written as a logic 0 for correct operation.

Register 0x09C4: Line Side INSBI Tributary Register Indirect Access Control Register

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	Reserved	0

Reserved:

This bit must be logic 0 for correct operation.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary mapping or control configuration RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Line Side INSBI Tributary Control Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Line Side INSBI Tributary Control Indirect Access Data Register.

HST_ADDR_ERR:

When set following a host read, this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to the Line Side INSBI Tributary Register Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. The BUSY bit is asserted for up to 4.32us after a page switch.

Register 0x09C6: Line Side INSBI Tributary Control Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ENBL	0

Reserved:

All reserved bits, except Bit 2, must be set to the default for correct operation. Reserved Bit 2 must be set to logic 1 for correct operation.

ENBL:

The ENBL bit is used to enable the tributary. Writing to the Line Side INSBI Tributary Register Indirect Access Control with the ENBL bit set enables the Line Side EXSBI to take tributary data from an T1/E1 link and transmit that data to the tributary mapped to that link.

Note: Any write to a Tributary Control RAM location for a tributary will generate a configuration reset on that tributary, irrespective of whether the data written to the tributary control RAM location is unchanged from the previous value.

Register 0x09C7: Line Side INSBI MIN_DEPTH for T1 and E1 Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_DEP_E1[3]	0
Bit 6	R/W	MIN_DEP_E1[2]	1
Bit 5	R/W	MIN_DEP_E1[1]	1
Bit 4	R/W	MIN_DEP_E1[0]	1
Bit 3	R/W	MIN_DEP_T1[3]	0
Bit 2	R/W	MIN_DEP_T1[2]	1
Bit 1	R/W	MIN_DEP_T1[1]	1
Bit 0	R/W	MIN_DEP_T1[0]	1

MIN_DEP_E1[3:0]:

Used to modify the MIN_DEPTH for E1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

MIN_DEP_T1[3:0]:

Used to modify the MIN_DEPTH for T1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

Register 0x09C9: Line Side INSBI T1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	1
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	1
Bit 0	R/W	MAX_THR_T1[0]	0

MIN_THR_T1[3:0]:

Used to modify the Minimum Threshold for T1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed in clock master mode.

MAX_THR_T1[3:0]:

Used to modify the Maximum Threshold for T1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification in clock master mode.

MAX_THR_T1 should be set to 1100 to guarantee correct operation.

Register 0x09CA: Line Side INSBI E1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E1[3]	0
Bit 6	R/W	MIN_THR_E1[2]	0
Bit 5	R/W	MIN_THR_E1[1]	1
Bit 4	R/W	MIN_THR_E1[0]	0
Bit 3	R/W	MAX_THR_E1[3]	1
Bit 2	R/W	MAX_THR_E1[2]	1
Bit 1	R/W	MAX_THR_E1[1]	1
Bit 0	R/W	MAX_THR_E1[0]	0

MIN_THR_E1[3:0]:

Used to modify the Minimum Threshold for E1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed in clock master mode

MIN_THR_E1 should be set to 0110 to guarantee correct operation.

MAX_THR_E1[3:0]:

Used to modify the Maximum Threshold for E1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification in clock master mode.

MAX_THR_E1 should be set to 1100 to guarantee correct operation.

Register 0x09D1: Line Side INSBI Depth Check Interrupt Status Register

Bit	Type	Function	Default
Bit 7	R	SPE[1]	0
Bit 6	R	SPE[0]	1
Bit 5	R	TRIB[4]	0
Bit 4	R	TRIB[3]	0
Bit 3	R	TRIB[2]	0
Bit 2	R	TRIB[1]	0
Bit 1	R	TRIB[0]	0
Bit 0	R	DCR_INTI	0

DCR_INTI:

This bit is set when a Depth Check error is detected. This bit is cleared to 0 when read.

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected.

Legal values for TRIB[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'.

When a depth check error has not been detected the TRIB field may contain an out of range link value.

Values in these fields should only be looked at when DCR_INTI is a '1'.

This register will contain the interrupt status even if the corresponding interrupt enable is not set.

Register 0x09D2: Line Side INSBI Master Interrupt Status Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	X
Bit 0	R	LAC1FP_SYNCI	X

LAC1FP_SYNCI:

This bit is set when a LAC1FPI realignment has been detected. Reading this register clears this interrupt source.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected. Reading this register clears this interrupt source.

10.23 Line Side EXSBI Registers

Register 0x09E0: Line Side EXSBI Control Register

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DC_ENBL	1
Bit 5	R/W	DC_INT_EN	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	SBI_PERR_EN	0
Bit 0	R/W	SBI_PAR_CTL	1

Reserved:

The reserved bits must be set to their defaults for correct operation.

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for checking of the SBI parity signal, LDDP. When SBI_PAR_CTL is a logic 0 parity will be even. When SBI_PAR_CTL is logic 1 parity will be odd

SBI_PERR_EN:

The SBI_PERR_EN bit is used to enable the SBI Parity Error interrupt generation. When SBI_PERR_EN is a logic 1 SBI parity errors will result in the assertion low of the INTB output.

FIFO_UDRE:

This bit is set to enable the generation of an interrupt when a FIFO under-run is detected.

FIFO_OVRE:

This bit is set to enable the generation of an interrupt when a FIFO over-run is detected.

DC_INT_EN:

This bit is set to enable the generation of an interrupt when either of the following events occurs.

A Depth Check error (DC_ERRI).

An external resynchronization event occurs on either the LDC1FP (LDC1FP_SYNCI) or the internal SBI bus (SBIIP_SYNCI) signals.

DC_ENBL:

This bit enables the Depth Check Resets. The depth checker logic will periodically monitor the FIFO Depth and compare it against the write and read pointers. When DC_ENBL is asserted high and there is a discrepancy the tributary is reset by the depth checker. When DC_ENBL is low the tributary reset is suppressed but the Depth Check Error is reported via the Depth Check Interrupt Reason Register.

Register 0x09E1: Line Side EXSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	X

This register is cleared when read.

Back to back reads of this register must be at least 250 ns apart.

This Underrun interrupt register is the output of a priority encoder of the underrun history of all links. The most significant links have the highest priority and will be reported first if underruns simultaneously occur on multiple links.

If bit 0 is zero, no links have entered underrun since the last read, and all pending underrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has entered underrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently enters underrun, the reporting of the multiple underruns can prevent the reporting of underrun on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete underrun history.

FIFO_UDRI:

This bit is set when a FIFO underrun is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the underrun was detected. Legal values for LINK[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'. LINK[4:0] and SPE[1:0] are invalid unless FIFO_UDRI is set.

Register 0x09E2: Line Side EXSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_OVRI	X

This register is cleared when read.

Back to back reads of this register must be at least 250 ns apart.

This Overrun interrupt register is the output of a priority encoder of the overrun history of all links. The most significant links have the highest priority and will be reported first if overruns simultaneously occur on multiple links.

If bit 0 is zero, no links have overrun since the last read, and all pending overrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has overrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note: If a tributary is misbehaving so that it frequently overruns, the reporting of the multiple overruns can prevent the reporting of overruns on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete overrun history.

FIFO_OVRI:

This bit is set when a FIFO overrun is detected. This bit is cleared when read.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the overrun was detected. Legal values for LINK[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'. LINK[4:0] and SPE[1:0] are invalid unless FIFO_OVRI is set.

Register 0x09E3: Line Side EXSBI Tributary RAM Indirect Access Address Register

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify to which tributary the Mapping or Control register write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'.

Reserved:

This bit must be set to logic 0 for correct operation.

Register 0x09E4: Line Side EXSBI Tributary RAM Indirect Access Control Register

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R	HST_ADDR_ERR	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	Reserved	0

Reserved:

This bit must be set to logic 0 for correct operation.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary mapping or control configuration RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Line Side EXSBI Tributary Control Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Line Side EXSBI Tributary Control Indirect Access Data Register.

HST_ADDR_ERR:

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. For E1 out of range tributaries are 1,22 to 1,28; 2,22 to 2,28 and 3,22 to 3,28.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to the Line Side EXSBI Tributary Register Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence.

Register 0x09E6: Line Side EXSBI Tributary Control RAM Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ENBL	0

Reserved:

These bits must be logic 0 for correct operation.

ENBL:

The ENBL bit is used to enable the Tributary. Writing to the Line Side EXSBI Tributary RAM Indirect Access Control Register with the ENBL bit set enables the System Interface EXSBI to take tributary data from an SBI tributary and transmit that data to the T1/E1 link mapped to that tributary.

Note: Any write to a Tributary Control register for a tributary will generate a configuration reset on that tributary, irrespective of whether the data written to the tributary control register is unchanged from the previous value.

Register 0x09E7: Line Side SBI Parity Error Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	TRIB[4]	X
Bit 4	R	TRIB[3]	X
Bit 3	R	TRIB[2]	X
Bit 2	R	TRIB[1]	X
Bit 1	R	TRIB[0]	X
Bit 0	R	PERRI	X

PERRI:

When set PERRI indicates that an SBI parity error has been detected. This bit is cleared when read.

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] field are used to specify the SBI tributary for which a parity error was detected. These fields are only valid only when PERRI is set.

Register 0x09E8: Line Side EXSBI MIN_DEPTH for T1 and E1 Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_DEP_E1[3]	0
Bit 6	R/W	MIN_DEP_E1[2]	1
Bit 5	R/W	MIN_DEP_E1[1]	1
Bit 4	R/W	MIN_DEP_E1[0]	1
Bit 3	R/W	MIN_DEP_T1[3]	0
Bit 2	R/W	MIN_DEP_T1[2]	1
Bit 1	R/W	MIN_DEP_T1[1]	1
Bit 0	R/W	MIN_DEP_T1[0]	1

MIN_DEP_T1[3:0]:

Used to modify the MIN_DEPTH for T1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

MIN_DEP_E1[3:0]:

Used to modify the MIN_DEPTH for E1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

Register 0x09EA: Line Side EXSBI T1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	0
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	0
Bit 0	R/W	MAX_THR_T1[0]	1

MAX_THR_T1[3:0]:

Used to modify the Maximum Threshold for T1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request, in clock master mode.

MIN_THR_T1[3:0]:

Used to modify the Minimum Threshold for T1 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated, in clock master mode.

Register 0x09EB: Line Side EXSBI E1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E1[3]	0
Bit 6	R/W	MIN_THR_E1[2]	0
Bit 5	R/W	MIN_THR_E1[1]	1
Bit 4	R/W	MIN_THR_E1[0]	0
Bit 3	R/W	MAX_THR_E1[3]	1
Bit 2	R/W	MAX_THR_E1[2]	1
Bit 1	R/W	MAX_THR_E1[1]	0
Bit 0	R/W	MAX_THR_E1[0]	1

MAX_THR_E1[3:0]:

Used to modify the Maximum Threshold for E1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request, in clock master mode.

MIN_THR_E1[3:0]:

Used to modify the Minimum Threshold for E1 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated, in clock master mode.

Register 0x09EE: Line Side EXSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	DC_ERRI	X

DC_ERRI:

This bit is set when a Depth Check error is detected. Reading this register clears this bit unless another Depth Check Interrupt is pending. Pending interrupts can occur when many links are reset simultaneously due to a reconfiguration or SBI bus resynchronization. Multiple pending interrupts can also occur on a single link when the DC_RSTEN bit is set, persisting until the link FIFO is stable.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected. Legal values for LINK[4:0] are b'00001' through b'10000'. Legal values for SPE[1:0] are b'01' through b'10'. When an over run has not been detected the LINK field may contain an out of range link value. Values in these fields are only valid when DC_ERRI is a '1'.

Register 0x09EF: Line Side EXSBI FIFO Control Register

Bit	Type	Function	Default
Bit 7	R/W	FI_EMPTY_ENBL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	X
Bit 0	R	LDC1FP_SYNCI	X

LDC1FP_SYNCI:

This bit is set when a LDC1FP realignment has been detected. Reading this register clears this interrupt source.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected. Reading this register clears this interrupt source.

FI_EMPTY_ENBL:

This bit must be logic 1 for correct operation of line side SBI bus. Setting it prevents FIFO underflows. If this bit is logic 0, tributary bits may be lost or corrupted.

Register 0x0D00, 0x0D01, 0x0D02, 0x0D03, 0x0D04, 0x0D05, 0x0D06, 0x0D20, 0x0D21, 0x0D22, 0x0D23, 0x0D24, 0x0D25, 0x0D26: T1/E1 Mode Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	T1/E1B	1
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

Reserved bits must be written to default values for correct operation.

T1/E1B:

The T1/E1B configures the device for T1 or E1 operation. If T1/E1B is logic 1, T1 mode is selected. If T1/E1B is logic 0, E1 mode is selected.

Note: All T1/E1 configuration registers must be programmed to either T1 or E1 operation. Mixed-modes are not supported.

Register 0x0D80, 0x0D81, 0x0D82, 0x0D83, 0x0D84, 0x0D85, 0x0D86, 0x0DA0, 0x0DA1, 0x0DA2, 0x0DA3, 0x0DA4, 0x0DA5, 0x0DA6: T1/E1 Mode Configuration 3

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	T1/E1B	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

These bits must remain at their default values for correct operation.

T1/E1B:

The T1/E1B configures the device for T1 or E1 operation. If T1/E1B is logic 1, T1 mode is selected. If T1/E1B is logic 0, E1 mode is selected.

Note: All T1/E1 configuration registers must be programmed to either T1 or E1 operation. Mixed-modes are not supported.

Register 0x0E00 - 0x0E011, 0x0E20 - 0x0E31: T1/E1 Mode Configuration 4

Tributary Address Map:

SPE	Trib	Register	Trib	Register	Trib	Register
1	1	0xE00	8	0xE08	15	0xE10
1	2	0xE01	9	0xE09	16	0xE11
1	3	0xE02	10	0xE0A		
1	4	0xE03	11	0xE0B		
1	5	0xE04	12	0xE0C		
1	6	0xE05	13	0xE0D		
1	7	0xE06	14	0xE0E		
2	1	0xE20	8	0xE28	15	0xE30
2	2	0xE21	9	0xE29	16	0xE31
2	3	0xE22	10	0xE2A		
2	4	0xE23	11	0xE2B		
2	5	0xE24	12	0xE2C		
2	6	0xE25	13	0xE2D		
2	7	0xE26	14	0xE2E		

Bit	Type	Function	Default
Bit 7	R/W	T1/E1B	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	ETT	0
Bit 0	R/W	Reserved	0

Reserved:

Reserved bits must be written to default values for correct operation.

ETT:

The Egress Transparent Tributary control bit, ETT, allows a tributary to be passed transparently from System side SBI ADD bus to the Line side SBI ADD bus. When the ETT is set to logic 1 the tributary from the System side SBI will bypass the entire egress data path and be output on the Line side SBI bus.

T1/E1B:

The T1/E1B configures the device for T1 or E1 operation. If T1/E1B is logic 1, T1 mode is selected. If T1/E1B is logic 0, E1 mode is selected.

Note: All T1/E1 configuration registers must be programmed to either T1 or E1 operation. Mixed-modes are not supported. Only Registers 0x0E00 – 0x0E06 and 0x0E20 – 0x0E26 need configuring. The T1/E1B bit in registers 0x0E08 – 0x0E11 and 0x0E28 – 0x0E31 are read only.

11 Test Features Description

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Notes on Register Bits:

1) Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2) Writeable register bits are not initialized upon reset unless otherwise noted.

Register 0x1000: Master Test Register

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to select TE-32 test features.

Reserved:

These bits must be logic 0 for correct operation.

HIZIO:

The HIZIO bit controls the tri-state modes of the output pins of the TE-32. While the HIZIO bit is a logic 1, all output pins of the TE-32, except the data bus, are held in a high-impedance state. The microprocessor interface is still active.

HIZDATA:

The HIZDATA bit controls the tri-state modes of the TE-32. While the HIZIO bit is a logic 1, all output pins of the TE-32, except the data bus, are held in a high-impedance state. While the HIZDATA bit is a logic 1, the data bus is held in a high-impedance state which inhibits microprocessor read cycles.

11.1 JTAG Test Port

The TE-32 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 10 Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 11 Identification Register

Length	32 bits
Version number	0x2
Part Number	0x8316
Manufacturer's identification code	0x0CD
Device identification	0x283160CD

The boundary scan register is made up of 302 boundary scan cells, divided into input observation (IN_CELL), output (OUT_CELL) and bi-directional (IO_CELL) cells. These cells are detailed in the following pages. The first 32 cells form the ID code register and carry the code 283160CDH. The boundary scan chain order is presented in Table 12.

Table 12 Boundary Scan Register

Pin/ Enable	Bit #	Cell Type	Id Bit	Pin/ Enable	Bit #	Cell Type	Id Bit
SDC1FP_MVID_1	0	IO_CELL	-	OEB_D_3	151	OUT_CELL	-
OEB_SDC1FP_MVID_1	1	OUT_CELL	-	D_4	152	IO_CELL	-
SBIACT_MVID_2	2	OUT_CELL	-	OEB_D_4	153	OUT_CELL	-
OEB_SBIACT_MVID_2	3	OUT_CELL	-	D_5	154	IO_CELL	-

Pin/ Enable	Bit #	Cell Type	Id Bit	Pin/ Enable	Bit #	Cell Type	Id Bit
SAJUST_REQ_MVID_3	4	OUT_CELL	-	OEB_D_5	155	OUT_CELL	-
OEB_SAJUST_REQ_MVID_3	5	OUT_CELL	-	D_6	156	IO_CELL	-
SDDATA_0_MVID_4	6	OUT_CELL	-	OEB_D_6	157	OUT_CELL	-
OEB_SDDATA_0_MVID_4	7	OUT_CELL	-	D_7	158	IO_CELL	-
SDDATA_1	8	OUT_CELL	-	OEB_D_7	159	OUT_CELL	-
OEB_SDDATA_1	9	OUT_CELL	-	ALE	160	IN_CELL	-
SDDATA_2	10	OUT_CELL	-	RSTB	161	IN_CELL	-
OEB_SDDATA_2	11	OUT_CELL	-	A_0	162	IN_CELL	-
SDDATA_3	12	OUT_CELL	-	A_1	163	IN_CELL	-
OEB_SDDATA_3	13	OUT_CELL	-	A_2	164	IN_CELL	-
SDDATA_4_MVID_5	14	OUT_CELL	-	A_3	165	IN_CELL	-
OEB_SDDATA_4_MVID_5	15	OUT_CELL	-	A_4	166	IN_CELL	-
SDDATA_5_MVID_6	16	OUT_CELL	-	A_5	167	IN_CELL	-
OEB_SDDATA_5_MVID_6	17	OUT_CELL	-	A_6	168	IN_CELL	-
SDDATA_6_MVID_7	18	OUT_CELL	-	A_7	169	IN_CELL	-
OEB_SDDATA_6_MVID_7	19	OUT_CELL	-	A_8	170	IN_CELL	-
SDDATA_7_MVID_8	20	OUT_CELL	-	A_9	171	IN_CELL	-
OEB_SDDATA_7_MVID_8	21	OUT_CELL	-	A_10	172	IN_CELL	-
SDDP	22	OUT_CELL	-	A_11	173	IN_CELL	-
OEB_SDDP	23	OUT_CELL	-	A_12	174	IN_CELL	-
SDPL	24	OUT_CELL	-	WRB	175	IN_CELL	-
OEB_SDPL	25	OUT_CELL	-	RDB	176	IN_CELL	-
SDV5	26	OUT_CELL	-	CSB	177	IN_CELL	-
OEB_SDV5	27	OUT_CELL	-	LAV5	178	OUT_CELL	-
Unused	28	OUT_CELL	-	OEB_LAV5	179	OUT_CELL	-
Unused	29	OUT_CELL	-	Unused	180	OUT_CELL	-
Unused	30	OUT_CELL	-	Unused	181	OUT_CELL	-
Unused	31	OUT_CELL	-	LADP	182	OUT_CELL	-
Unused	32	OUT_CELL	-	OEB_LADP	183	OUT_CELL	-
Unused	33	OUT_CELL	-	LADATA_0	184	OUT_CELL	-
Unused	34	OUT_CELL	-	OEB_LADATA_0	185	OUT_CELL	-
Unused	35	OUT_CELL	-	LADATA_1	186	OUT_CELL	-
Unused	36	OUT_CELL	-	OEB_LADATA_1	187	OUT_CELL	-
Unused	37	OUT_CELL	-	LADATA_2	188	OUT_CELL	-

Pin/ Enable	Bit #	Cell Type	Id Bit	Pin/ Enable	Bit #	Cell Type	Id Bit
Unused	38	OUT_CELL	-	OEB_LADATA_2	189	OUT_CELL	-
Unused	39	OUT_CELL	-	LADATA_3	190	OUT_CELL	-
Unused	40	OUT_CELL	-	OEB_LADATA_3	191	OUT_CELL	-
Unused	41	OUT_CELL	-	LADATA_4	192	OUT_CELL	-
SREFCLK	42	IN_CELL	-	OEB_LADATA_4	193	OUT_CELL	-
MVED_1	43	IN_CELL	-	LADATA_5	194	OUT_CELL	-
MVED_2	44	IN_CELL	-	OEB_LADATA_5	195	OUT_CELL	-
S77_MVED_3	45	IN_CELL	-	LADATA_6	196	OUT_CELL	-
SAC1FP_MVED_4	46	IN_CELL	-	OEB_LADATA_6	197	OUT_CELL	-
SADATA_0	47	IN_CELL	-	LADATA_7	198	OUT_CELL	-
SADATA_1	48	IN_CELL	-	OEB_LADATA_7	199	OUT_CELL	-
SADATA_2	49	IN_CELL	-	LAPL	200	OUT_CELL	-
SADATA_3_MVED_5	50	IN_CELL	-	OEB_LAPL	201	OUT_CELL	-
SADATA_4_MVED_6	51	IN_CELL	-	LAC1FPO	202	OUT_CELL	-
SADATA_5_MVED_7	52	IN_CELL	-	OEB_LAC1FPO	203	OUT_CELL	-
SADATA_6_MVED_8	53	IN_CELL	-	LAC1FPI	204	IN_CELL	-
SADATA_7	54	IN_CELL	-	Logic 0	205	IN_CELL	-
SADP	55	IN_CELL	-	Logic 0	206	IN_CELL	-
SAPL	56	IN_CELL	-	Logic 0	207	IN_CELL	-
SAV5	57	IN_CELL	-	Logic 0	208	IN_CELL	-
SBIDET_0	58	IN_CELL	-	Logic 0	209	IN_CELL	-
SBIDET_1	59	IN_CELL	-	Logic 0	210	IN_CELL	-
Logic 0	60	IN_CELL	-	Logic 0	211	IN_CELL	-
TS0ID	61	OUT_CELL	-	Logic 0	212	IN_CELL	-
OEB_TS0ID	62	OUT_CELL	-	LDPL	213	IN_CELL	-
Logic 0	63	IN_CELL	-	LDV5	214	IN_CELL	-
Logic 0	64	IN_CELL	-	Logic 0	215	IN_CELL	-
Logic 0	65	IN_CELL	-	LDC1FP	216	IN_CELL	-
CCSID_1	66	OUT_CELL	-	LDDP	217	IN_CELL	-
OEB_CCSID_1	67	OUT_CELL	-	LDDATA_0	218	IN_CELL	-
CCSID_2	68	OUT_CELL	-	LDDATA_1	219	IN_CELL	-
OEB_CCSID_2	69	OUT_CELL	-	LDDATA_2	220	IN_CELL	-
CCSID_3	70	OUT_CELL	-	LDDATA_3	221	IN_CELL	-
OEB_CCSID_3	71	OUT_CELL	-	LDDATA_4	222	IN_CELL	-
CASID_1	72	OUT_CELL	-	LDDATA_5	223	IN_CELL	-
OEB_CASID_1	73	OUT_CELL	-	LDDATA_6	224	IN_CELL	-
CASID_2	74	OUT_CELL	-	LDDATA_7	225	IN_CELL	-
OEB_CASID_2	75	OUT_CELL	-	Logic 0	226	IN_CELL	-
CASID_3	76	OUT_CELL	-	LREFCLK	227	IN_CELL	-

Pin/ Enable	Bit #	Cell Type	Id Bit	Pin/ Enable	Bit #	Cell Type	Id Bit
OEB_CASID_3	77	OUT_CELL	-	Unused	228	OUT_CELL	-
CASID_4	78	OUT_CELL	-	Unused	229	OUT_CELL	-
OEB_CASID_4	79	OUT_CELL	-	Unused	230	OUT_CELL	-
Unused	80	OUT_CELL	-	Unused	231	OUT_CELL	-
Unused	81	OUT_CELL	-	Unused	232	OUT_CELL	-
Unused	82	OUT_CELL	-	Unused	233	OUT_CELL	-
Unused	83	OUT_CELL	-	Logic 0	234	IN_CELL	-
Unused	84	OUT_CELL	-	Logic 0	235	IN_CELL	-
Unused	85	OUT_CELL	-	Logic 0	236	IN_CELL	-
CASID_5	86	OUT_CELL	-	Logic 0	237	IN_CELL	-
OEB_CASID_5	87	OUT_CELL	-	Unused	238	OUT_CELL	-
CASID_6	88	OUT_CELL	-	Unused	239	OUT_CELL	-
OEB_CASID_6	89	OUT_CELL	-	Unused	240	OUT_CELL	-
CASID_7	90	OUT_CELL	-	Unused	241	OUT_CELL	-
OEB_CASID_7	91	OUT_CELL	-	Unused	242	OUT_CELL	-
CASID_8	92	OUT_CELL	-	Unused	243	OUT_CELL	-
OEB_CASID_8	93	OUT_CELL	-	Logic 0	244	IN_CELL	-
Unused	94	OUT_CELL	-	Logic 0	245	IN_CELL	-
Unused	95	OUT_CELL	-	Logic 0	246	IN_CELL	-
Unused	96	OUT_CELL	-	Logic 0	247	IN_CELL	-
Unused	97	OUT_CELL	-	Unused	248	OUT_CELL	-
Unused	98	OUT_CELL	-	Unused	249	OUT_CELL	-
Unused	99	OUT_CELL	-	Unused	250	OUT_CELL	-
Unused	100	OUT_CELL	-	Unused	251	OUT_CELL	-
Unused	101	OUT_CELL	-	Unused	252	OUT_CELL	-
Unused	102	OUT_CELL	-	Unused	253	OUT_CELL	-
Unused	103	OUT_CELL	-	Logic 0	254	IN_CELL	-
Unused	104	OUT_CELL	-	Logic 0	255	IN_CELL	-
Unused	105	OUT_CELL	-	Logic 0	256	IN_CELL	-
Unused	106	OUT_CELL	-	Logic 0	257	IN_CELL	-
Unused	107	OUT_CELL	-	Unused	258	OUT_CELL	-
Unused	108	OUT_CELL	-	Unused	259	OUT_CELL	-
Unused	109	OUT_CELL	-	Unused	260	OUT_CELL	-
Unused	110	OUT_CELL	-	Unused	261	OUT_CELL	-
Unused	111	OUT_CELL	-	Unused	262	OUT_CELL	-
Unused	112	OUT_CELL	-	Unused	263	OUT_CELL	-
Unused	113	OUT_CELL	-	Unused	264	OUT_CELL	-
CTCLK	114	IN_CELL	-	Unused	265	OUT_CELL	-
CCSED_1	115	IN_CELL	-	Unused	266	OUT_CELL	-

Pin/ Enable	Bit #	Cell Type	Id Bit	Pin/ Enable	Bit #	Cell Type	Id Bit
CCSED_2	116	IN_CELL	-	Unused	267	OUT_CELL	-
CCSED_3	117	IN_CELL	-	Logic 0	268	IN_CELL	-
CASED_1	118	IN_CELL	-	Logic 0	269	IN_CELL	-
CASED_2	119	IN_CELL	-	Unused	270	OUT_CELL	1
CASED_3	120	IN_CELL	-	Unused	271	OUT_CELL	0
CASED_4	121	IN_CELL	-	Unused	272	OUT_CELL	1
Logic 0	122	IN_CELL	-	Unused	273	OUT_CELL	1
Logic 0	123	IN_CELL	-	Unused	274	OUT_CELL	0
Logic 0	124	IN_CELL	-	Unused	275	OUT_CELL	0
CASED_5	125	IN_CELL	-	Unused	276	OUT_CELL	1
CASED_6	126	IN_CELL	-	Unused	277	OUT_CELL	1
CASED_7	127	IN_CELL	-	Unused	278	OUT_CELL	0
CASED_8	128	IN_CELL	-	Unused	279	OUT_CELL	0
Logic 0	129	IN_CELL	-	Logic 0	280	IN_CELL	0
Logic 0	130	IN_CELL	-	Logic 0	281	IN_CELL	0
Logic 0	131	IN_CELL	-	Unused	282	OUT_CELL	0
Logic 0	132	IN_CELL	-	Unused	283	OUT_CELL	1
Logic 0	133	IN_CELL	-	Unused	284	OUT_CELL	1
Logic 0	134	IN_CELL	-	Unused	285	OUT_CELL	0
Logic 0	135	IN_CELL	-	Unused	286	OUT_CELL	1
Logic 0	136	IN_CELL	-	Unused	287	OUT_CELL	0
Logic 0	137	IN_CELL	-	Unused	288	OUT_CELL	0
Logic 0	138	IN_CELL	-	Unused	289	OUT_CELL	0
CMVFPB	139	IN_CELL	-	Unused	290	OUT_CELL	1
CMVFPC	140	IN_CELL	-	Unused	291	OUT_CELL	1
CMV8MCLK	141	IN_CELL	-	Logic 0	292	IN_CELL	0
INTB	142	OUT_CELL	-	Logic 0	293	IN_CELL	0
OEB_INTB	143	OUT_CELL	-	Unused	294	OUT_CELL	0
D_0	144	IO_CELL	-	Unused	295	OUT_CELL	0
OEB_D_0	145	OUT_CELL	-	Unused	296	OUT_CELL	0
D_1	146	IO_CELL	-	Unused	297	OUT_CELL	1
OEB_D_1	147	OUT_CELL	-	Unused	298	OUT_CELL	0
D_2	148	IO_CELL	-	Unused	299	OUT_CELL	0
OEB_D_2	149	OUT_CELL	-	Logic 0	300	IN_CELL	0
D_3	150	IO_CELL	-	Logic 0	301	IN_CELL	0

NOTES:

1. Register bit 301 is the first bit of the scan chain (closest to TDI).
2. Enable cell OEB_pinname, sets ball pinname to high-impedance when set high.
3. IN_CELL's labeled "Logic 0" will always capture 0, since they are permanently tied to VSS.

12 Operation

12.1 Line Side SBI Initialization

The Line Side SBI Interface is enabled for normal operation by setting SBIBUS register bit in register 0x0700 to logic 1. In addition, reserved bit 4 in registers 0x0003, 0x0004 and 0x0005 must be set to logic 1.

12.2 Clock and Frame Synchronization Constraints

It should be noted that LREFCLK, SREFCLK and CTCLK are specified for standard oscillators. Discontinuities to these clocks while transmitting and receiving data may cause error and framing or error events within any or all the tributaries.

Depending on the modes of operation utilized, some coordination between LREFCLK, SREFCLK, and SDC1FP is required.

12.2.1 SBI Buses Both 19.44 MHz

The rising and falling edges of LREFCLK must be aligned with a tolerance of +/- 5ns to the corresponding edges of SREFCLK.

When Transparent Tributaries (TTs) are supported on the egress datapath, the SAC1FP pulse must be precisely 13 SREFCLK cycles before the LAC1FPI pulse.

12.2.2 77.76 MHz System Side SBI Bus and 19.44 MHz Line Side SBI Bus

The rising edge of LREFCLK must be aligned with a tolerance of +/- 4ns to the rising edge of SREFCLK.

For reliable operation, the STM-1s used within the SBI bus must be aligned to LREFCLK. To this end, one may manipulate the SSTM[1:0] register bits and the position of the SDC1FP pulses. Table 13 summarizes the combinations. See Figure 15 for the functional timing diagram.

Table 13 77.76 MHz System Side SBI to 19.44 MHz Line Side SBI Alignment Options

SSTM[1:0]	SREFCLK Cycles SDC1FP sampling edge leads LREFCLK rising edge
00	1
01	2
10	3
11	0

As alternate formulation, if SSTM[1:0] was converted to its decimal equivalent, one would have to satisfy the constraint:

(SSTM + 1) mod 4 = Clock Cycles SDC1FP leads LREFCLK.

Note:

1. Transparent Tributaries are not supported in this mode.
2. SDC1FP must be generated from an external source.

The 77.76 MHz System Side SBI to 19.44 MHz Line Side SBI timing constraints are described in more detail in the following example (Figure 14 and Figure 15):

Figure 14 77.76 MHz System Side SBI to 19.44 MHz Line Side SBI example

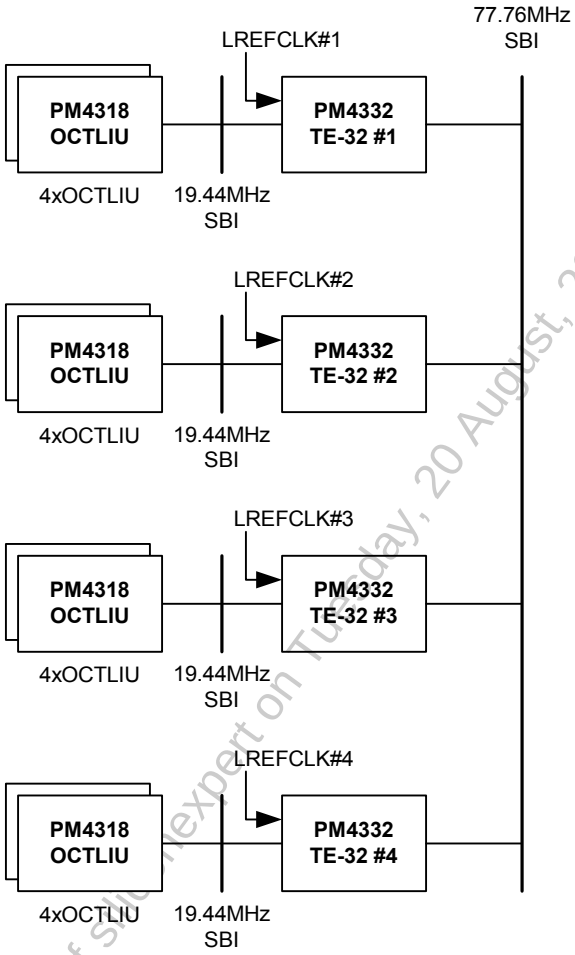
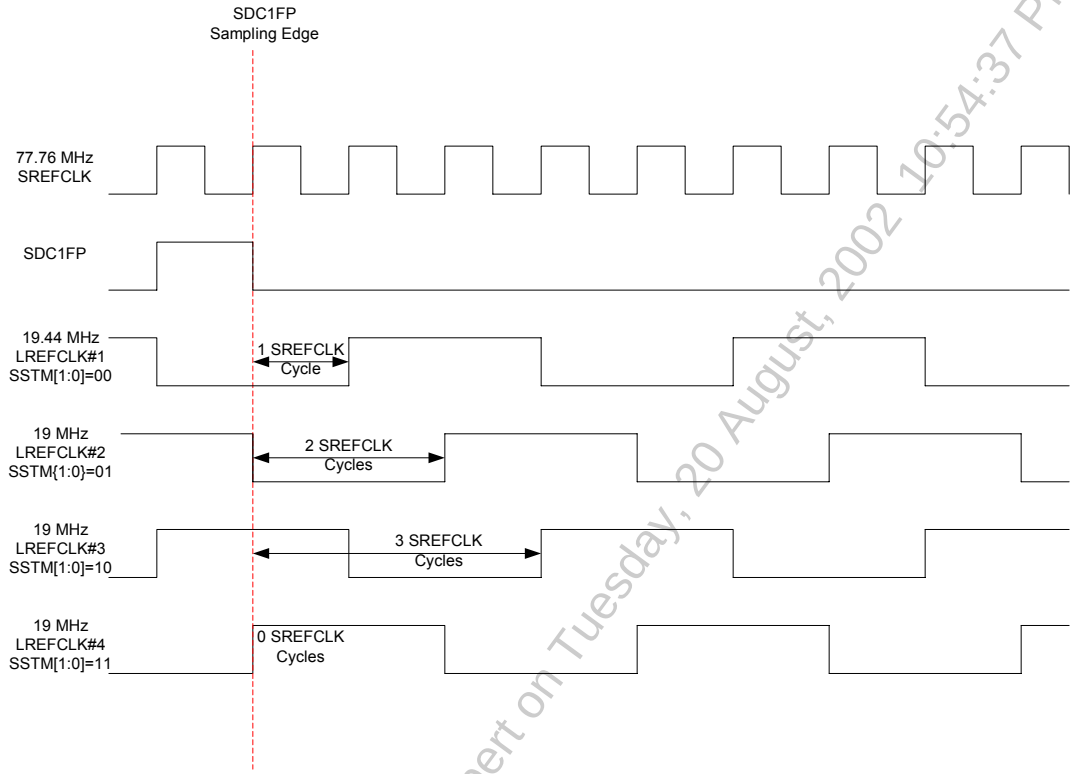


Figure 15 77.76 MHz System Side SBI to 19.44 MHz Line Side SBI timing diagram



12.3 SLC®96

The following is a comprehensive discussion of the roles and responsibilities of TE-32 and external logic in the support of the SLC®96 standard, Bellcore TR-TSY-000008. While the TE-32 handles most of the protocol functions, some external processing is required, especially of the datalink transported in the Fs bits.

12.3.1 Transmit

While the TE-32 supports transmission of AIS and the Yellow alarm, and supports signaling insertion, it is the responsibility of external logic to generate all F-bits. This means valid Ft and Fs bits as well as the datalink. To pass the F-bits transparently, the FDIS context bit must be set to logic 1 through the T1/E1 Transmitter Indirect Channel Data registers.

The TE-32 can insert robbed bit signaling. For the TE-32 to insert the signaling into the correct frames (6^{th} and 12^{th}), it must know the multiframe alignment consistent with the encoding of the F-bits. Therefore, it is imperative a multiframe indication is provided by the system interface. For the SBI interface (which must be used to implement SLC-96), the PPSSSSFR octets (those following V5) communicate multiframe alignment, signaling and the F-bits. The TRIB_TYP[1:0] bits of the EXSBI Tributary Control Indirect Access Data register should be set to "00" to configure the tributary to "Framed with CAS".

Because the F-bits are being sourced from the system interface, controlled frame slips must be avoided, if the TX-ELST is being used, to maintain superframe integrity. The T1/E1 transmit clock must be referenced to CTCLK. For SBI, CTCLK must be frequency locked to SREFCLK. Two alternate configurations for SBI avoid the need for the TX-ELST: the transmit clock is slaved to the data rate at the system interface or the TE-32 acts as a timing master using the AJUST_REQ output to set the data rate.

Insertion of nine state signaling is straight forward. A sixteen bit encoding (i.e. ABCD) is used regardless of whether the signaling is inserted from the system interface or via register access through the T1/E1 Transmit Per-Channel Controller. The ABCD state is sampled every 24 frames. The "AB" values are inserted into the first superframe and the "CD" values are inserted into the second. Thus, if toggling A or B bits are required, it is sufficient that A ≠ C or B ≠ D, respectively.

12.3.2 Receive

The T1 framer will determine frame alignment within 13ms if it is programmed to frame to SLC®96 (i.e. ESF=0, FMS[1:0]=10) and is provided with valid SLC®96 frame overhead. The framer is tolerant to the existence of the data link. Once in frame, only the Ft bits are used to determine loss of frame and for monitoring framing bit errors.

The presence of Yellow, Red, and AIS Carrier Fail Alarms is detected and integrated in accordance with the specifications defined in Bellcore TR-TSY-000191.

The datalink is not terminated within the TE-32. Instead, it is provided on either the SBI for external processing. Because the tributary may be subject to controlled frame slips, the external logic should be tolerant to the infrequent duplication or deletion of bits within the F-bit sequence.

Signaling is terminated elegantly. The signaling for two consecutive superframes is captured as an aggregate presented as ABCD, with "CD" being the second set of A and B signaling bits. The ABCD bits are treated as cohesive state that is subject to debouncing (if enabled single bit errors will be filtered) and freezing. The four bits are available on the SBI Drop interface, and through the SIGX Indirect Channel Data Register registers. A ≠ C is an indication that the A bit is toggling. B ≠ D is an indication that the B bit is toggling. (Note, the following signaling states are all equivalent; they all represent toggling A and B bits: 0110, 1100, 0011, 1001.) An interrupt on change of signaling will only occur if the collected ABCD state changes, but not just from toggling A or B bits.

12.4 Servicing Interrupts

The TE-32 will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

Read the bits of the TE-32 Master Interrupt Source register (0x0010) to identify which of the three interrupt registers (0x0011, 0x0012 or 0x0015) needs to be read to identify the interrupt.

Read the bits of the second level Master Interrupt Source register to identify the interrupt source.

Service the interrupt by reading the register containing the interrupt status bit that is asserted.

If the INTB pin is still logic 0, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

Elastic Store Interrupts

Following device initialization the Elastic Store (ELST) W12C (write logic 1 to clear) "Reserved" register bits must be cleared. This will prevent the SLPI[44:29,16:1] interrupts from being blocked and the interrupt service routine from locking up.

For the T1/E1 Receive H-MVIP Elastic Store refer to registers 0x0086, 0x0087, 0x008A-0x008E.

For the T1/E1 Receive SBI Elastic Store refer to registers 0x00A6, 0x00A7, 0x00AA-0x00AE.

For the T1/E1 Transmit Elastic Store refer to registers 0x00C6, 0x00C7, 0x00CA-0x00CE.

12.5 Using the Performance Monitoring Features

The T1/E1 PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval is very small (less than 0.001%).

An accumulation interval is initiated by writing to one of the PMON event counter register addresses or by writing to the Global PMON Update register. After initiating an accumulation interval, 3.5 recovered clock periods must be allowed to elapse to permit the PMON counter values to be properly transferred before the PMON registers may be read.

The odds of any one of the T1/E1 counters saturating during a one second sampling interval go up as the bit error rate (BER) increases. At some point, the probability of counter saturation reaches 50%. This point varies, depending upon the framing format and the type of event being counted. The BER at which the probability of counter saturation reaches 50% is shown for various counters in Table 14 for E1 mode, and in Table 15 for T1 mode.

Table 14 PMON Counter Saturation Limits (E1 mode)

Counter	BER
FER	4.0×10^{-3}
CRCE	cannot saturate
FEBE	cannot saturate

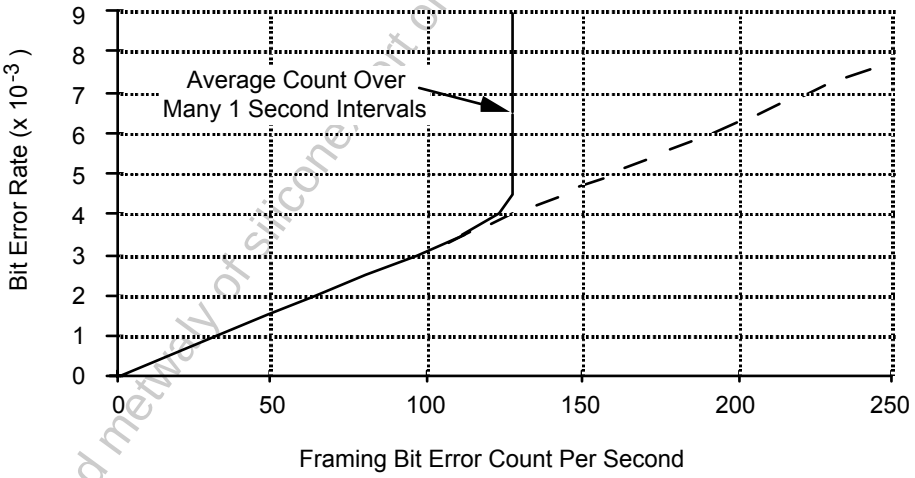
Table 15 PMON Counter Saturation Limits (T1 mode)

Counter	Format	BER
FER	SF	1.6×10^{-3}
	ESF	6.4×10^{-2}
CRCE	SF	1.28×10^{-1}
	ESF	cannot saturate

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. The following figures show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above 10^{-3}, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

Figure 16 illustrates the expected count values for a range of Bit Error Ratios in E1 mode.

Figure 16 FER Count vs. BER (E1 mode)



Since the maximum number of CRC sub-multiframes that can occur in one second is 1000, the 10-bit FEBE and CRCE counters cannot saturate in one second. Despite this, there is not a linear relationship between BER and CRC-4 block errors due to the nature of the CRC-4 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per sub-multiframe, so the number of CRC-4 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-4 error is often due to more than one bit error. Thus, the relationship between BER and CRCE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using CRC-4 counts to determine the BER. Since FEBEs are indications of CRCEs at the far end, and are accumulated identically to CRCEs, the same explanation holds for the FEBE event counter.

The bit error rate for E1 can be calculated from the one-second PMON CRCE count by the following equation:

$$\textbf{Bit Error Rate} = 1 - 10^{\left(\frac{\log\left(1-\frac{8}{8000}CRCE\right)}{8*256}\right)}$$

Figure 17 CRCE Count vs. BER (E1 mode)

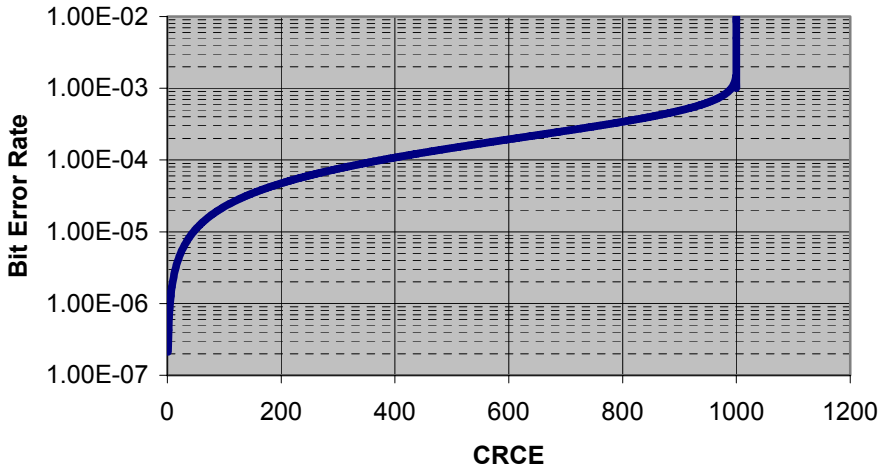
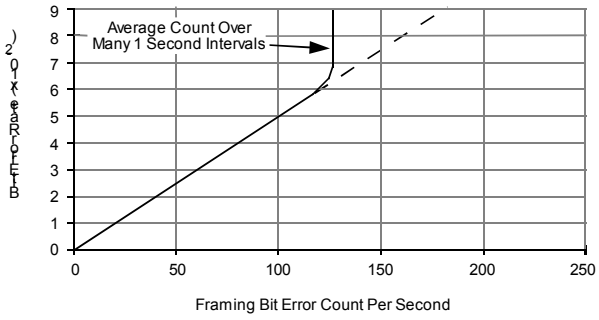


Figure 18 illustrates the expected count values for a range of Bit Error Ratios in T1 mode.

Figure 18 FER Count vs. BER (T1 ESF mode)

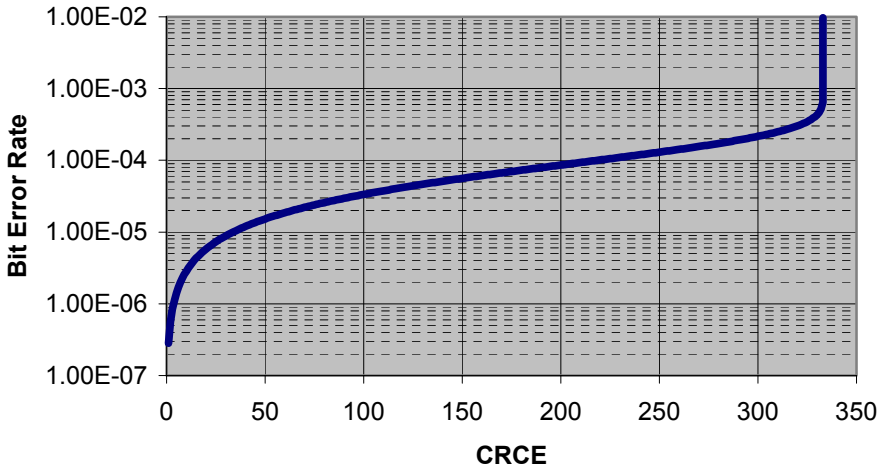


Since the maximum number of ESF superframes that can occur in one second is 333, the 9-bit BEE counter cannot saturate in one second in ESF framing format. Despite this, there is not a linear relationship between BER and BEE count, due to the nature of the CRC-6 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per superframe, so the number of CRC-6 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-6 error is often due to more than one bit error. Thus, the relationship between BER and BEE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using ESF CRC-6 counts to determine the BER.

The bit error rate for T1 ESF can be calculated from the one-second PMON CRCE count by the following equation:

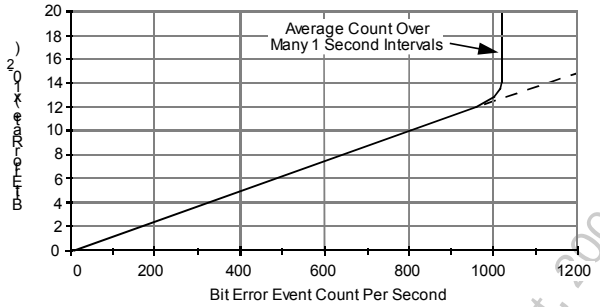
Bit Error Rate = 1 - 10 $^{\left(\frac{\log\left(1-\frac{24}{8000}BEE\right)}{24*193}\right)}$

Figure 19 CRCE Count vs. BER (T1 ESF mode)



For T1 SF format, the CRCE and FER counts are identical, but the FER counter is smaller and should be ignored.

Figure 20 CRCE Count vs. BER (T1 SF mode)



12.6 Using the Internal T1/E1 Data Link Receiver

A time-sliced HDLC receiver processes the data links extracted from the tributaries. Receive packets are queued in a dedicated 128 byte FIFO for each tributary. The reading of the FIFOs by an external microprocessor is usually done in response to an interrupt, but polling is also supported.

On power up of the system, the receiver defaults to a disabled state. One must use the RHDL Indirect Channel Data registers to program each tributary. The configuration of each tributary is independent of all others. The RHDL Interrupt Control register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. The FIFO threshold is a global setting optimized for a particular system by trading off minimizing the number of interrupts against avoiding FIFO overflows.

When the receiver is first enabled to delineate packets, it will assume the link is idle and immediately begin searching for flags. No bytes will be written into the FIFO until a flag is recognized. This is also true after an abort is detected. If packet delineation is disabled, all bytes are written raw into the FIFO.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The T1/E1 Receive HDLC processor (RHDL) can be used in a polled or interrupt driven mode for the transfer of packet data. In the polled mode, the processor controlling the RHDL must periodically read the RHDL Interrupt Status #1 register to determine if any tributaries need processing. In the interrupt driven mode, the processor controlling the RHDL uses the TE-32 INTB output and the TE-32 Master Interrupt Source registers to determine when to service the RHDL.

In the case of interrupt driven data transfer from the RHDL to the processor, the INTB output of the TE-32 is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the TE-32 Master Interrupt Source register followed by the Master Interrupt Source T1E1 register to determine if RHDL is the interrupt source. Once it has identified that the RHDL has generated the interrupt, it processes the data in the following order:

Read the RHDL Interrupt Status #1 register. The value returned will indicate if any of RHDL Interrupt Status #2 through #11 should be read. Any bits returned as a logic 1 will indicate the associated tributary needs servicing. The bits in the RHDL Interrupt Status registers are write-one-to-clear, so the value read should be written back. Repeat steps 2 through 8 for each tributary with an INT bit set.

Write the RHDL Indirect Channel Address with the tributary index and set the FACCESS bit to logic 1.

Write the RHDL Indirect Status with 0x40 to initiate an indirect read.

Read RHDL Indirect Channel Data #2 register (0x011B) until CBUSY is returned as logic 0. Store the last FE, OVR, PKIN and PBS[2:0] bits read.

Read the HDLC data byte from the RHDL Indirect Channel Data #1 register (0x011A).

If OVR = 1, then discard the last frame and go to step 2. Overrun causes a reset of FIFO pointers and the loss of 128 bytes. Because an overflow likely occurred in the midst of a packet, discard all byte up to the next end-of-packet read.

Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

If PBS[2:0] = 010, an abort has occur so discard the data byte read in step 5.

If PBS[2:0] = 1XX, store the last byte of the packet and check the PBS[1:0] bits for CRC or non-integer-byte errors before deciding whether or not to keep the packet.

If PBS[2:0] = 000, store the packet data.

If FE = 0, go to step 3 else service the next tributary or exit this interrupt service routine to wait for the next interrupt.

If the RHDL data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

12.7 Using the Internal T1/E1 Data Link Transmitter

A time-sliced HDLC transmitter (THDL) formats the data links inserted into the T1/E1 tributaries. Raw packets are written by an external microprocessor to a dedicated 128 byte FIFO for each tributary. The HDLC transmitter reads the FIFO once a complete packet is written or when a specified FIFO fill threshold is passed. Also, Performance Reporting Messages (PRMs) may be transmitted autonomously once a second. The transmitter takes care of bit stuffing and insertion of the CRC protection and flags.

By default, the HDLC transmitter operates in a clear channel mode in which the contents of the FIFO are transmitted verbatim without bit stuffing or CRC. If the FIFO becomes empty, flags will be transmitted. To enable the HDLC features, the DELIN context bit must be set via the THDL Indirect Channel Data registers.

FIFO thresholds must be set to avoid overflows and underflows, which result in lost data and an abort sequence. The actual thresholds depend on operating system latencies and algorithms used to write the packets. The Upper Transmit Threshold value determines how many bytes must be written before transmission of an incomplete packet starts. It should be set at a value large enough to ensure an underflow does not occur before the complete packet is written under worst case conditions, such as excessive interrupt servicing. Note that complete packets are always transmitted regardless of the Upper Transmit Threshold value. A large Upper Transmit Threshold value may result in FIFO overflows if large packets are being written. To avoid overflows, it is recommended writes only resume after the Lower Interrupt Threshold is reached.

The T1/E1 Transmit HDLC processor (THDL) can be used in a polled or interrupt driven mode for the transfer of packet data. In the polled mode, the processor controlling the THDL must periodically read the THDL Interrupt Status #1 register to determine if there's been a change in FIFO status. In the interrupt driven mode, the processor controlling the THDL uses the TE-32 INTB output and the TE-32 Master Interrupt Source registers to determine when to service the THDL.

In the case of interrupt driven data transfer from the processor to THDL, the INTB output of the TE-32 is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the TE-32 Master Interrupt Source register followed by the Master Interrupt Source T1E1 register to determine if HDLC Transmitter is the interrupt source. Once it has identified that the THDL has generated the interrupt, it processes the data in the following order:

Read the THDL Interrupt Status #1 register. The value returned will indicate if any of THDL Interrupt Status #2 through #11 should be read. Any bits returned as a logic 1 will indicate the associated tributary needs servicing. The bits in the THDL Interrupt Status registers are write-one-to-clear, so the value read should be written back. Repeat steps 2 through 8 for each tributary with an INT bit set.

Write the THDL Indirect Channel Address with the tributary index and set the FACCESS bit to logic 1.

Write the THDL Indirect Status register (0x0130) with 0x40 to initiate an indirect read.

Read the THDL Indirect Status register until CBUSY is returned as logic 0.

Read the THDL Indirect Channel Data #2 register (0x0133).

A logic 1 OVRI indicates the FIFO for the tributary has overflowed and a packet has been corrupted. The entire contents of the current packet should be written again to the FIFO.

A logic 1 UDRI indicates the FIFO for the tributary has underrun, a packet has been corrupted and an abort has been sent. The entire contents of the current packet should be written again to the FIFO.

A logic 1 LFILLI indicates the FIFO level has dropped below a programmed threshold or has become empty. Packet data may be written. If EMPTY is logic 1, 128 bytes may be written. If EMPTY is logic 0, 128 minus the LINT[6:0] value bytes may be written. Write the THDL Indirect Status register (0x0130) with 0x00 to configure indirect writes. Also, the EOM bit should be initialized to zero and need not be written for each byte except the last of the packet. For each byte, repeat the following:

a. Read the THDL Indirect Status register (0x0130) until CBUSY is returned as logic 0.

b. If the byte is the last of a packet, write a logic 1 to the EOM bit position of the second THDL Indirect Channel Data Register (0x0134).

c. Write a byte to the first THDL Indirect Channel Data Register (0x0133). This initiates the indirect write.

12.8 Using the Time-Sliced T1/E1 Transceivers

12.8.1 Initialization

The configuration of the 32 T1/E1 framers is stored in context RAMs. These RAMs are initialized to all zeros upon release of reset. This effectively places the framers in T1 SF mode with frame slip buffers and jitter attenuators in both the ingress and egress paths. All trunk conditioning and alarm generation defaults to disabled.

12.9 T1 Automatic Performance Report Format

Table 16 Performance Report Message Structure and contents

Octet No.	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
1	FLAG							
2	SAPI						C/R	EA
3	TEI							EA
4	CONTROL							
5	G3	LV	G4	U1	U2	G5	SL	G6
6	FE	SE	LB	G1	R	G2	Nm	NI
7	G3	LV	G4	U1	U2	G5	SL	G6
8	FE	SE	LB	G1	R	G2	Nm	NI
9	G3	LV	G4	U1	U2	G5	SL	G6
10	FE	SE	LB	G1	R	G2	Nm	NI
11	G3	LV	G4	U1	U2	G5	SL	G6
12	FE	SE	LB	G1	R	G2	Nm	NI
13	FCS							
14	FCS							
15	FLAG							

Notes:

1. The order of transmission of the bits is LSB (Bit 1) to MSB (Bit 8).

Table 17 Performance Report Message Structure Notes

Octet No.	Octet Contents	Interpretation
1	01111110	Opening LAPD Flag
2	00111000 00111010	From CI: SAPI=14, C/R=0, EA=0 From carrier: SAPI=14,C/R=1,EA=0
3	00000001	TEI=0,EA=1
4	00000011	Unacknowledged Frame
5,6	Variable	Data for latest second (T')
7,8	Variable	Data for Previous Second(T'-1)
9,10	Variable	Data for earlier Second(T'-2)
11,12	Variable	Data for earlier Second(T'-3)
13,14	Variable	CRC16 Frame Check Sequence
15	01111110	Closing LAPD flag

Table 18 Performance Report Message Contents

Bit Value	Interpretation
G1=1	CRC ERROR EVENT =1
G2=1	1<CRC ERROR EVENT ≤5
G3=1	5<CRC ERROR EVENT ≤10
G4=1	10<CRC ERROR EVENT ≤100
G5=1	100<CRC ERROR EVENT ≤319
G6=1	CRC ERROR EVENT ≤ 320
SE=1	Severely Errored Framing Event ≥ 1(FE shall =0)
FE=1	Frame Synchronization Bit Error Event ≥1 (SE shall=0)
LV=1	Line code violation event ≥ 1. This bit is always encoded as 0.
SL=1	Slip Event ≥ 1. This bit is always zero if the ELSTBYP bit of the RX-SBI-ELST Indirect Channel Data register has been set to logic 1. When H-MVIP only mode is set (i.e. SYSOPT=01), the slips are relative to the CMV8MCLK input. Otherwise, the slips are relative to the SREFCLK.
LB=1	Payload Loopback Activated. TE-32 doesn't perform payload loopbacks; therefore, this bit is always encoded as 0.
U1,U2=0	Under Study For Synchronization.
R=0	Reserved (Default Value =0)
NmNI=00,01,10,11	One second Report Modulo 4 Counter

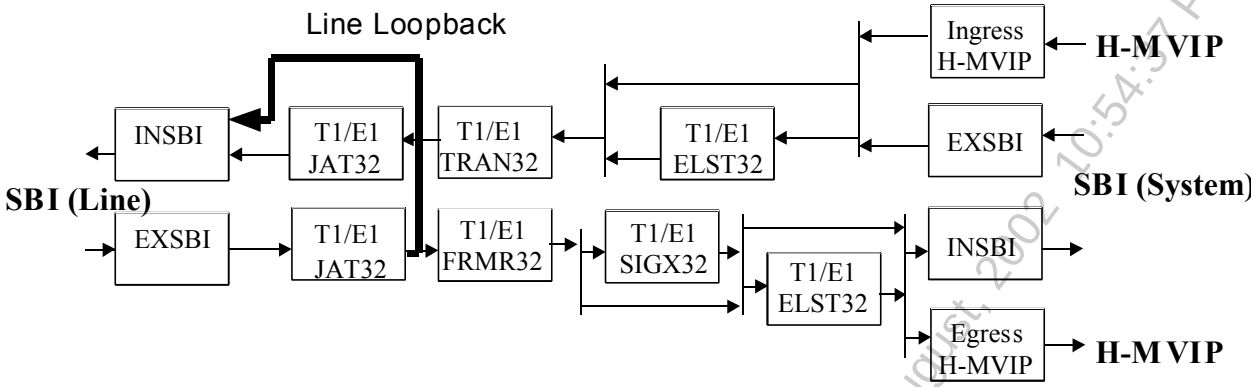
12.10 T1/E1 Framer Loopback Modes

The TE-32 provides two loopback modes for T1/E1 links to aid in network and system diagnostics. The internal T1/E1 line loopback can be initiated at any time via the µP interface, but is usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the framer.

T1/E1 Line Loopback

T1/E1 Line loopback is initiated by setting the LLOOP bit to a 1 through the TJAT Indirect Channel Data register. When in line loopback mode, the appropriate T1/E1 framer in the TE-32 is configured to internally connect the jitter-attenuated clock and data from the RJAT to the transmit clock and data going to the line side SBI bus. The RJAT may be bypassed if desired. Conceptually, the data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 21.

Figure 21 T1/E1 Line Loopback

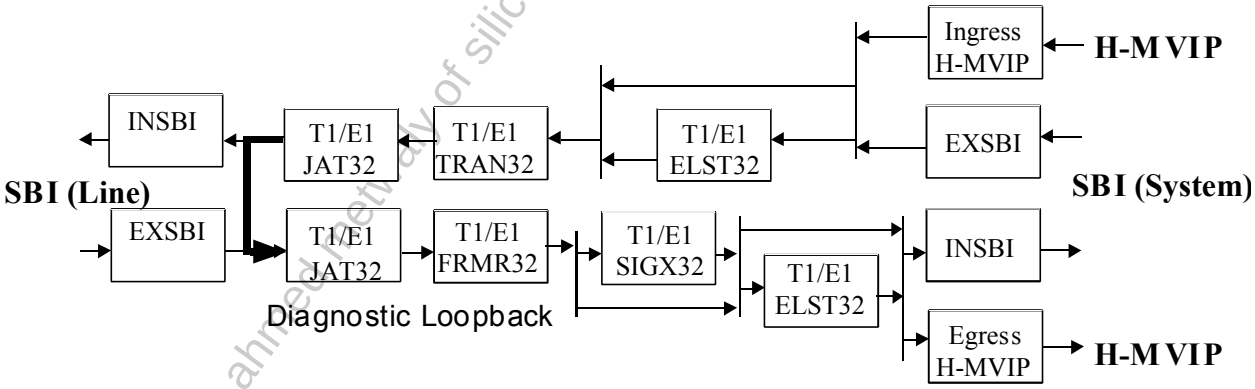


T1/E1 Diagnostic Digital Loopback

When Diagnostic Digital loopback is initiated, by writing a 1 to the DLOOP bit through the RJAT Indirect Channel Data register, the appropriate T1/E1 framer in the TE-32 is configured to internally connect its transmit clock and data to the receive clock and data. The data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 22.

Note: The RX_LKRATE_SEL (Receive Linkrate Select) bit in register 0x0040, must be set to logic '0' if DLOOP is enabled. Otherwise the internal linkrate information will be corrupt.

Figure 22 T1/E1 Diagnostic Digital Loopback



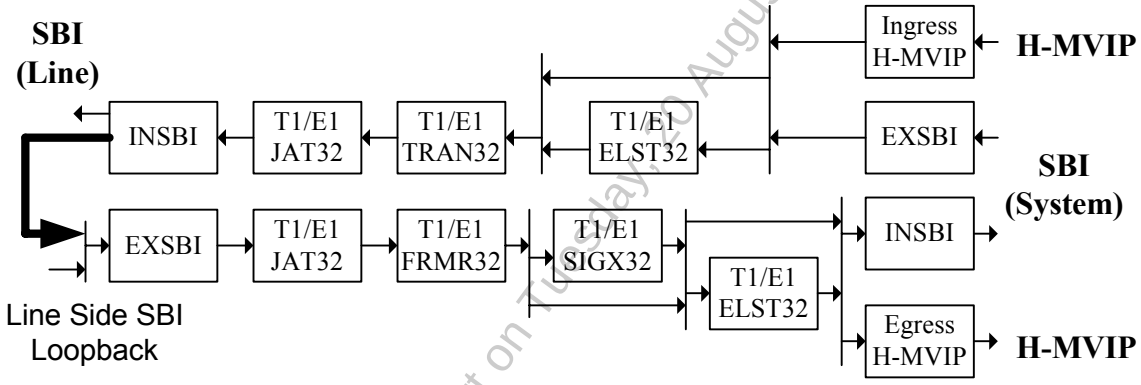
12.11 Line Side SBI Bus Diagnostic Loopback Mode

The TE-32 provides a loopback at the line side SBI bus interface to aid in network and system diagnostics at the line side SBI interface.

The line side SBI Bus diagnostic loopback allows the add bus stream to be looped back into the drop bus receive path, overriding the data stream received on the drop bus inputs. While the line side SBI diagnostic loopback is active, valid data continues to be transmitted on the line side SBI add bus outputs. The entire line side SBI drop bus is overwritten by the diagnostic loopback. This loopback is enabled by writing to the DLOOP bit in the Line Side SBI Master Loopback Control register (0x070A). This is illustrated in Figure 23.

Note: DLOOP1, DLOOP2 (in register 0x0702), DLOOP3 (in register 0x0703), DLOOP4 and DLOOP5 (in register 0x0704), must also be set to logic 1 to enable diagnostic loopback.

Figure 23 Line Side SBI Bus Diagnostic Loopback



12.12 SBI Bus Data Formats

The TE-32 uses the Scaleable Bandwidth Interconnect (SBI) bus as a high density link interconnect with devices processing T1s and E1s. The SBI bus is a multi-point to multi-point bus.

12.12.1 Multiplexing Structure

The SBI structure uses a locked SONET/SDH structure fixing the position of the TU-3 relative to the STS-3/STM-1. The SBI is also of fixed frequency and alignment as determined by the reference clock (SREFCLK) and frame indicator signals (SAC1FP, SDC1FP, LAC1FPI and LDC1FP). Frequency deviations are compensated by adjusting the location of the T1/E1 channels using floating tributaries as determined by the V5 indicator and payload signals (SDV5, SAV5, LDV5, LAV5, SDPL, SAPL, LDPL and LAPL).

able 19 represents a 19.44 Mbit/s signal, showing the bus structure for carrying T1 and E1 tributaries in a SDH STM-1 like format. The TE-32 supports up to 32 T1s or 32 E1s (out of a possible 84 T1s and 63 E1s) which are carried within the 3 multiplexed Synchronous Payload Envelopes called SPE1, SPE2 and SPE3 (in columns 16-270). Each envelope carries up to 28 T1s or 21 E1s. SPE1 carries the T1s numbered 1,1 through 1,28 and E1s numbered 1,1 through 1,21. SPE2 carries the T1s numbered 2,1 through 2,28 and E1s numbered 2,1 through 2,21. SPE3 carries the T1s numbered 3,1 through 3,28 and E1s numbered 3,1 through 3,21. The frame signal (SAC1FP, SDC1FP, LAC1FPI or LDC1FP) occurs during the octet labeled C1 in Row 1 column 7. The Add and Drop buses have independent frame signals to allow for arbitrary alignment of the two buses.

On the line side SBI the mapping of the 32 T1s or E1s is fixed. The first 16 T1s or E1s are mapped to the first 16 tributaries of SPE1 (i.e 1,1 through 1,16), and the second 16 T1s or E1s are mapped to the first 16 tributaries of SPE2 (i.e 2,1 through 2,16). SPE3 is unused.

On the system side SBI the 32 T1s or E1s can be mapped to any of the above mentioned tributaries. However, internally the TE-32 requires the 32 T1s or E1s to be mapped to SPE1 (1,1 through 1,16) and SPE2 (2,1 through 2,16). This is achieved by using the time switches in the system side INSBI and EXSBI Control Registers.

The system side SBI can be optionally configured to run at 77.76 Mbit/s, by setting the S77 input to logic 1 and SREFCLK to 77.76 MHz. The 77.76 MHz SBI bus, referred to as SBI336, is exactly four interleaved 19.44 MHz SBI buses. There are four STM-1s each containing 3 SPE's which are each able to carry upto 28 T1s or 21 E1s. In this mode, the TE-32 drives or samples the SBI bus every fourth cycle. The System Side SBI STM-1 Select bits, SSTM[1:0], determine during which one of the four byte interleaved STM-1s the TE-32 drives SADATA[7:0] and expects data on SDDATA[7:0].

Table 19 19.44 MHz SBI Structure for Carrying Multiplexed Links

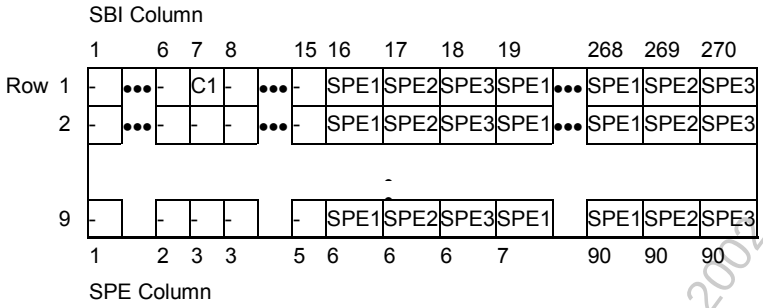
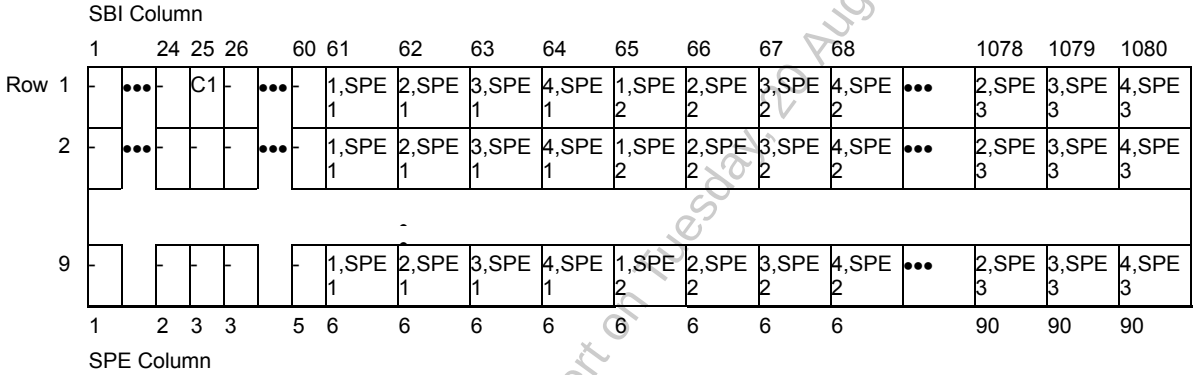


Table 20 77.76 MHz SBI (SBI336) Structure for Carrying Multiplexed Links



12.12.2 Tributary Numbering

Tributary numbering for T1 and E1 uses the SPE number, followed by the Tributary number within that SPE and are numbered sequentially. Table 21 and Table 22 show the T1 and E1 column numbering and relates the tributary number to the SPE column numbers and overall SBI column structure.

Table 21 T1 Tributary Column Numbering

T1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,35,63			19,103,187
2,1		7,35,63		20,104,188
3,1			7,35,63	21,105,189
1,2	8,36,64			22,106,190
2,2		8,36,64		23,107,191
•••				
1,28	34,62,90			100,184,268
2,28		34,62,90		101,185,269
3,28			34,62,90	102,186,270

Table 22 E1 Tributary Column Numbering

E1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,28,49,70			19,82,145,208
2,1		7,28,49,70		20,83,146,209
3,1			7,28,49,70	21,84,147,210
1,2	8,29,50,71			22,85,148,211
2,2		8,29,50,71		23,86,149,212
•••				
1,21	27,48,69,90			79,142,205,268
2,21		27,48,69,90		80,143,206,269
3,21			27,48,69,90	81,144,207,270

12.12.3 SBI Timing Master Modes

The TE-32 System Interface SBI bus supports both synchronous and asynchronous SBI timing modes. The Line Side SBI bus only supports asynchronous timing modes. Synchronous modes apply only to framed T1 and E1 tributaries and are used with ingress elastic stores to rate adapt the receive tributaries to the fixed SBI data rate. Asynchronous modes allow T1 and E1 tributaries to float within the SBI structure to accommodate differences in timing.

In synchronous SBI mode, the T1 DS0s and E1 timeslots are in a fixed format and do not move relative to the SBI structure. The SBI frame pulse, SAC1FP or SDC1FP, in synchronous mode can be enabled to indicate CAS signaling multi-frame alignment by pulsing once every 12th 2KHz frame pulse period. SREFCLK sets the ingress rate from the receive elastic store.

In Asynchronous modes, timing is communicated across the Scaleable Bandwidth Interconnect by floating data structures within the SBI. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet be passing an extra octet in the V3 octet locations. When the source is slower than the SBI the floating payload is retarded by leaving the octet after the V3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

On the system interface Drop Bus, the TE-32 is timing master as determined by the arrival rate of data over the line side SBI bus. Likewise, on the line side Add Bus, the TE-32 is timing master as determined by either the arrival rate of data over the system interface SBI bus or the CTCLK input frequency.

On the line side Drop Bus, the TE-32 is timing slave.

On the system interface Add Bus, the TE-32 can be either the timing master or the timing slave.

When the TE-32 is the timing slave it receives its transmit timing information from the arrival rate of data across the SBI bus. When the TE-32 is the timing master, it signals devices on the SBI Add bus to speed up or slow down with the justification request signal, SAJUST_REQ. The TE-32 as timing master indicates a speedup request to a Link Layer SBI device by asserting the justification request signal high during the V3 octet. When this is detected by the Link Layer it will speed up the channel by inserting extra data in the next V3 octet. The TE-32 indicates a slow down request to the Link Layer by asserting the justification request signal high during the octet after the V3 octet. When detected by the Link Layer it will retard the channel by leaving the octet following the next V3 octet unused. Both advance and retard rate adjustments take place in the frame or multi-frame following the justification request.

12.12.4SBI Link Rate Information

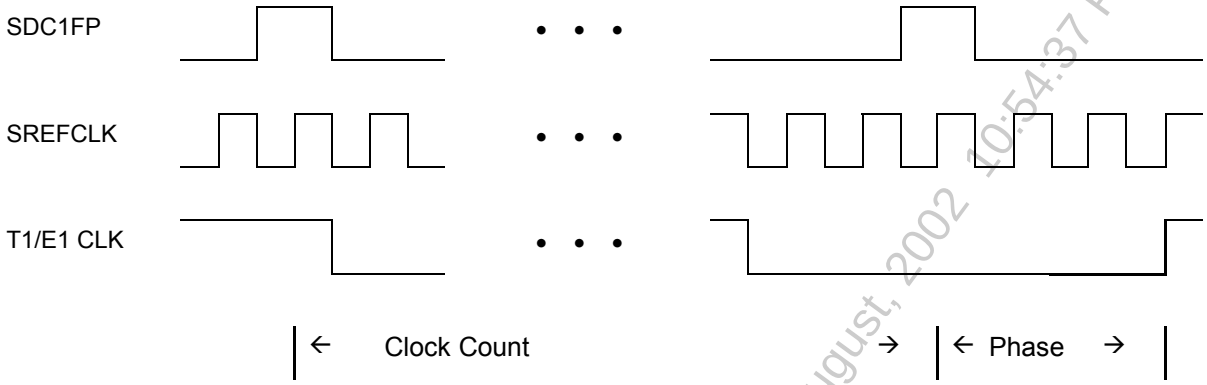
The TE-32 SBI bus provides a method for carrying link rate information between devices. For T1 and E1, the link rate information is always generated on the system interface Drop and line side Add buses, and always ignored on the system interface Add and line side Drop buses. These methods use the reference 19.44 MHz SBI clock and the SAC1FP frame synchronization signal to measure channel clock ticks and clock phase for transport across the bus.

The T1 and E1 method allows for a count of the number of T1 or E1 rising clock edges between 2 KHz SDC1FP/LAC1FP frame pulses. This count is encoded in ClkRate[1:0] to indicate that the nominal number of clocks, one more than nominal or one less than nominal should be generated during the SDC1FP/LAC1FP period. This method also counts the number of 19.44 MHz clock rising edges after sampling SDC1FP/LAC1FP high to the next rising edge of the T1 or E1 clock, giving the ability to control the phase of the generated clock. The link rate information passed across the SBI bus via the V4 octet and is shown in Table 23.

Table 24 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

Note that while the TE-32 generates valid link rate information on the SBI Drop bus, it ignores the V4 byte on the Add bus.

Table 23 SBI T1/E1 Link Rate Information



Link Rate Octet	Bit #	7	6	5:4	3:0
T1/E1 Format		ALM	0	ClkRate[1:0]	Phase[3:0]

Table 24 SBI T1/E1 Clock Rate Encoding

ClkRate[1:0]	T1 Clocks / 2KHz	E1 Clocks / 2 KHz
“00” – Nominal	772	1024
“01” – Fast	773	1025
“1x” – Slow	771	1023

12.12.5SBI Alarms

The TE-32 transfers alarm conditions across the SBI for T1and E1 tributaries.

Table 23 and Table 24 show the alarm indication bit, ALM, as bit 7 of the Link Rate Octet. Devices connecting to the TE-32 which do not support alarm indications must set this bit to 0 on the SBI bus.

The presence of an alarm condition is indicated by the ALM bit set high in the Link Rate Octet. For T1 and E1 tributaries, either an out-of-frame condition or Red alarm (persistent out-of-frame) may set the ALM as determined by the IREDEN and IOOFEN per-tributary configuration bits. The absence of an alarm condition is indicated by the ALM bit set low in the Link Rate Octet. In the egress direction, the TE-32 can be configured to use the alarm bit to force AIS on a per link basis by the EALMEN register bit.

12.12.6T1 Tributary Mapping

Table 25 shows the format for mapping T1s within the SPE octets. The DS0s and framing bits within each T1 are easily located within this mapping for channelized T1 applications. It is acceptable for the framing bit to not carry a valid framing bit on the system interface Add Bus since the TE-32 will provide this information. Unframed T1s use the exact same format for mapping 32 T1s into the SBI except that the T1 tributaries need not align with the frame bit and DS0 locations. The V1, V2 and V4 octets are not used to carry T1 data and are either reserved or used for control across the interface. When enabled, the V4 octet is the Link Rate octet of Table 23. It carries alarm and clock phase information across the SBI bus. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries a T1 data octet but only during rate adjustments as indicated by the V5 indicator signals, SDV5, SAV5, LAV5 and LDV5, and payload signals, SDPL, SAPL, LAV5 and LDV5. The PPSSSSFR octets carry channel associated signaling (CAS) bits and the T1 framing overhead. The DS0 octets are the 24 DS0 channels making up the T1 link.

The V1, V2, V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for T1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating T1 is identified via the V5 Indicator signals, which locate the V5 octet. When the T1 tributary rate is faster than the SBI nominal T1 tributary rate, the T1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the T1 tributary rate is slower than the nominal SBI tributary rate the T1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

Table 25 T1 Framing Format

	COL #	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28
ROW #	1-18	19	20-102	103	104-186	187	188-270
1	Unused	V1	V1	V5	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V2	V2	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V3	V3	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V4	V4	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-

The $P_1P_0S_1S_2S_3S_4$FR octet carries T1 framing in the F bit and channel associated signaling in the P_1P_0 and $S_1S_2S_3S_4$bits. Channel associated signaling is optional. The R bit is reserved and is set to 0. The P_1P_0bits are used to indicate the phase of the channel associated signaling and the $S_1S_2S_3S_4$ bits are the channel associated signaling bits for the 24 DS0 channels in the T1. Table 26 shows the channel associated signaling bit mapping and how the phase bits locate the sixteen state CAS mapping for super frame and extended superframe formats. When using four state CAS then the signaling bits are A1-A24, B1-B24, A1-A24, B1-B24 in place of are A1-A24, B1-B24, C1-C24, D1-D24. When using 2 state CAS there are only A1-A24 signaling bits.

The P_1P_0 and $S_1S_2S_3S_4$ bits are unused on the line side SBI Bus. Data on the Line side SBI is unframed.

For the system interface Drop Bus only, when the SYNCH_TRIB bit is set for a tributary, the DS0 alignment is precisely as presented in Table 25, and the P_1P_0 and $S_1S_2S_3S_4$bits in the first row of Table 26 are aligned to the multiframe indicated by the SDC1FP signal, be it an input or output. The F-bit positions in Table 26 have an arbitrary alignment relative to the P_1P_0 bits that will change with each controlled frame slip; that illustrated is only an example. The signaling contained within the robbed bit positions of the DS0s will also have an arbitrary alignment relative to the P_1P_0 bits.

Table 26 T1 Channel Associated Signaling bits

				SF	ESF	
S_1	S_2	S_3	S_4	F	F	P_1 P_0
A1	A2	A3	A4	F1	M1	00
A5	A6	A7	A8	S1	C1	00
A9	A10	A11	A12	F2	M2	00
A13	A14	A15	A16	S2	F1	00
A17	A18	A19	A20	F3	M3	00
A21	A22	A23	A24	S3	C2	00
B1	B2	B3	B4	F4	M4	01
B5	B6	B7	B8	S4	F2	01
B9	B10	B11	B12	F5	M5	01
B13	B14	B15	B16	S5	C3	01
B17	B18	B19	B20	F6	M6	01
B21	B22	B23	B24	S6	F3	01
C1	C2	C3	C4	F1	M7	10
C5	C6	C7	C8	S1	C4	10
C9	C10	C11	C12	F2	M8	10
C13	C14	C15	C16	S2	F4	10
C17	C18	C19	C20	F3	M9	10
C21	C22	C23	C24	S3	C5	10
D1	D2	D3	D4	F4	M10	11
D5	D6	D7	D8	S4	F5	11
D9	D10	D11	D12	F5	M11	11
D13	D14	D15	D16	S5	C6	11
D17	D18	D19	D20	F6	M12	11
D21	D22	D23	D24	S6	F6	11

T1 tributary asynchronous timing is compensated via the V3 octet. T1 tributary link rate adjustments are optionally passed across the SBI via the V4. T1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location.

In synchronous mode, the T1 tributary mapping is fixed to that shown in Table 25 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

12.12.7E1 Tributary Mapping

Table 27 shows the format for mapping E1s within the SPE octets. The timeslots and framing bits within each E1 are easily located within this mapping for channelized E1 applications. It is acceptable for the framing bits to not carry valid framing information on the system interface Add Bus since the TE-32 will provide this information. Unframed E1s use the exact same format for mapping 32 E1s into the SBI except that the E1 tributaries need not align with the timeslot locations associated with channelized E1 applications. The V1, V2 and V4 octets are not used to carry E1 data and are either reserved or used for control information across the interface. When enabled, the V4 octet carries clock phase information across the SBI. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries an E1 data octet but only during rate adjustments as indicated by the V5 indicator signals, SDV5 and SAV5, and payload signals, SDPL and SAPL. The PP octets carry channel associated signaling phase information and E1 multiframe alignment. TS#0 through TS#31 make up the E1 channel.

The V1, V2, V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for E1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating E1 is identified via the V5 Indicator signals, SDV5 and SAV5, which locate the V5 octet. When the E1 tributary rate is faster than the E1 tributary nominal rate, the E1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the E1 tributary rate is slower than the nominal rate the E1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

For the system interface Drop Bus only, when the SYNCH_TRIB bit is set for a tributary, the timeslot alignment is precisely as presented in Table 27.

Table 27 E1 Framing Format

	COL #	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21
ROW #	1-18	19	20-81	82	83-144	145	146-207	208	209-270
1	Unused	V1	V1	V5	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V2	V2	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V3	V3	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V4	V4	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-

When using channel associated signaling (CAS) TS#16 carries the ABCD signaling bits and the timeslots 17 through 31 are renumbered 16 through 30. The PP octet is 0x00 for all frames except for the frame which carries the CAS for timeslots 15/30 at which time the PP octet is C0h. The first octet of the CAS multi-frame, RRRRRRRR, is reserved and should be ignored by the receiver when CAS signaling is enabled. Table 28 shows the format of timeslot 16 when carrying channel associated signaling.

On the line side, the signaling multiframe alignment is not communicated; the PP octet is irrelevant. The E1 frame establishes signaling multiframe assuming TS#16 contains a valid frame alignment pattern.

Table 28 E1 Channel Associated Signaling bits

TS#16[0:3]	TS#16[4:7]	PP
RRRR	RRRR	00
ABCD1	ABCD16	00
ABCD2	ABCD17	00
ABCD3	ABCD18	00
ABCD4	ABCD19	00
ABCD5	ABCD20	00
ABCD6	ABCD21	00
ABCD7	ABCD22	00
ABCD8	ABCD23	00
ABCD9	ABCD24	00
ABCD10	ABCD25	00
ABCD11	ABCD26	00
ABCD12	ABCD27	00
ABCD13	ABCD28	00
ABCD14	ABCD29	00
ABCD15	ABCD30	C0

E1 tributary asynchronous timing is compensated via the V3 octet. E1 tributary link rate adjustments are optionally passed across the SBI via the V4 octet. E1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location.

In synchronous mode, the E1 tributary mapping is fixed to that shown in Table 27 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

12.13 H-MVIP Data Format

The H-MVIP data and Channel Associated Signaling interfaces on the TE-32 are able to carry all the DS0s for the T1s or all timeslots for the E1s. When carrying timeslots from E1s the H-MVIP frame is completely filled with 128 timeslots from four E1s but when carrying DS0s from four T1s there are not enough DS0s to completely fill the 128 byte frame. Table 29 shows how the DS0s and CAS bits of four T1s are formatted in the 128 timeslot H-MVIP frame.

Table 30 shows the timeslot and CAS bit H-MVIP format when in E1 mode.

Table 29 Data and CAS T1 H-MVIP Format

Timeslot Number	First T1 DS0 Number	Second T1 DS0 Number	Third T1 DS0 Number	Fourth T1 DS0 Number
0-3	Undefined	Undefined	Undefined	Undefined
4-7	1	1	1	1
8-11	2	2	2	2
12-15	3	3	3	3
16-19	Undefined	Undefined	Undefined	Undefined
20-23	4	4	4	4
24-27	5	5	5	5
28-31	6	6	6	6
32-35	Undefined	Undefined	Undefined	Undefined
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
108-111	21	21	21	21
112-115	Undefined	Undefined	Undefined	Undefined
116-119	22	22	22	22
120-123	23	23	23	23
124-127	24	24	24	24

Table 30 Data and CAS E1 H-MVIP Format

Timeslot Number	First E1 TS Number	Second E1 TS Number	Third E1 TS Number	Fourth E1 TS Number
0-3	0	0	0	0
4-7	1	1	1	1
8-11	2	2	2	2
12-15	3	3	3	3
16-19	4	4	4	4
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
120-123	30	30	30	30
124-127	31	31	31	31

In the ingress direction, each CAS timeslot is encoded as follows (time increases to the right):

1	2	3	4	5	6	7	8
Unused	CGA	OOSMF	OOF	A	B	C	D

The OOF bit is high when the framer has lost frame alignment. The OOSMF bit is high when E1 signaling multiframe alignment has been lost. It is also high when T1 frame alignment has been lost. The CGA bit is high if an integrated AIS or RED alarm has been declared.

In the egress direction, each CAS timeslot is encoded as follows (time increases to the right):

1	2	3	4	5	6	7	8
Unused	Unused	SIGC[1]	SIGC[0]	A	B	C	D

If the INBANDCTL bit of the TPCC Configuration register is logic 1, the SIGC[1:0] field takes on the same definition as the SIGC[1:0] context bits programmed through the TPCC Indirect Channel Data registers. If INBANDCTL is logic 0, the SIGC[1:0] field is unused

In E1 mode, the H-MVIP Common Channel Signaling interface on TE-32 carries timeslot 16 for ISDN signaling, timeslot 15 and timeslot 31 for V5.2 interfaces. In T1 mode, the CCS H-MVIP interface only carries channel 28. E1 and T1 signaling may be mixed on a SPE granularity. Table 31 shows the H-MVIP format for carrying common channeling signaling channels. These formats are fixed so when a signaling or V5.2 channel is not in use the H-MVIP timeslot is filled with all ones.

Table 31 CCS H-MVIP Format

H-MVIP Timeslot Number	CCSID[1], CCSED[1]		CCSID[2], CCSED[2]	CCSID[3], CCSED[3]
	T1 Number (Ch 24)	E1 Number TS 16	E1 Number TS 15	E1 Number TS 31
0	1	1	1	1
1	2	2	2	2
2	3	3	3	3
3	4	4	4	4
4	5	5	5	5
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
15	16	16	16	16
16	undefined	undefined	undefined	undefined
17	undefined	undefined	undefined	undefined
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
28	17	17	17	17
29	18	18	18	18
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
44	32	32	32	32
45	undefined	undefined	undefined	undefined
46	undefined	undefined	undefined	undefined

12.14 System Side SBI 77.76 MHz operation

The TE-32 has the option to operate the system side SBI bus in either 19.44 or 77.76MHz SBI mode. There is a digital delay-locked loop (DLL) needed to simultaneously meet the output propagation delay as well as the setup and hold time requirements for the 77.76MHz SBI bus interface. The DLL is used to minimize output delay on all bus outputs. The DLL measures the phase difference between the external clock and a reference clock and generates an internal clock, which reduces the phase difference between the external clock and the reference clock to zero.

There is a start-up condition in the TE-32 that may cause the DLL of the 77.76MHz SBI to lock-up. The SBI drop bus tristates in this lock-up condition. This lock-up condition is avoided if the start-up interrupt service routine includes the register accesses below, and is implemented upon device configuration:

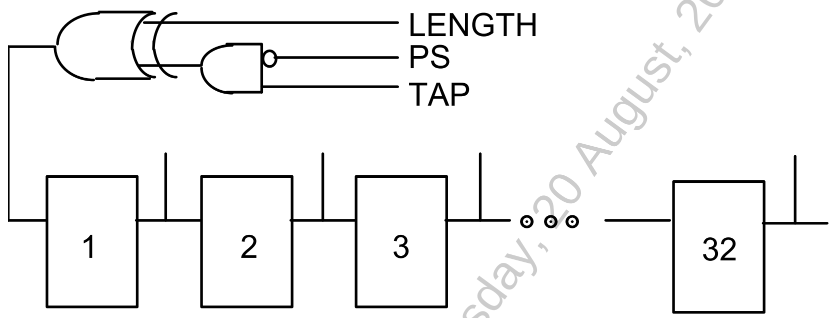
1. Set ERRORE (ERROR interrupt enable) bit to 1 in Register 0x01C4: DLL Configuration. In doing so, an interrupt will be generated upon assertion event of the ERROR indicator status in Register 0x01C7: DLL Control Status. This ERROR bit is set high when the DLL has run out of dynamic range and attempts to move beyond the end of the delay line. Polling may also be used.

2. If the ERROR bit is set high indicating the DLL is locking up, a **DLL software reset** must be invoked for the DLL to regain lock. Writing any values to Register 0x01C6: DLL Delay Tap Status does this and ensures the SBI drop bus will not tristate.

12.15 Full Featured T1/E1 Pattern Generation and Detection

This section applies to the PRBS and fixed pattern generators and detectors accessible through the T1/E1 Pattern Generator and Detector Registers (0x0500 – 0x05B7). The pattern generators can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 24 below.

Figure 24 PRGD Pattern Generator



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

Generating and Detecting Patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers. The repetitive pattern will then be continuously generated. The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream. It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences. Note that the PRGD does NOT look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers (which will then contain the 32 bits detected immediately prior to the strobe).

Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T Recommendation O.151. The register configurations required to generate these patterns and others are indicated in Table 32 and Table 33.

Table 32 Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
2^3 -1	00	02	FF	FF	FF	FF	0	0
2^4 -1	00	03	FF	FF	FF	FF	0	0
2^5-1	01	04	FF	FF	FF	FF	0	0
2^6 -1	04	05	FF	FF	FF	FF	0	0
2^7 -1	00	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1
2^9 -1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} -1	02	09	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} -1	02	10	FF	FF	FF	FF	0	0
2^{18} -1	06	11	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
2^{21} -1	01	14	FF	FF	FF	FF	0	0
2^{22} -1	00	15	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} -1	02	18	FF	FF	FF	FF	0	0
2^{28} -1	02	1B	FF	FF	FF	FF	0	0
2^{29} -1	01	1C	FF	FF	FF	FF	0	0
2^{31} -1	02	1E	FF	FF	FF	FF	0	0

Table 33 Repetitive Pattern Generation (PS bit = 1)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

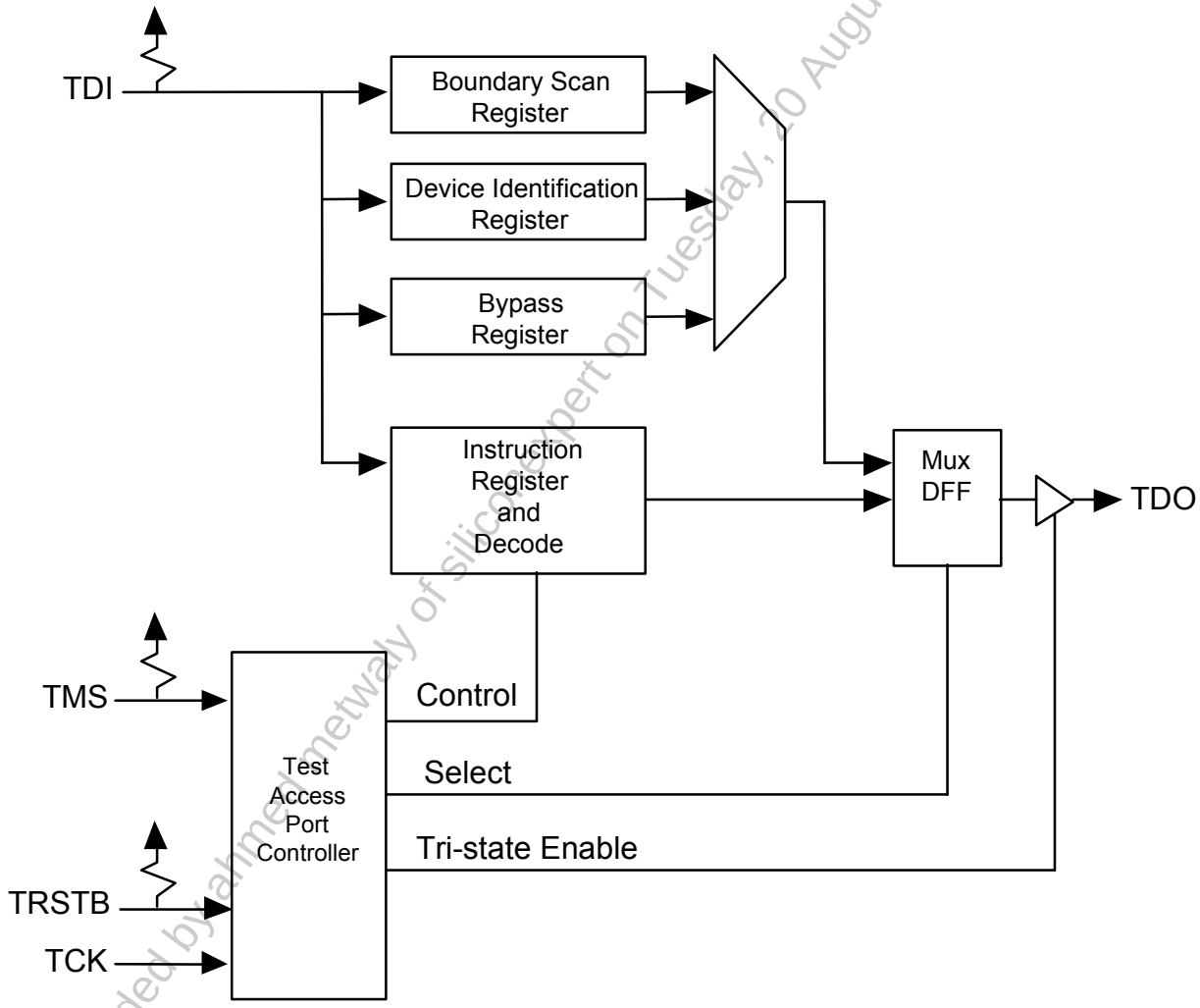
Notes for the Pseudo Random and Repetitive Pattern Generation Tables:

- The PS bit and the QRSS bit are contained in the PRGD Control register
- TR = PRGD Tap Register
- LR = PRGD Length Register
- IR#1 = PRGD Pattern Insertion #1 Register
- IR#2 = PRGD Pattern Insertion #2 Register
- IR#3 = PRGD Pattern Insertion #3 Register
- IR#4 = PRGD Pattern Insertion #4 Register
- The TINV bit and the RINV bit are contained in the PRGD Control register

12.16 JTAG Support

The TE-32 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 25 Boundary Scan Architecture



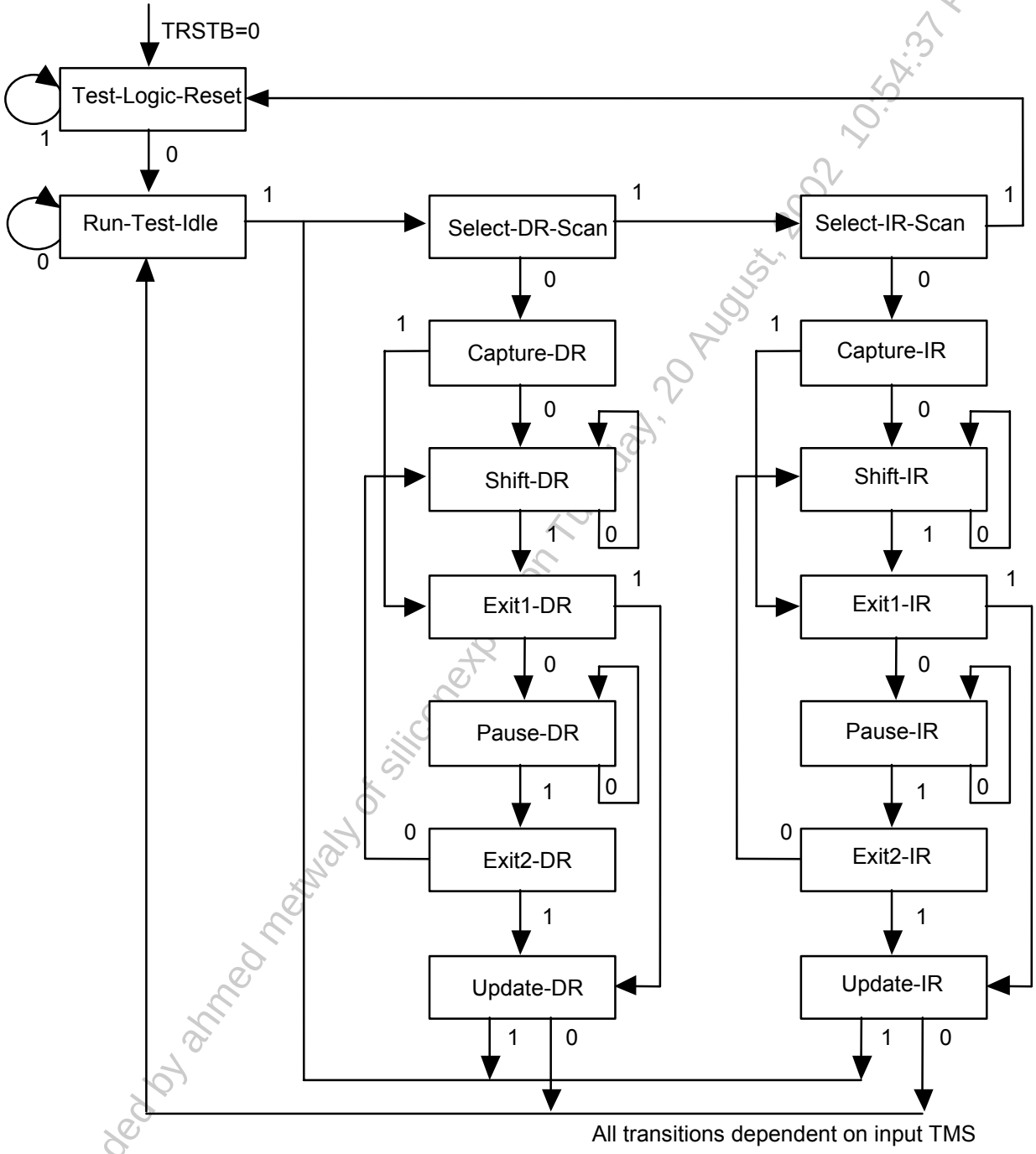
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI, and forced onto all digital outputs.

12.16.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 26 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out of the output, TDO, using the Shift-DR state.

Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table in the JTAG Test Port section 11.2.

Figure 27 Input Observation Cell (IN_CELL)

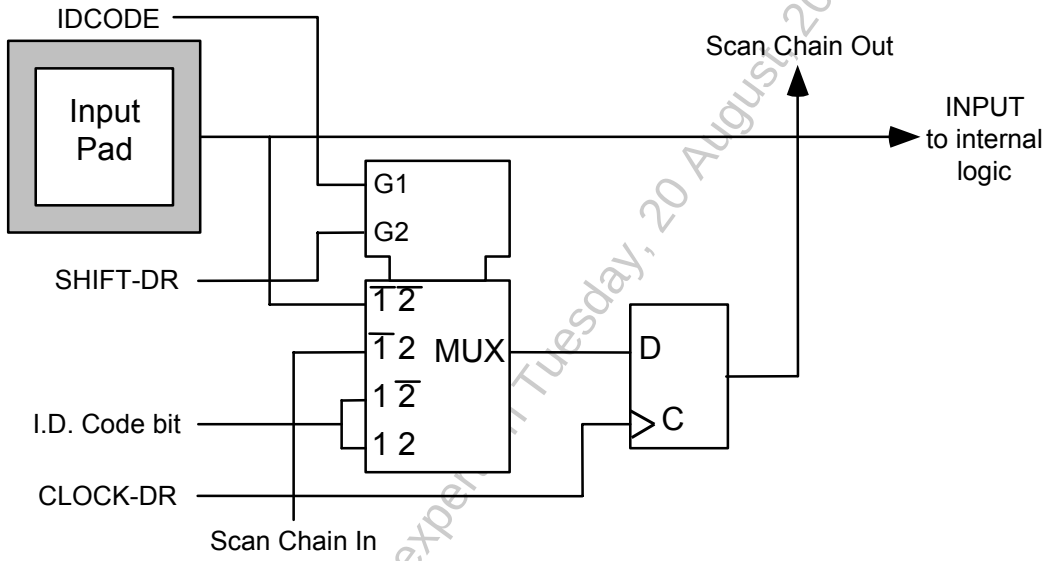


Figure 28 Output Cell (OUT_CELL)

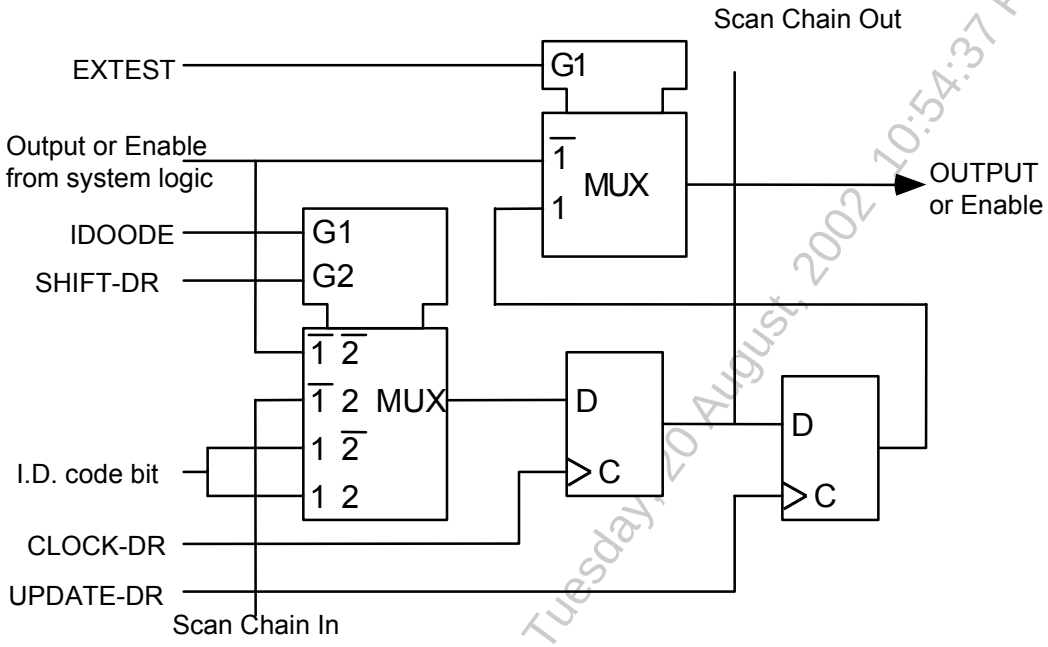


Figure 29 Bidirectional Cell (IO_CELL)

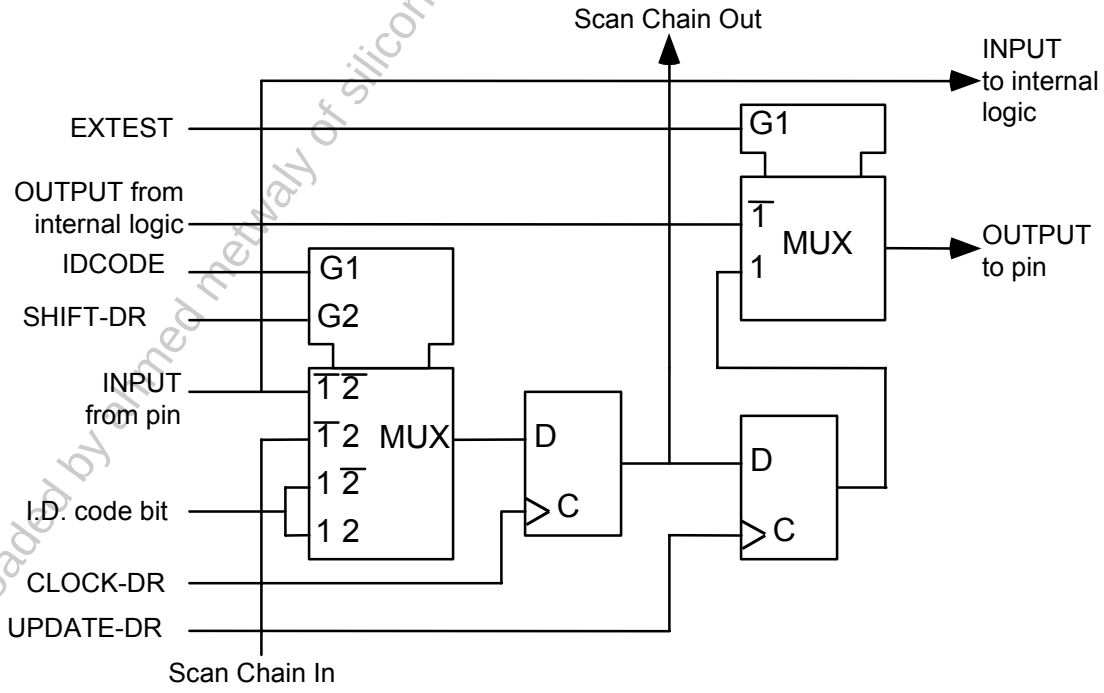
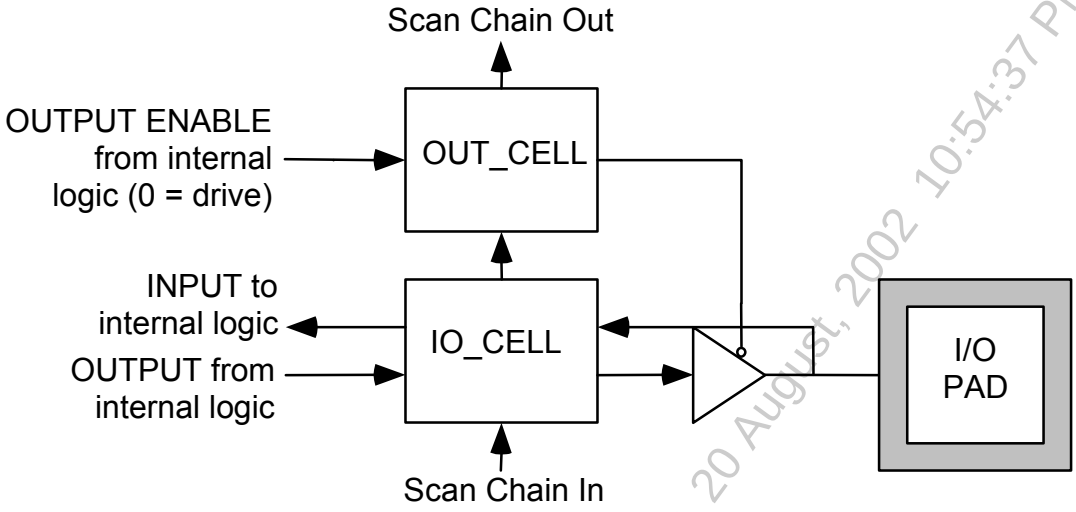


Figure 30 Layout of Output Enable and Bidirectional Cells



13 Functional Timing

13.1 SBI Bus Interface Timing

Figure 31 SBI Bus T1/E1 Functional Timing

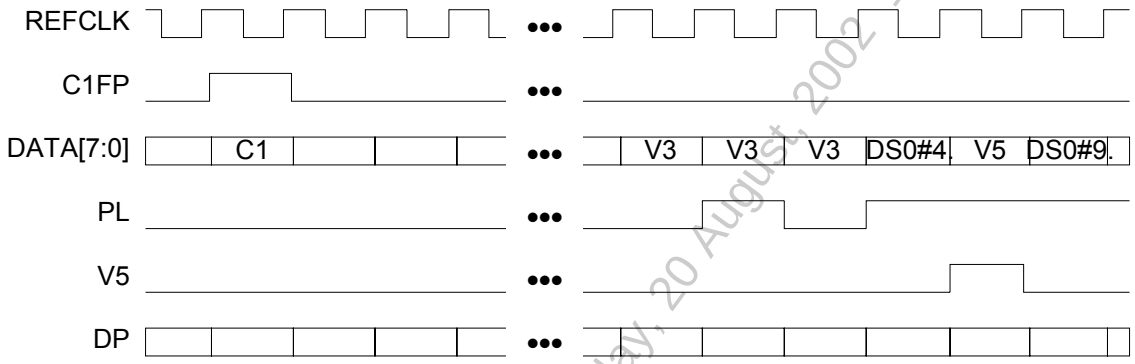


Figure 31 illustrates the operation of the SBI Bus, using a negative justification on the second to last V3 octet as an example. The justification is indicated by asserting PL high during the V3 octet. The timing diagram also shows the location of one of the tributaries by asserting V5 high during the V5 octet.

Generic signal names are used in Figure 31 because it applies to all four SBI interfaces.

The System Side SBI Add bus has one additional signal: the SAJUST_REQ output. The SAJUST_REQ signal is used to by the TE-32 in SBI master timing mode to provide transmit timing to SBI link layer devices.

Figure 32 System Interface SBI ADD Bus Justification Request Functional Timing

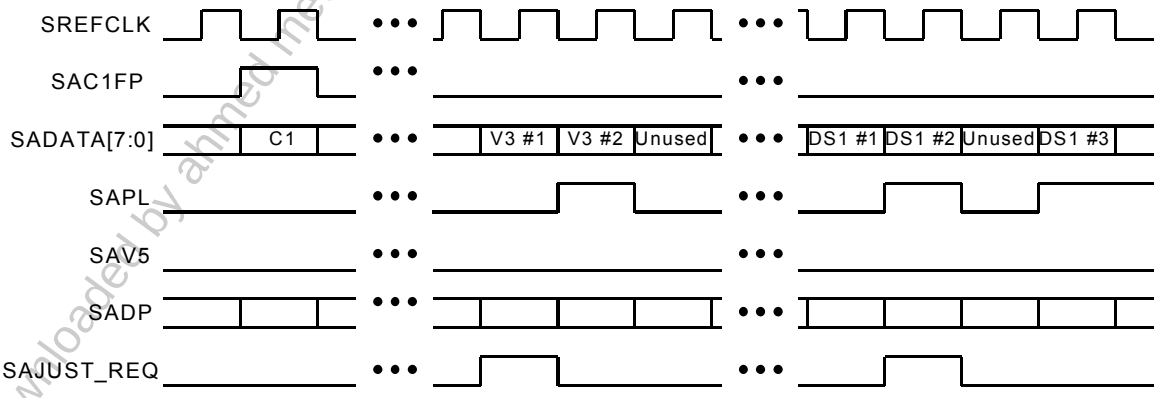


Figure 32 illustrates the operation of the System Interface SBI Add Bus, using positive and negative justification requests as an example. (The responses to the justification requests would take effect during the next multi-frame. The SAPL signal illustrates the response to a positive justification request for DS1 #1 and a negative justification request for DS1 #2 in the previous multiframe). The negative justification request occurs on the DS1 #1 tributary when SAJUST_REQ is asserted high during the V3 octet. The positive justification occurs on the DS1 #2 tributary when SAJUST_REQ is asserted high during the first DS1 #2 octet after the V3 octet.

13.1.1 Notes on 77.76MHz System Side Bus Operation

SBI bus operation at 77.76MHz is simply a byte interleaved multiplex of a 19.44 MByte/s stream with idle cycles. The STM-1 of interest is identified by the SSTM[1:0] bits of the Master Bus Configuration register. On the Add bus, the three unused STM-1s are simply ignored, including parity. On the Drop bus, the unused STM-1s are high-impedance. The following is of special note:

1. Regardless of the state of the SSTM[1:0] bits, the SAC1FP and SDC1FP pulses always identify the 25th byte of the frame.

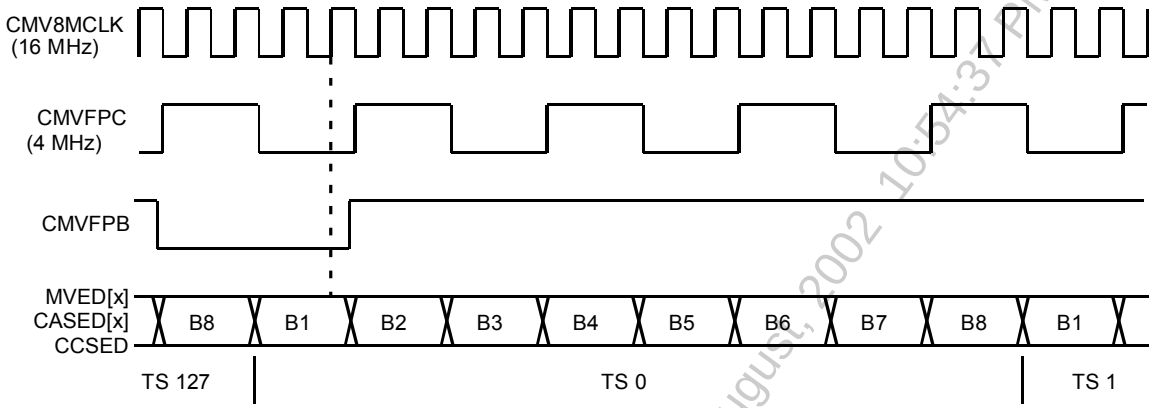
2. Up to four devices may be directly connected to the same bus. Current consumption is minimized if all devices are of the same type (ie. all TE-32s). All devices must receive the same SAC1FP and SDC1FP signals.

3. The SBI bus becomes unconditionally high-impedance upon either a hardware or software reset. All necessary configuration and at least one SDC1FP pulse should precede the setting of the GSOE register bit.

13.2 Egress H-MVIP Link Timing

The timing relationship of the common H-MVIP clock, CMV8MCLK, frame pulse clock, CMVFPC, data, MVED[x], CASED[x] or CCSED, and frame pulse, CMVFPB, signals of a link configured for 8.192 Mbit/s H-MVIP operation with a type 0 frame pulse is shown in Figure 33. The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbit/s H-MVIP operation. The TE-32 samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame. The TE-32 samples the data provided on MVED[x], CASED[x] and CCSED at the ¾ point of the data bit using the rising edge of CMV8MCLK as indicated for bit 1 (B1) of time-slot 1 (TS 1) in Figure 33. B1 is the most significant bit and B8 is the least significant bit of each octet.

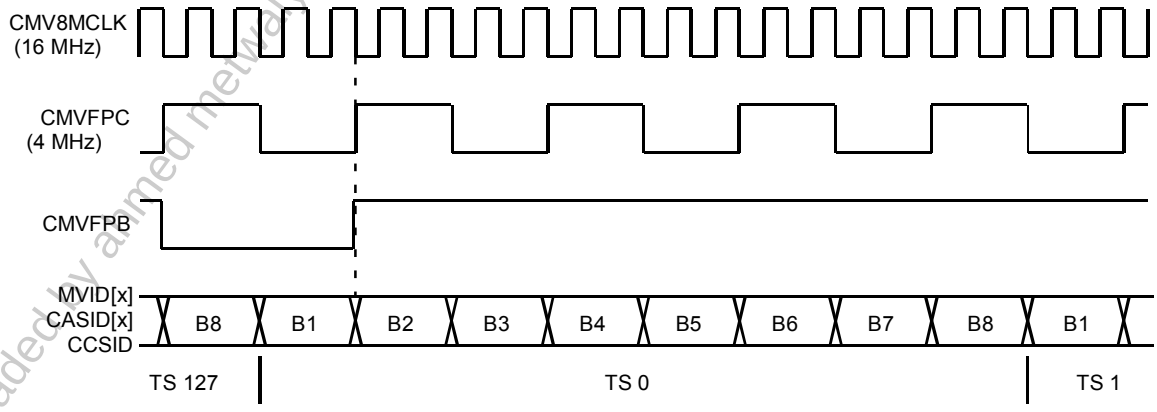
Figure 33 Egress 8.192 Mbit/s H-MVIP Link Timing



13.3 Ingress H-MVIP Link Timing

The timing relationship of the common 8M H-MVIP clock, CMV8MCLK, frame pulse clock, CMVFPC, data, MVID[x], CASID[x] or CCSID, and frame pulse, CMVFPB, signals of a link configured for 8.192 Mbit/s H-MVIP operation with a type 0 frame pulse is shown in Figure 34. The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbit/s H-MVIP operation. The TE-32 samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame. The TE-32 updates the data provided on MVID[x], CASID[x] and CCSID on every second falling edge of CMV8MCLK as indicated for bit 2 (B2) of time-slot 1 (TS 1) in Figure 34. The first bit of the next frame is updated on MVID[x], CASID[x] and CCSID on the falling CMV8MCLK clock edge for which CMVFPB is also sampled low. B1 is the most significant bit and B8 is the least significant bit of each octet.

Figure 34 Ingress 8.192 Mbit/s H-MVIP Link Timing



14 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 34 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Ambient Temperature under Bias		-40 to +85	°C
Storage Temperature	T_{ST}	-40 to +125	°C
Supply Voltage	$V_{DD1.8}$	-0.3 to + 3.6	V_{DC}
Supply Voltage	$V_{DD3.3}$	-0.3 to + 6.0	V_{DC}
Voltage on Any Pin	V_{IN}	-0.3 to 6.0	V_{DC}
Static Discharge Voltage		±1000	V
Latch-Up Current		±100	mA
DC Input Current	I_{IN}	±20	mA
Lead Temperature		+230	°C
Junction Temperature	T_J	+150	°C

Notes on Power Supplies:

1. VDD3.3 should power up before VDD1.8.
2. VDD3.3 should not be allowed to drop below the VDD1.8 voltage level except when VDD1.8 is not powered.

15 D.C. Characteristics

T_A = -40°C to +85°C, $V_{DD3.3}$ = 3.3V ±8%, $V_{DD1.8}$ = 1.8V ±8%
(Typical Conditions: T_A = 25°C, $V_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = 1.8V)

Table 35 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDD3.3	Power Supply	2.97	3.3	3.63	Volts	
VDD1.8	Power Supply	1.65	1.8	1.95	Volts	
VIL	Input Low Voltage	0		0.8	Volts	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	0	0.1	0.4	Volts	VDD = min, IOL = -4mA for D[7:0], CASID[1:8], CCSID[1:3], TS0ID, TDO and INTB, IOL = -8mA for SDDATA[3:1], SDDP, SDPL, SDV5, MVID[5:8]/SDDATA[4:7], MVID[4]/SDDATA[0], MVID[3]/SAJUST_REQ, MVID[2]/SBIACT, MVID[1]/SDC1FP, LAC1FPO, LADATA[7:0], LADP, LAPL, IOL = -2mA for others. Note 3
VOH	Output or Bidirectional High Voltage	2.4		VDD3.3	Volts	VDD = min, IOH = 4mA for D[7:0], CASID[1:8], CCSID[1:3], TS0ID, TDO and INTB, IOH = 8mA for SDDATA[3:1], SDDP, SDPL, SDV5, MVID[5:8]/SDDATA[4:7], MVID[4]/SDDATA[0], MVID[3]/SAJUST_REQ, MVID[2]/SBIACT, MVID[1]/SDC1FP, LAC1FPO, LADATA[7:0], LADP, LAPL, IOH = 2mA for others. Note 3
VT+	Reset Input High Voltage	2.0			Volts	TTL Schmidt
VT-	Reset Input Low Voltage			0.6	Volts	
VTH	Reset Input Hysteresis Voltage		TBD		Volts	

Symbol	Parameter	Min	Typ	Max	Units	Conditions
IILPU	Input Low Current	+20		+300	µA	VIL = GND. Notes 1, 3
IIHPU	Input High Current	-10		+10	µA	VIH = VDD. Notes 1, 3
IILPD	Input Low Current for Input A[12]	-10		+10	µA	VIL = GND. Notes 3, 4
IIHPD	Input High Current for Input A[12]	+20		+350	µA	VIH = VDD. Notes 3, 4
IIL	Input Low Current	-10		+10	µA	VIL = GND. Notes 2, 3
IIH	Input High Current	-10		+10	µA	VIH = VDD. Notes 2, 3
CIN	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
CIO	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
IDDOP1	Operating Current IDD1.8 IDD3.3		 340 5	 500	mA	VDD = 3.63 V, Outputs Unloaded, SBI System Interface
IDDOP2	Operating Current IDD1.8 IDD3.3		 340 5	 500	mA	VDD = 3.63 V, Outputs Unloaded, H-MVIP System Interface

Notes on D.C. Characteristics

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bi-directional pin with internal pull-down resistor.

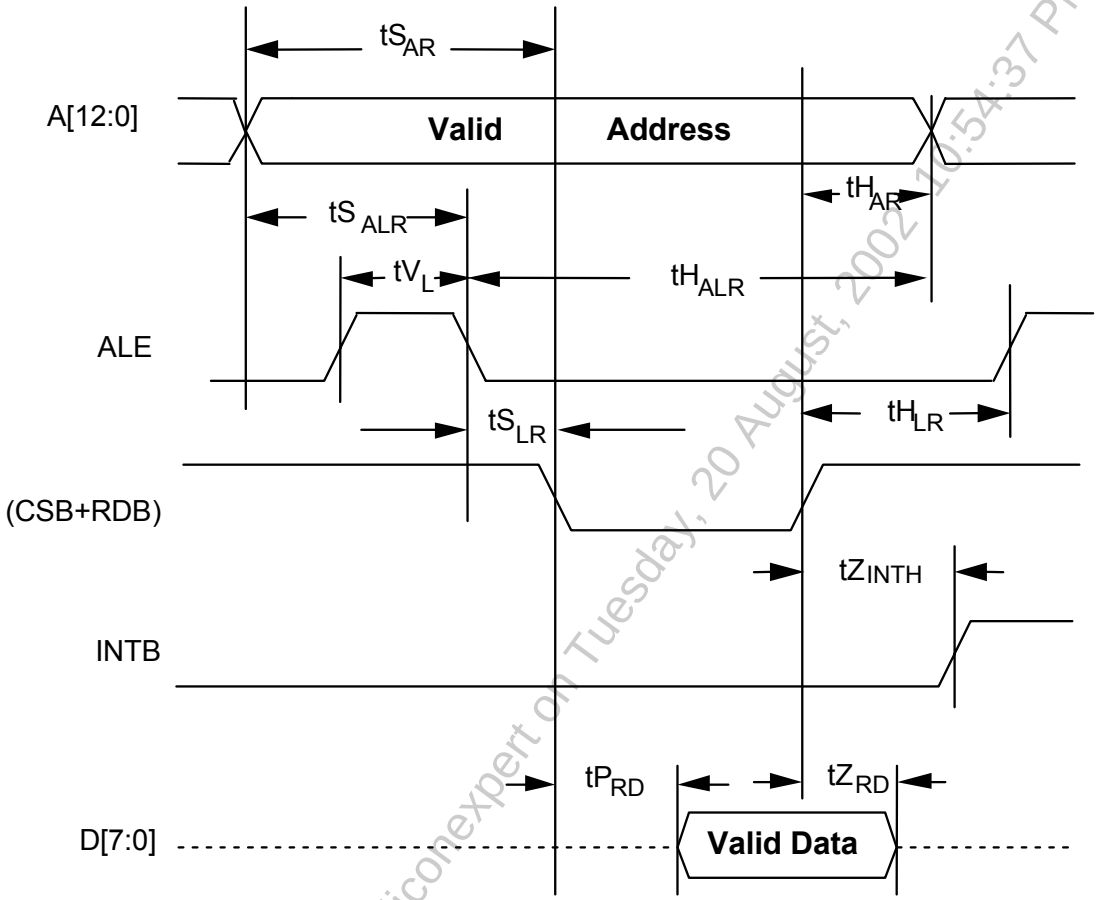
16 Microprocessor Interface Timing Characteristics

(T_A = -40°C to +85°C, $V_{DD3.3}$ = 3.3V ±8%, $V_{DD1.8}$ = 1.8V ±8%)

Table 36 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	10		ns
tHAR	Address to Valid Read Hold Time	5		ns
tSALR	Address to Latch Set-up Time	10		ns
tHALR	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns
tSLR	Latch to Read Set-up	0		ns
tHLR	Latch to Read Hold	5		ns
tPRD	Valid Read to Valid Data Propagation Delay		30	ns
tZRD	Valid Read Negated to Output Tri-state		20	ns
tZINTH	Valid Read Negated to Output Tri-state		50	ns

Figure 35 Microprocessor Interface Read Timing



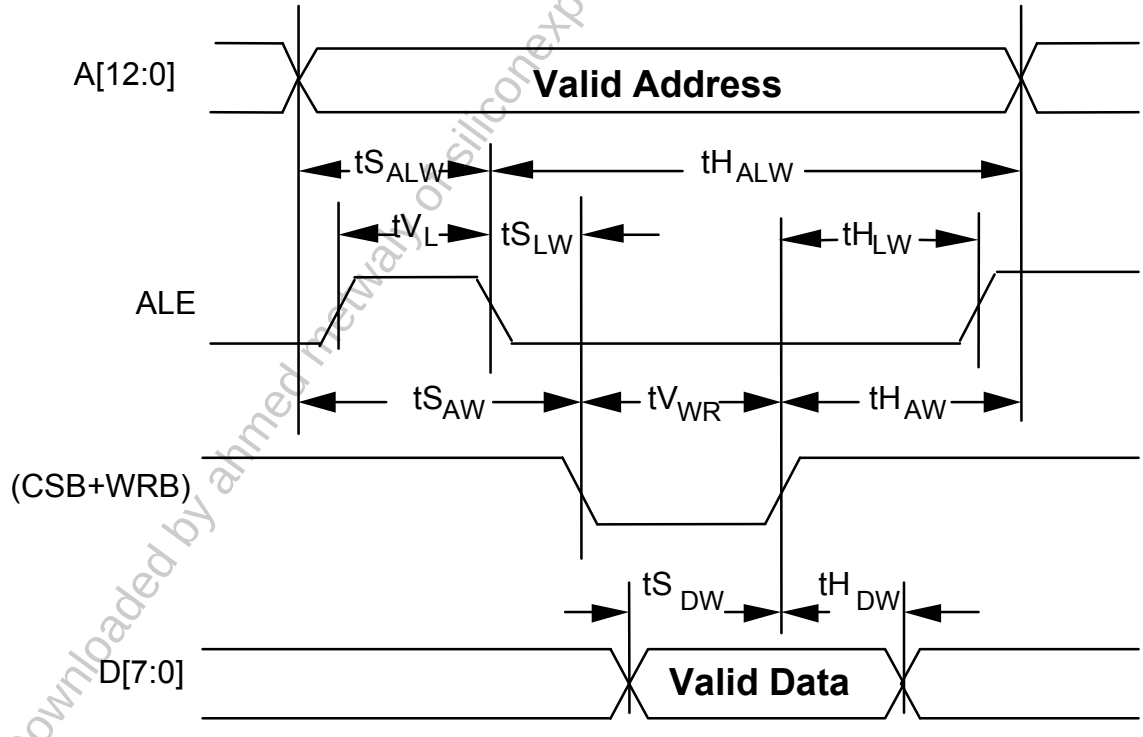
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable.
5. Parameter tHAR is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 37 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	10		ns
tSDW	Data to Valid Write Set-up Time	20		ns
tSALW	Address to Latch Set-up Time	10		ns
tHALW	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns
tSLW	Latch to Write Set-up	0		ns
tHLW	Latch to Write Hold	5		ns
tHDW	Data to Valid Write Hold Time	5		ns
tHAW	Address to Valid Write Hold Time	5		ns
tVWR	Valid Write Pulse Width	40		ns

Figure 36 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, tSLW and tHLW are not applicable.
3. Parameter tHAW is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17 TE-32 Timing Characteristics

(T_A = -40°C to +85°C $V_{DD3.3}$ = 3.3V ±8%, $V_{DD1.8}$ = 1.8V ±8%)

Table 38 RSTB Timing

Symbol	Description	Min	Max	Units
tVRSTB	RSTB Pulse Width	100		ns

Figure 37 RSTB Timing

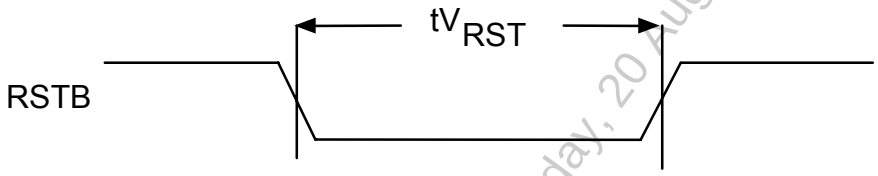


Table 39 Line Side SBI Bus Input Timing (Figure 41)

Symbol	Description	Min	Max	Units
	LREFCLK Frequency	19.44 -50 ppm	19.44 +50 ppm	MHz
	LREFCLK Duty Cycle	40	60	%
	LREFCLK skew relative to SREFCLK	-5	5	ns
tS_{LSBI}	All Line Side SBI BUS Inputs Set-Up Time to LREFCLK	5		ns
TH_{LSBI}	All Line Side SBI BUS Inputs Hold Time to LREFCLK	1		ns

Notes on Line Side SBI Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Figure 38 Line Side SBI BUS Input Timing

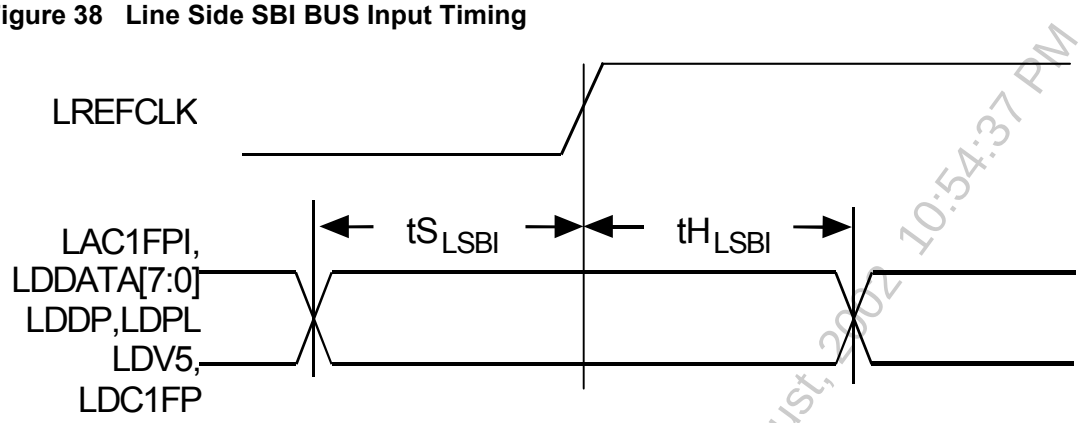


Table 40 Line Side SBI Bus Output Timing (Figure 39 and Figure 40)

Symbol	Description	Min	Max	Units
t_{PLSBI}	LREFCLK rising to all Line Side SBI BUS Outputs Valid	3	20	ns
t_{ZLSBI}	LREFCLK rising to all Line Side SBI BUS tristateable Outputs going tristate	3	20	ns
$T_{PLSBIOE}$	LREFCLK rising to all Line Side SBI BUS tristateable Outputs going valid from tristate	0	14	ns

Notes on Line Side SBI Bus Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 100 pF load on all the outputs.
3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.
4. The propagation delay, t_{PLSBI}, should be used when Line Side SBI bus outputs are always driven as configured by LADDOE in the Bus Configuration register. Note that under any specific operating condition, t_{ZLSBI} is guaranteed to be less than $t_{PLSBIOE}$.

Figure 39 Line Side SBI BUS Output Timing

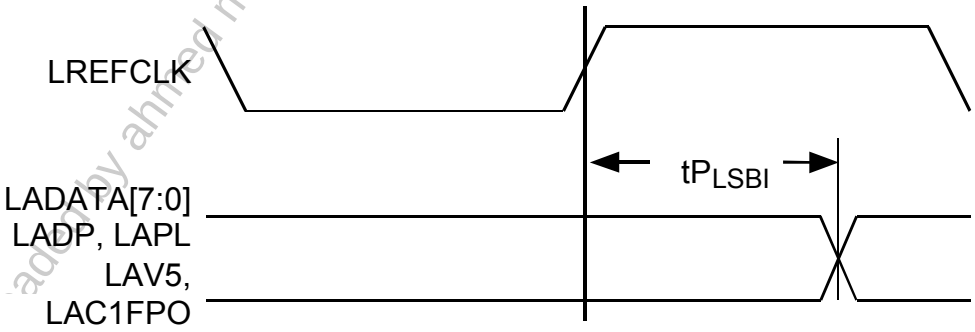


Figure 40 Line Side SBI BUS Tristate Output Timing

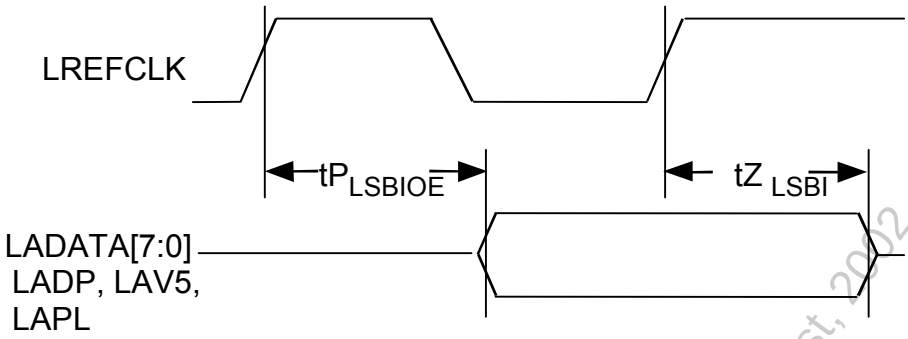


Table 41 System Side SBI ADD BUS Timing 19.44 MHz (Figure 41)

Symbol	Description	Min	Max	Units
	SREFCLK Frequency	19.44 -50 ppm	19.44 +50 ppm	MHz
	SREFCLK Duty Cycle	40	60	%
$t_{SSBIADD}$	All SBI ADD BUS Inputs Set-Up Time to SREFCLK	4		ns
$t_{HSBIADD}$	All SBI ADD BUS Inputs Hold Time to SREFCLK	0		ns
$t_{PSBIADD}$	SREFCLK to SAJUST_REQ Valid	2	15	ns
$t_{ZSBIADD}$	SREFCLK to SAJUST_REQ Tristate	2	15	ns

Table 42 System Side SBI ADD BUS Timing 77.76 MHz (Figure 41)

Symbol	Description	Min	Max	Units
	SREFCLK Frequency	77.76 -50 ppm	77.76 +50 ppm	MHz
	SREFCLK Duty Cycle	40	60	%
$t_{SSBIADD}$	All SBI ADD BUS Inputs Set-Up Time to SREFCLK	2.7		ns
$t_{HSBIADD}$	All SBI ADD BUS Inputs Hold Time to SREFCLK	0		ns
$t_{PSBIADD}$	SREFCLK to SAJUST_REQ Valid	1	6	ns
$t_{ZSBIADD}$	SREFCLK to SAJUST_REQ Tristate	1	6	ns

Notes on System Side SBI Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Figure 41 System Side SBI ADD BUS Timing

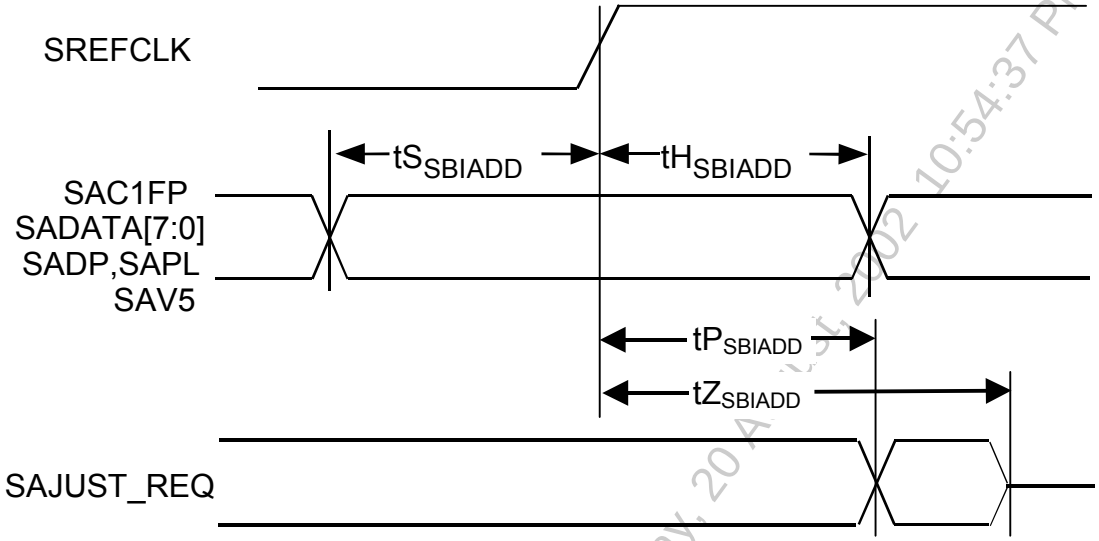


Table 43 System Side SBI DROP BUS Timing 19.44 MHz (Figure 42 and Figure 43)

Symbol	Description	Min	Max	Units
$^{t}S_{SBIDROP}$	SDC1FP Set-Up Time to SREFCLK	4		ns
$^{t}H_{SBIDROP}$	SDC1FP Hold Time to SREFCLK	0		ns
$^{t}P_{SDC1FP}$	SREFCLK to SDC1FP Output Valid	2	17	ns
$^{t}P_{SBIDROP}$	SREFCLK to All SBI DROP BUS Outputs (except SDC1FP) Valid	2	17	ns
$^{t}Z_{SBIDROP}$	SREFCLK to All SBI DROP BUS Outputs (except SDC1FP) Tristate	2	16	ns
$^{t}P_{OUTEN}$	SBIDET[1] and SBIDET[0] low to All SBI DROP BUS Outputs Valid	0	17	ns
$^{t}Z_{OUTEN}$	SBIDET[1] and SBIDET[0] high to All SBI DROP BUS Outputs Tristate	0	16	ns
$^{t}S_{DET}$	SBIDET[n] Set-Up Time to SREFCLK	4		ns
$^{t}H_{DET}$	SBIDET[n] Hold Time to SREFCLK	0		ns

Table 44 System Side SBI DROP BUS timing 77.76 MHz (Figure 42 and Figure 43)

Symbol	Description	Min	Max	Units
$t_{SSBIDROP}$	SDC1FP Set-Up Time to SREFCLK	3		ns
$t_{HSBIDROP}$	SDC1FP Hold Time to SREFCLK	0		ns
$t_{PSDC1FP}$	SREFCLK to SDC1FP Output Valid	1	7	ns
$t_{PSBIDROP}$	SREFCLK to All SBI DROP BUS Outputs (except SDC1FP) Valid	1	7	ns
$t_{ZSBIDROP}$	SREFCLK to All SBI DROP BUS Outputs (except SDC1FP) Tristate	1	7	ns

Notes on System Side SBI Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 100 pF load on all the outputs.
3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

Figure 42 System Side SBI DROP BUS Timing

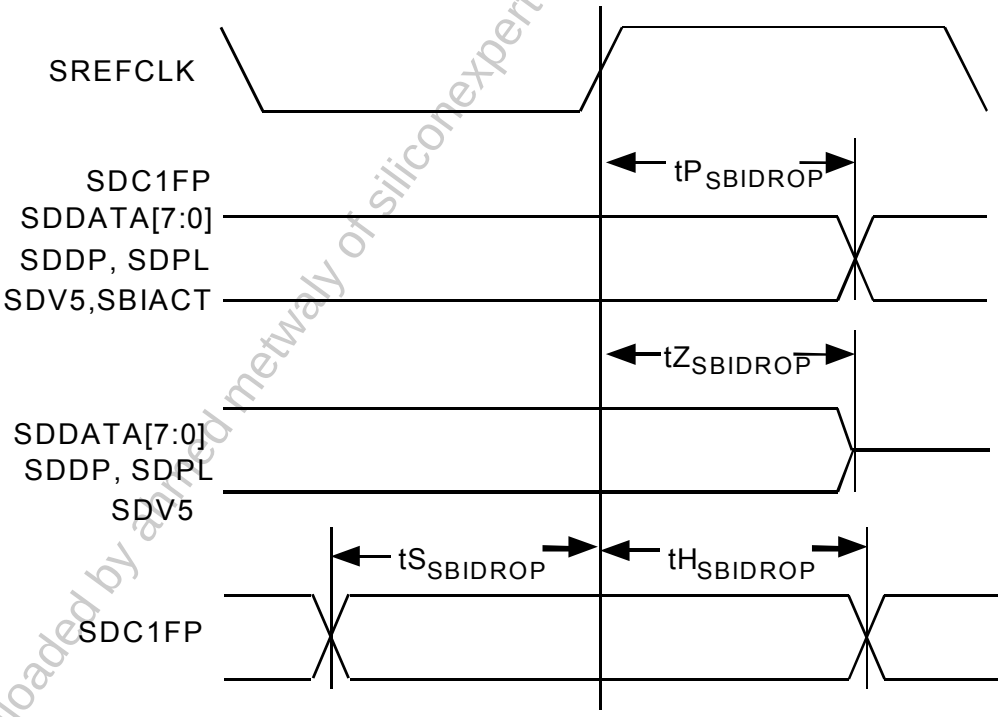


Figure 43 System Side SBI DROP BUS Collision Avoidance Timing

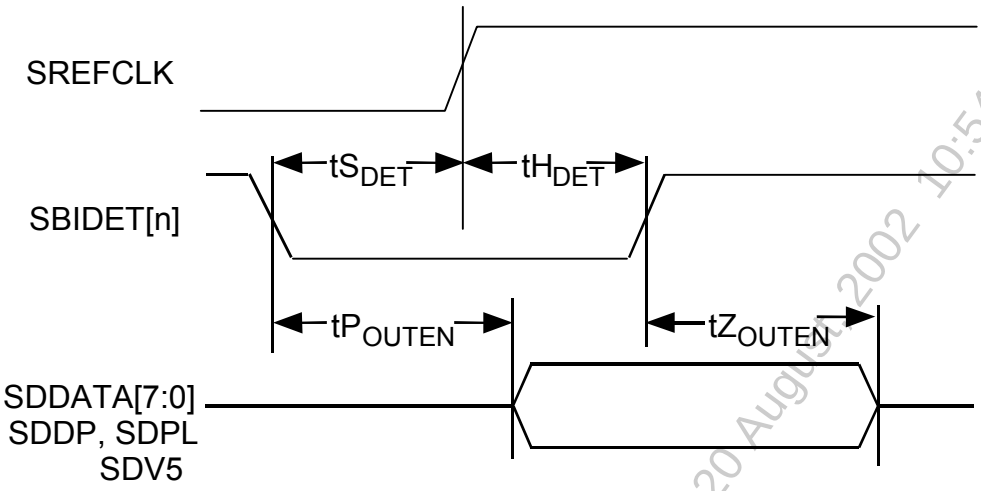


Table 45 H-MVIP Egress Timing (Figure 44)

Symbol	Description	Min	Max	Units
	CMV8MCLK Frequency (See Note 3)	16.384-50 ppm	16.384+50 ppm	MHz
	CMV8MCLK Duty Cycle	40	60	%
	CMVFPC Frequency (See Note 4)	4.092	4.100	MHz
	CMVFPC Duty Cycle	40	60	%
$t^{P}MVC$	CMV8MCLK to CMVFPC skew	-10	10	ns
$t^{S}HMVED$	MVED[1:8], CASED[1:8], CCSED[1:3] Set-Up Time	5		ns
$t^{H}HMVED$	MVED[1:8], CASED[1:8], CCSED[1:3] Hold Time	5		ns
$t^{S}MVFPB$	CMVFPB Set-Up Time	5		ns
$t^{H}MVFPB$	CMVFPB Hold Time	5		ns

Notes on H-MVIP Egress Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. Measured between any two CMV8MCLK falling edges.
4. Measured between any two CMVFPC falling edges.

Figure 44 H-MVIP Egress Data & Frame Pulse Timing

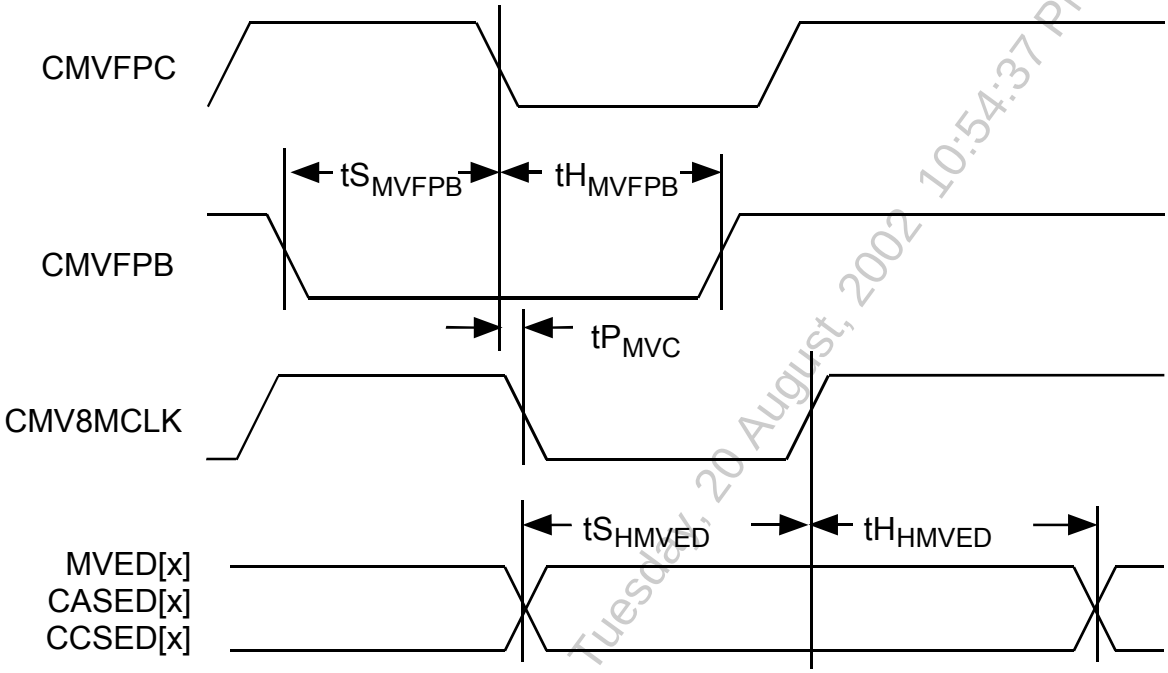


Table 46 H-MVIP Ingress Timing (Figure 45)

Symbol	Description	Min	Max	Units
$^{t}P_{HMVID}$	CMV8MCLK Low to MVID[1:8], CASID[1:8], CCSID[1:3], TS0ID Valid	4	25	ns

Notes on H-MVIP Ingress Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on all the outputs.
3. Output propagation delays of signal outputs that are specified in relation to a reference output are measured with a 50 pF load on both the signal output and the reference output.

Figure 45 H-MVIP Ingress Data Timing

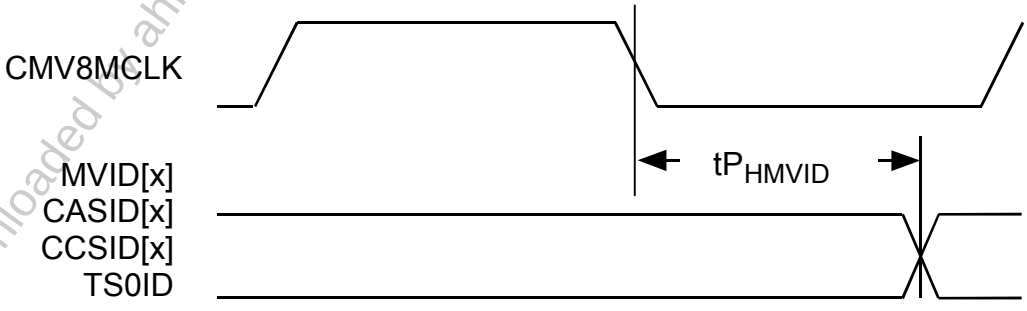


Table 47 XCLK Input (Figure 46)

Symbol	Description	Min	Max	Units
t_{LXCLK}	XCLK_T1 and XCLK_E1 Low Pulse Width[4]	8		ns
t_{HXCLK}	XCLK_T1 and XCLK_E1 High Pulse Width[4]	8		ns
t_{XCLK}	XCLK_T1 and E1_XLK Period (typically 1/37.056 MHz ± 32 ppm for XCLK_T1 and 1/49.152 MHz for XCLK_E1)	20		ns

Figure 46 XCLK Input Timing

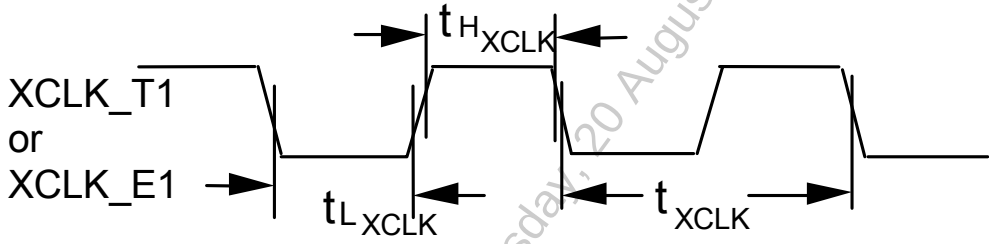
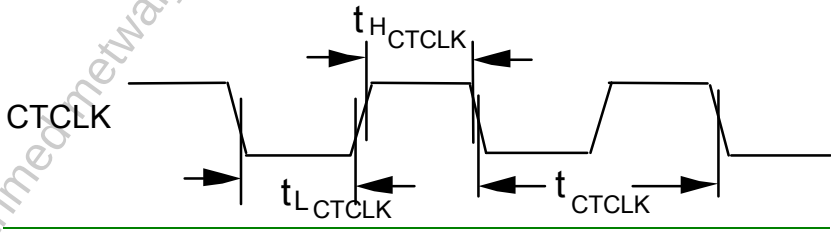


Table 48 Transmit Line Interface Timing (Figure 47)

Symbol	Description	Min	Max	Units
	CTCLK Frequency (Must be integer multiple of 8 KHz.)	0.008	2.048	MHz
t_{HCTCLK}	CTCLK High Duration	60		ns
t_{LCTCLK}	CTCLK Low Duration	60		ns

Figure 47 Transmit Line Interface Timing



Notes on Ingress and Egress Serial Interface Timing

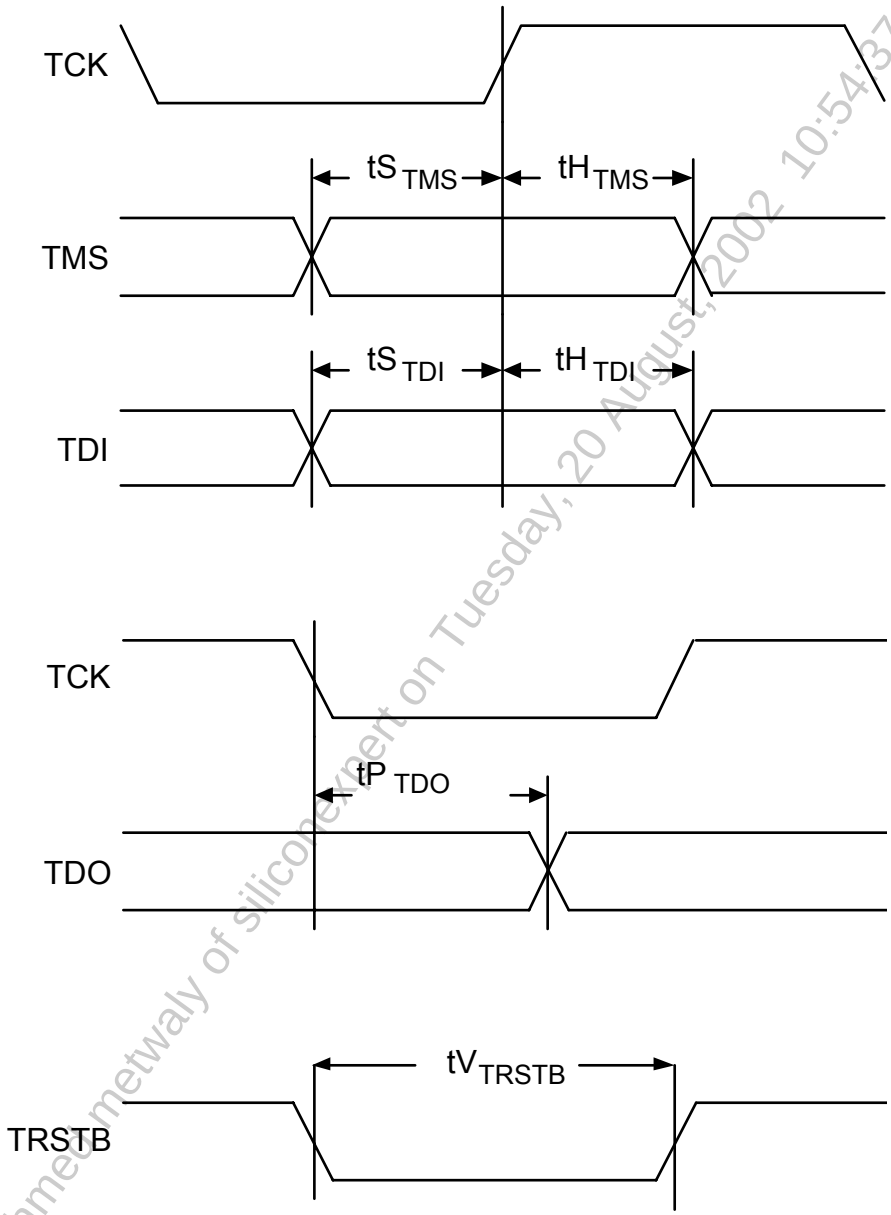
1. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.
2. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
3. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

4. Setup, hold, and propagation delay specifications are shown relative to the default active clock edge, but are equally valid when the opposite edge is selected as the active edge.
5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
6. Output propagation delays are measured with a 50 pF load on all outputs.

Table 49 JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
t_{STMS}	TMS Set-up time to TCK	50		ns
t_{HTMS}	TMS Hold time to TCK	50		ns
t_{STDI}	TDI Set-up time to TCK	50		ns
t_{HTDI}	TDI Hold time to TCK	50		ns
t_{PTDO}	TCK Low to TDO Valid	2	50	ns
t_{VTRSTB}	TRSTB Pulse Width	100		ns

Figure 48 JTAG Port Interface Timing



18 Ordering and Thermal Information

Table 50 Ordering Information

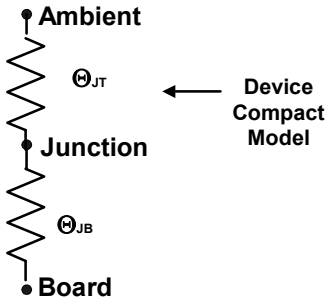
Part No.	Description
PM4332-PI	324 Plastic Ball Grid Array (PBGA)

This product is designed to operate over a wide temperature range and is suited for industrial applications such as central office equipment or in-field locations.

Maximum long-term operating junction temperature to ensure adequate long-term life	105 ^{0}C
Maximum junction temperature for short-term excursions with guaranteed continued functional performance.[1] This condition will typically be reached when local ambient reaches 70 Deg C.	125 ^{0}C
Minimum ambient temperature	-40 ^{0}C

Thermal Resistance vs Air Flow[2]			
Airflow	Natural Convection	200 LFM	400 LFM
Θ_{JA} (^{0}C/W)	18.6	15.2	12.4

Device Compact Model[3]	
Θ_{JT} (^{0}C/W)	5.6
Θ_{JB} (^{0}C/W)	11.5



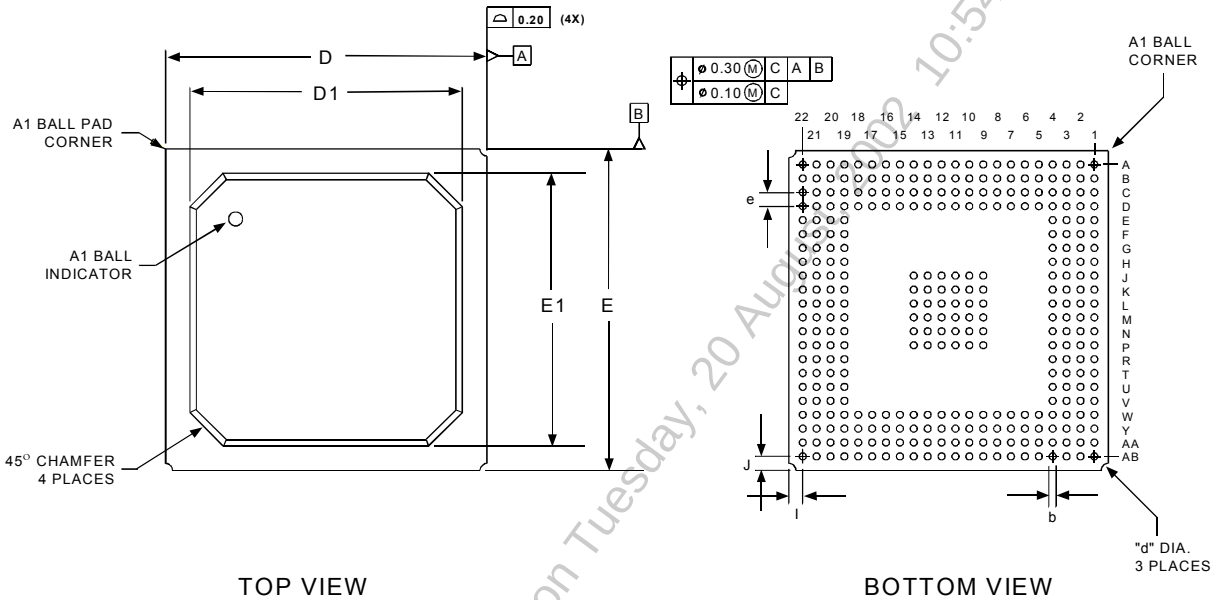
Operating power is dissipated in package (watts) at worst case power supply	
Power (watts)	1.0W

Notes

1. Short-term is understood as the definition stated in Bellcore Generic Requirements GR-63-Core.
2. Θ_{JA} , the total junction to ambient thermal resistance as measured according to JEDEC Standard JESD51 (2S2P)
3. Θ_{JB}, the junction-to-board thermal resistance and $\Theta_{JT,}$ the residual junction to ambient thermal resistance are obtained by simulating conditions described in JEDEC Standard, JESD 15-8.

19 Mechanical Information

Figure 49 324 Pin PBGA 23x23mm Body



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES COPLANARITY.
3) DIMENSION bbb DENOTES PARALLEL.

PACKAGE TYPE : 324 PLASTIC BALL GRID ARRAY - PBGA																	
BODY SIZE : 23 x 23 x 2.28 MM (4 layer)																	
Dim.	A (2 layer)	A (4 layer)	A1	A2	D	D1	C (2 layer)	C (4 layer)	E	E1	l	J	b	d	e	aaa	bbb
Min	1.82	2.07	0.40	1.12	-	19.00	0.30	0.55	-	19.00	-	-	0.50	-	-	-	-
Nom.	2.03	2.28	0.50	1.17	23.00	19.50	0.36	0.61	23.00	19.50	1.00	1.00	0.63	1.00	1.00	-	-
Max.	2.22	2.49	0.60	1.22	-	20.20	0.40	0.67	-	20.20	-	-	0.70	-	-	0.15	0.35