

Introduction

Optimized for the Altera® APEX™ II device architecture, the POS-PHY level 4 MegaCore® function (POSPHY4) interfaces cell and packet transfers between physical (PHY) and link layer devices. The POSPHY4 supports rates of up to SONET OC-192, and 10 gigabits per second (Gbps) Ethernet rates.

Features

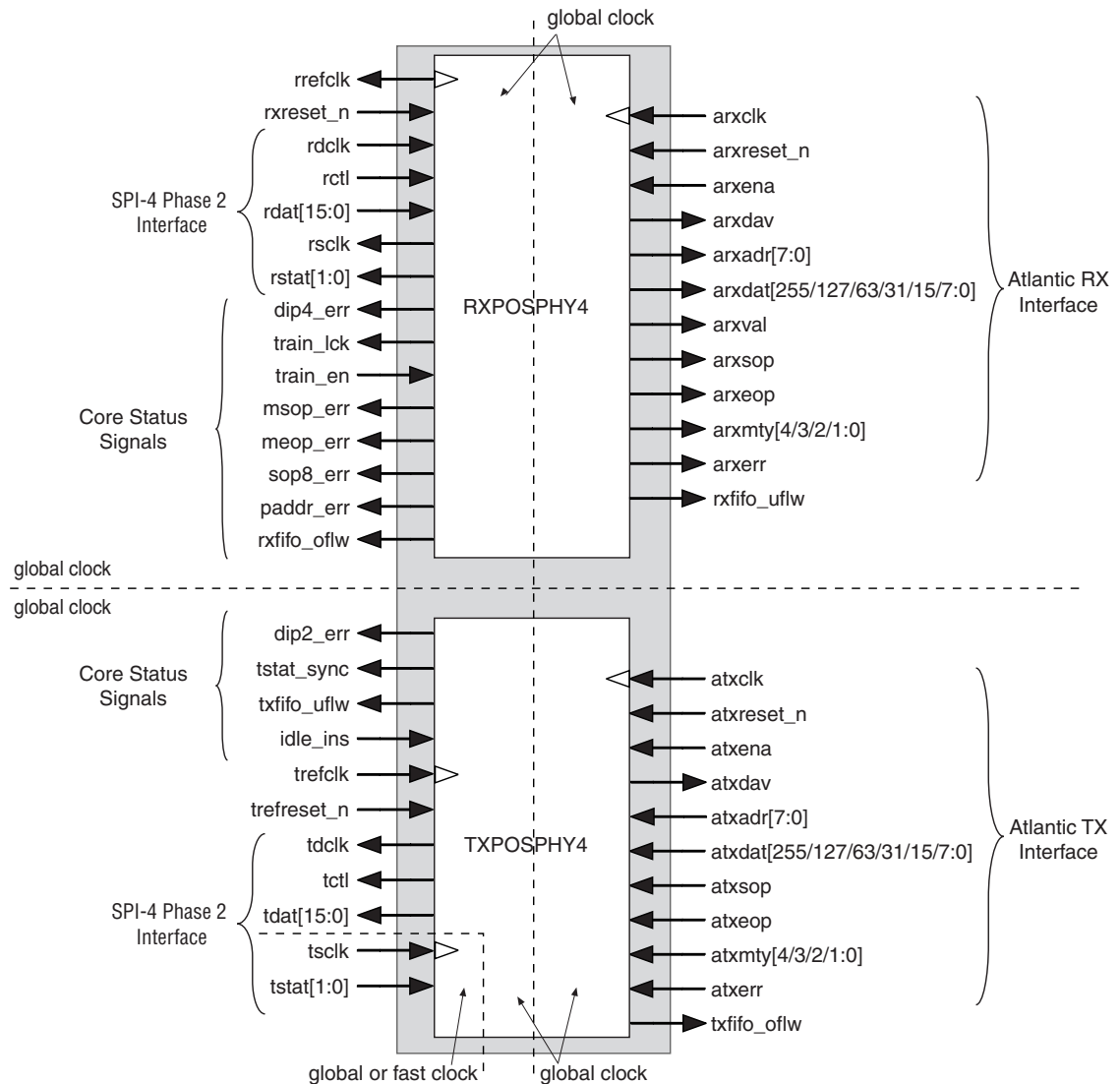
- SPI-4 Phase 2 interface data width of 16 bits (True-LVDS™ solution)
- Supports up to 832 Mbps on each LVDS channel
- Operates in single-PHY (SPHY), or multi-PHY (MPHY) mode with up to 256 ports
- Fixed start of packet (SOP) alignment significantly eases subsequent packet processing
- Configurable for receive or transmit directions
- FIFO buffer status management and indications
- Configurable FIFO buffer options (including port address optionally passed through FIFO buffer, adjustable FIFO buffer depth)
- Static alignment (training sequence required for word alignment in the receiver)
- Configurable Atlantic™ slave interface data width of 8, 16, 32, 64, 128 or 256 bits for simplified bridging with other Atlantic interface compatible cores
- Complies with all applicable standards, including:
 - Optical Internetworking Forum (OIF), *System Packet Interface Level 4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer Devices*, OIF-SPI4-02.0, January 2001.
 - PMC-Sierra Inc., *POS-PHY™ Level 4 A Saturn Packet and Cell Interface Specification for OC-192 SONET/SDH and 10 GB/s Ethernet Applications*, Issue 5 (Draft): June 2000.
 - Altera Corporation, *Atlantic Interface Specification*.

Functional Description

The POSPHY4 functions as a transmitter (TXPOSPHY4) master where data flows from the Atlantic interface to the SPI-4 interface, or as a receiver (RXPOSPHY4) slave where data flows from the SPI-4 interface to the Atlantic interface.

Figure 1 shows a block diagram of the RXPOSPHY4 and the TXPOSPHY4.

Figure 1. Block Diagram



The following lists the features for the RXPOSPHY4 and TXPOSPHY4, assuming a full-feature configuration.

RXPOSPHY4

- Static alignment for bit sampling (training sequence required for word alignment)
- Accepts packets (or cells) from the SPI-4 Phase 2 interface
- Control word processing
- Diagonal interleaved parity (DIP-4) parity error detection
- Fixed SOP alignment
- Adjustable FIFO buffer depth
- FIFO buffer status management
- Port address optionally passed through FIFO buffer

TXPOSPHY4

- Inserts training sequence
- Sends data packets (or cells) on the SPI-4 Phase 2 interface
- Inserts control words
- Generates DIP-4 parity
- Adjustable FIFO buffer depth
- FIFO buffer status management

Interfaces & Protocols

Two interfaces support the POSPHY4: the SPI-4 Phase 2 interface and the Atlantic interface. While multiple Atlantic interfaces can be used, the SPI-4 Phase 2 interface can only support a single transmitter, and/or a single receiver.

SPI-4 Phase 2 Interface

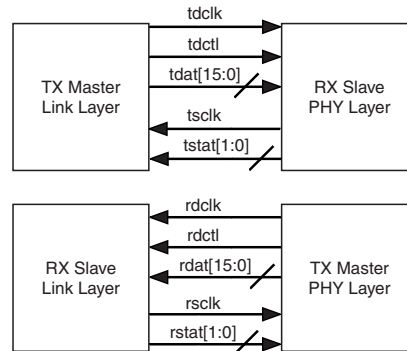
The SPI-4 Phase 2 interface is an external interface protocol developed by the Optical Internetworking Forum (OIF). The POSPHY4 complies with the static alignment requirements specified by this protocol. This interface passes data and control words in both the TX (master) and RX (slave) directions. It features a high-speed portion and a FIFO buffer status portion. The high-speed portion comprises a 16-bit data bus, a 1-bit control line, and a double data rate (DDR) clock. The FIFO buffer status portion comprises a 2-bit status channel and a clock. This interface supports a data width of 16 bits. The interface can be a PHY-link, link-link, link-PHY, or PHY-PHY connection.



For the purpose of this document, the POSPHY4 is implemented as a link layer device.

Figure 2 shows an SPI-4 Phase 2 PHY-link configuration, including a TX (master) and an RX (slave).

Figure 2. SPI-4 Phase 2 Top Level View



For further information on this interface, refer to the *System Packet Interface Level 4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer Devices*, available at <http://www.oiforum.com>.

Atlantic Interface

The Atlantic interface is a full-duplex synchronous bus protocol supporting both packets and cells. The POSPHY4 is an Atlantic interface slave using a configurable data path of 8, 16, 32, 64, 128, or 256 bits to deliver packets to the slave.

The Atlantic interface provides a connection between the FIFO buffer and neighboring logic. The width of the output bus (to FIFO buffer) is always as wide as, or wider than, the width of the input bus (Atlantic interface). The POSPHY4 FIFO buffer is used for crossing the clock domain from the Atlantic interface to the POSPHY4 reference clock.



For further information on this interface, refer to the *Atlantic Interface Functional Specification*, available at <http://www.altera.com>.

Generating Variants

Table 1 lists the optional features available to generate/request all POSPHY4 variants.

Table 1. Optional Features		
Options	Parameters	Choices
Data Flow Direction —Receive (RX) data flows from the SPI-4 interface to the Atlantic interface. Transmit (TX) data flows from the Atlantic interface to the SPI-4 interface.	DFLOW	RX/TX
Atlantic Data Width —Atlantic data bus width	ATLDW	8, 16, 32, 64, 128, 256
Calender Length —Number of ports and FIFO buffers (1)	CALLEN	1 - 256
Embedded Address —Send/receive address with data through the FIFO buffer (2)	EADDR	Yes /No
FIFO Buffer Depth —Number of elements	FDEPTH	0, 256, 512
FIFO Pipeline —FIFO buffer is pipelined for increased performance.	FPIPELINE	Yes/No
Almost Empty —Starving to Hungry threshold indications for each PHY port (2)	AE	$0 < AE < FDEPTH/2$
Almost Full —Hungry to Satisfied threshold indications for each PHY port (2)	AF	$FDEPTH/2 < AF < FDEPTH$
FIFO Threshold Low —FIFO buffer low watermark	FTL	$0 < FTL < FDEPTH/2$
FIFO Threshold High —FIFO buffer high watermark	FTH	$FDEPTH/2 < FTH < FDEPTH$
Calender M —Number of repeated FIFO buffer calculations before DIP-2 and framing occurs. (2)	CALM	1 - 255
Maxburst 1 —Number of 16-byte words that can be transmitted when the FIFO buffer is Starving. (2)	MB1	8 - 127
Maxburst 2 —Number of 16-byte words that can be transmitted when the FIFO buffer is Hungry. This number must be less than or equal to MB1. (2)	MB2	8 - 127
MaxT —Training Sequence Interval. The interval depends on the internal t_{refclk} cycle. If the chosen interval is 1, the sequence occurs every t_{refclk} cycle; if the chosen interval is 2, the sequence occurs every 2 t_{refclk} cycles. (2)	MAXT	8 - 2,048
Training Pattern Repetitions —ALPHA (α) is the number of repetitions of the training pattern sequence. (2)	ALPHA	1 - 255
Transmit Bandwidth Optimization —Yes inserts a single EOP/SOP control word between packets. No inserts of an EOP control word followed by a maximum of six IDLEs and a SOP control word between packets. (3)	TXBOPT	Yes/No

Notes:

- (1) If one port is chosen, the POSPHY4 operates in SPHY mode; if 2 to 256 ports are chosen, the POSPHY4 operates in MPHY mode. (The MPHY mode is not supported in version 1.0.0p1.)
- (2) These parameters do not materially affect the size of the POSPHY4.
- (3) TXBOPT=Yes is not supported in version 1.0.0p1.

Performance

Table 2 lists the estimated resources and speed of a SPHY POSPHY4 MegaCore function. These timing results were obtained using the Quartus II software version 1.1, and an APEX II EP2A15-7 device.

Table 2. SPHY Configuration		Utilization		Performance
Direction	Parameters	LE	ESB	f _{MAX} (MHz)
RXPOSPHY4	ATLDW=128, CALLEN=1, EADDR=No, FDEPTH=256, FTL=5, FTH=251, AE=30, AF=200, CALM=10, MB1=61, MB2=50, MAXT=2048, ALPHA=1, FPIPELINE=Yes	7,484	17	100
TXPOSPHY4	ATLDW=128, CALLEN=1, EADDR=No, FDEPTH=256, FTL=5, FTH=251, AE=30, AF=200, CALM=10, MB1=61, MB2=50, MAXT=2048, ALPHA=1, TXBOPT=No, FPIPELINE=Yes	2,955	17	100

Typical Applications

Figure 3 shows a POSPHY4 configured for link layer, in an APEX II device.

Figure 3. POSPHY4 as Link Layer Configuration

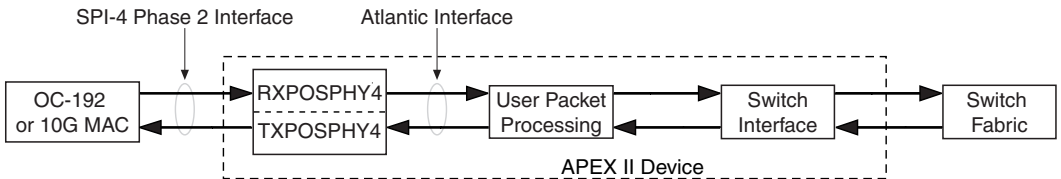
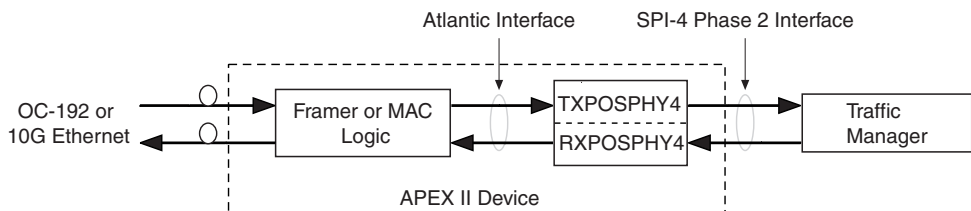


Figure 4 illustrates the POSPHY4 configured for PHY layer, in an APEX II device.

Figure 4. POSPHY4 as PHY Layer Configuration



Licensing

A license is not required to perform the following trial operations using your own custom logic:

- Instantiation
- Place-and-route
- Static timing analysis
- Simulation on third-party simulator

Only when you are ready to generate programming files, do you need to obtain a license through your local Altera sales representative.



All current variants use a single license with ordering code: PLSM-POSPHY4.

Deliverables

The following elements are provided with the POSPHY4 package:

- Data sheet
- User guide
- Atlantic interface functional specification
- Encrypted gate level netlist
- Place-and-route constraints (where necessary)
- Secure RTL simulation model
- Demo testbench
- Access to problem reporting system



If your chosen variant (configuration) is not included as part of the downloaded package, the MegaWizard® Plug-In generates the necessary text to request this variant. Forward this text to telecom@altera.com for processing.



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