SPT2110 NTSC/PAL VIDEO DECODER

KEY FEATURES

- Composite Video Input and S-Video Input
  - Composite Mode: 9-bit x 1 Channel Input
  - S-Video Mode: 9-bit x 2 Channel Input
- NTSC/PAL System Compatible
- Three Sample Rate Modes
  - Square Pixel Sampling
  - CCIR-601
  - 4Fsc Sampling (NTSC Only)
- Digital Outputs
  - 16-bit YCrCb (4:2:2)
  - 24-bit RGB (4:4:4)
  - HSYNC and HBLANK
  - VSYNC and VBLANK
  - ODD Field
- Integrated Sync Detect and Genlock Circuitry
- Selectable Color Separation Filtering
  - Trap Filter
  - 1H Comb Filter (NTSC Only)
  - 2H Comb Filter (NTSC Only)
- Picture Quality Adjustments:
  - Brightness - Peaking
  - Contrast - Hue
  - Contour - Saturation
- Standard MPU Host Interface
- Single +3.3 V Supply
- 230 mW Power Dissipation
- 100-lead PQFP Package

GENERAL DESCRIPTION

The SPT2110 is an NTSC/PAL-compatible video decoder capable of converting 9-bit digitized composite video or two channel 9-bit digitized S-Video into video data conforming to CCIR-601, YCrCb 4:2:2 or RGB 4:4:4 standards.

DIGITAL INPUT BUSSES

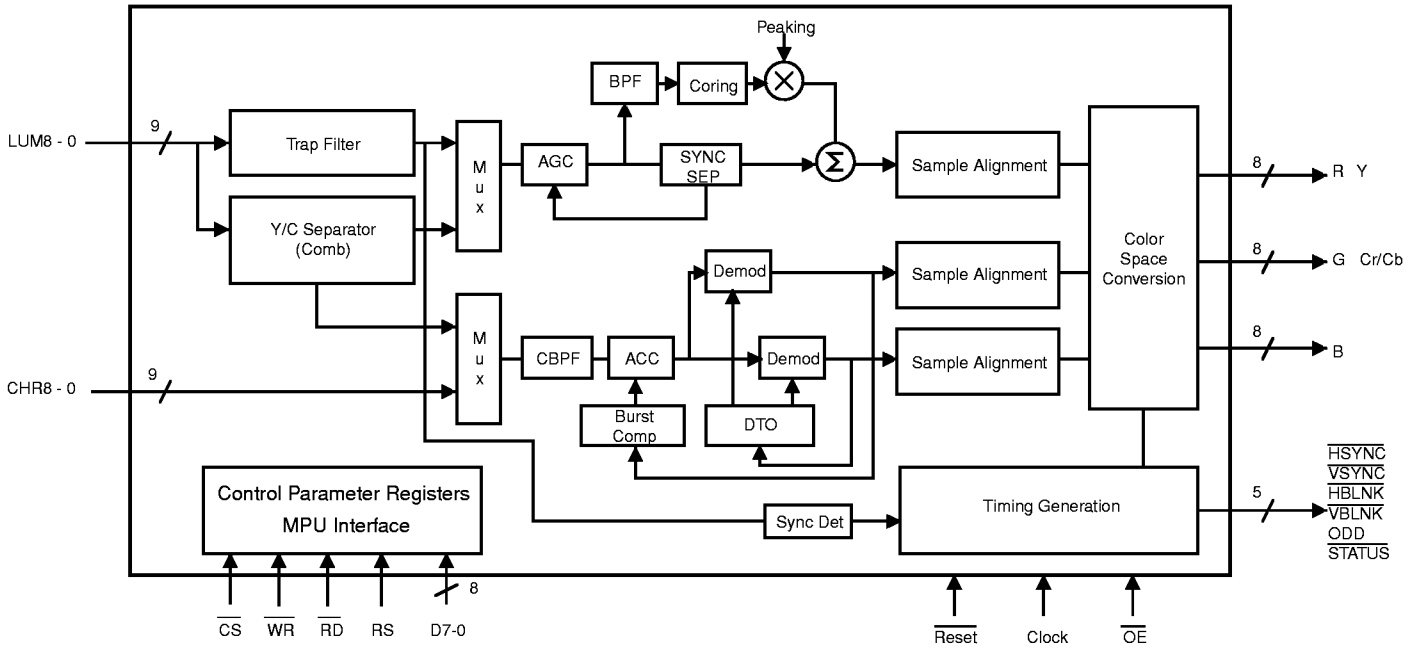
The SPT2110 Video Decoder has two 9-bit wide digital input busses. It accepts 9-bit wide digitized composite video or two 9-bit wide (Y/C) digitized S-Video data streams. This data is typically generated by the SPT7852 10-bit dual ADC as part of the NTSC/PAL Video Chip Set. The LUM8...0 bus accepts digitized composite video or the luminance digitized data of an S-Video signal. The CHR8...0 bus accepts digitized data of the chrominance signal of an S-Video signal.

LUMINANCE CHANNEL DESCRIPTION

The luminance digital data is presented to a trap filter and comb filter. The comb filter separates the color information from the luminance. The output of the comb filter is sent on to the chrominance channel for processing . (See the Chrominance Channel description). The trap filter suppresses the color information from the baseband video.

Following of the trap filter the luminance data is presented to a synchronization detection circuit. This circuitry also looks at the color burst signal to determine which field is being

SPT2110 BLOCK DIAGRAM



processed (odd or even). The detected synchronization signals are further processed and used for generating the synchronization signals for output from the decoder. (See the discussion for Data Output.)

The luminance channel has an automatic gain control (AGC) circuit that is controlled by the sync separation circuit, which follows the AGC circuit . The amplitude of the synchronization levels is used to determine the gain factor of the AGC.

From there the luminance data is sent through a digital bandpass filter (BPF). This is used to gain or attenuate the luminance signal band. A coring circuit following the BPF sets the minimum data transitions levels. A peaking control factor is incorporated to enhance the high frequency of the luminance signal. The luminance signal is processed by the sample alignment circuit. This ensures the same number of pixels per line and field. The last major processing is done in the color space conversion circuit. Further signal processing is done in the decoder. The luminance signals are translated from NTSC/PAL to YCrCb or RGB color space.

CHROMINANCE CHANNEL DESCRIPTION

The chrominance channel processes digital data from either the comb filter (chrominance separation filter) or directly from the 9-bit chrominance digital input bus. The chrominance channel immediately sends the chrominance data through a digital chrominance bandpass filter.

From there the signal is put through an automatic color correction (ACC) circuit, controlled by circuitry that is monitoring the amplitude and phase of the color burst signal (color reference). The carrier-suppressed color quadrature signal is digitally demodulated by two separate quadrature phase demodulators, with the color carrier reinserted by a discrete time oscillator (DTO) to extract the baseband chrominance difference signals.

Both color difference signals are sample aligned with the luminance signal data (as described above) and presented to the color space conversion circuit to translate them to the CrCb or RGB color space.

DIGITAL TIMEBASE GENERATION

The SPT2110 uses a fixed clock data sampling scheme with digital phase-locked loop to control internal digital shifting of the sampled data. The luminance and chrominance signal data are processed by the sample alignment circuit to ensure the same number of pixels per line and field. The robust timebase generation circuitry can operate over a wide range of video source quality levels including VCR fast-forward and paused modes.

RGB / YC_RC_B AND VIDEO TIMING SIGNAL DATA OUTPUTS

Digital output data is brought out on three 8-bit wide data busses. Two of the busses are used for YCrCb format data output, and all three busses are used for RGB format data output. Timing signals are available on discrete tri-statable outputs. These include horizontal sync, vertical sync, horizontal blanking, vertical blanking, even/odd field status and Cr/Cb synchronization flag.

OTHER INFORMATION

The SPT2110 operates off of a +3.3 V power supply and dissipates only 230 mW of power, which makes it ideal for various battery based applications. It is available in a 100-lead plastic quad flat pack (PQFP) package and operates over the commercial temperature range.

SPT2110 COMMAND REGISTERS

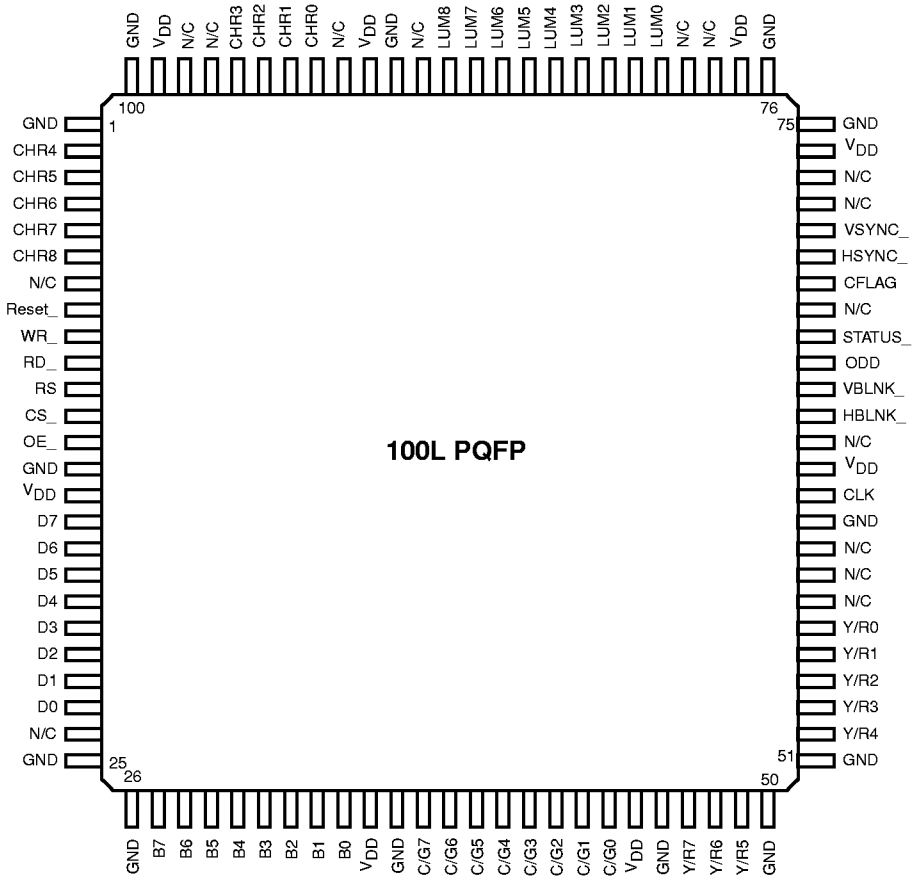
The SPT2110 is fully programmable through a standard MPU interface control multiplexed 8-bit address and data bus. Interface to the command register bus is provided through standard control lines: Chip Select, Read Control, Write Control, Register Select (for selecting address versus data bus) and Data Bus Lines.

The command registers allow for real-time control of the SPT2110 input/output formats, video timing and video processing parameter values. Please refer to the SPT2110 data sheet for detailed register functional descriptions and programming instructions. The following is a summary of the command register functions for the SPT2110.

SPT2110 REGISTER FUNCTION SUMMARY

Register	Address	Bit	Function
CHIP MASTER CONTROL			
RESET	00H	1	Data Path Reset
		0	Reset Device
INPUT MODE CONTROL			
MODEA	01H	3	Select NTSC/PAL
		2, 1	Select Sampling Frequency
		0	CVBS / S-Video Mode Select
OUTPUT MODE CONTROL			
MODEB	02H	6	Timing Signal Sync / Free Run Mode Select
		5	Select Output Data Format of Cr, Cb (Binary/2's Complement)
		4	YC / RGB Output Mode Select
		3	Select Data Offset of 16
		2	Select Range of Output Limit
		1	Reserved
		0	Order of Cr, Cb Output
FILTER CONTROL			
YCSEL	03H	1, 0	Select YC Separation Method
TIMING SIGNAL POLARITY CONTROL			
SYNCP	04H	5	Set CBFlag Polarity
		4	Set ODD Polarity
		3	Set VBLNK Polarity
		2	Set VSYNC Polarity
		1	Set HBLNK Polarity
		0	Set HSYNC Polarity
PICTURE QUALITY CONTROL			
AGC	05H	0	Automatic Gain Control On/Off
PBAND	06H	2 - 0	Select Contour Compensation Frequency Band
CORE	07H	2 - 0	Core Ring Level
PFACT	08H	2 - 0	Peaking Compensation Coefficient
CGAIN	09H	7 - 0	Color Signal Gain Value
ACC	0AH	0	Automatic Color Control On/Off
CKILL	0BH	0	Select Color Kill Mode
HUE	0CH	7 - 0	Hue Adjustment
VIDEO OUTPUT TIMING SIGNAL CONTROL			
HBKBG	0DH	7 - 0	Horizontal Blank Start Position Adjustment
HBKWD	0EH	7 - 0	Horizontal Blank Width Adjustment
VBKBG	0FH	7 - 0	Vertical Blank Start Position Adjustment
VBKEN	10H	7 - 0	Vertical Blank End Position Adjustment
LUMINANCE CONTROLS			
CONT	11H	7 - 0	Contrast Adjustment
BRI	12H	5 - 0	Brightness Adjustment
OUTPUT BUFFER STATE CONTROL			
HZSET	13H	7	Set R/Y and G/C Output to High Impedance
		6	Set B Output to High Impedance
		5	Set HSYNC Output to High Impedance
		4	Set VSYNC Output to High Impedance
		3	Set HBLNK Output to High Impedance
		2	Set VBLNK Output to High Impedance
		1	Set ODD Output to High Impedance
		0	Set STATUS and CFLAG Outputs to High Impedance

SPT2110 PIN OUT



SPT2110 NTSC/PAL VIDEO DECODER PIN FUNCTIONS

Signal Name	Pin Numbers	I/O	Function
Data I/O			
LUM8...0	80-88	I	Composite Video or Luminance Signal Input (LUM0 = LSB)
CHR8...0	2-6, 93-96	I	Chrominance Signal Input (CHR0 = LSB)
Y/R7...0	47-49 52-56	O	Luminance (Y) Data or R Data Output (RGB Mode) (High Z when OE_ = 1) (Y/R0 = LSB)
C/G7...0	37-44	O	Color (Cr/Cb) Data or G Data Output (RGB Mode) (High Z when OE_ = 1) (C/G0 = LSB)
B7...0	27-34	O	B Data Output (RGB Mode) (High Z when OE_ = 1) (B0 = LSB)
Clock and Sync Signals			
CLOCK	61	I	Clock Input
HSYNC_	70	O	Horizontal Sync Signal (High Z when OE_ = 1)
VSYNC_	71	O	Vertical Sync Signal (High Z when OE_ = 1)
HBLNK_	64	O	Horizontal Blanking Signal (High Z when OE_ = 1)
VBLNK_	65	O	Vertical Blanking Signal (High Z when OE_ = 1)
ODD	66	O	Field Identification Signal (EVEN/ODD) (High Z when OE_ = 1)
CFLAG	69	O	Cr, Cb Signal Sync (Logic 0 = Cr; Logic 1 = Cb)
STATUS_	67	O	Flag indicating sync detection when low.

SPT2110 NTSC/PAL VIDEO DECODER PIN FUNCTIONS - CONTINUED

Signal Name	Pin Numbers	I/O	Function
MPU Interface			
OE_	13	I	Output Enable: 0-Normal Output Mode 1-Specified output pins set to high impedance state
CS_	12	I	Chip Select (Active Low)
RS	11	I	Register Select: 0-Address register access 1-Address register specified data register accessed
RD_	10	I	Read Control (Active Low)
WR_	9	O	Write Control (Active Low)
D7...0	16-23	I/O	Data Bus/Register Address
RESET_	8	I	Reset Terminal (Active Low)
Power Supply Connections			
V_{DD}	15, 35, 45, 62, 74, 77, 91, 99	-	+3.3 V Power Supply
V_{SS}	1, 14, 25, 26, 36, 46, 50, 51, 60, 75, 76, 90, 100	-	Digital Ground
N/C	7, 24, 57-59,63, 68, 72, 73,78, 79, 89, 92, 97, 98	-	No Connect