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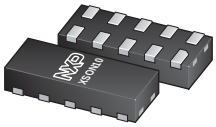


PUSB3F4-TBR

ESD protection for ultra high-speed interfaces

Rev. 1 — 6 October 2011 Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as High-Definition Multimedia Interface (HDMI), DisplayPort, SuperSpeed USB, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes high-level ESD protection diodes for ultra high-speed signal lines and is encapsulated in a 4-channel XSON10 Pb-free package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.5 pF. These diodes provide protection to downstream components from ESD voltages up to ±8 kV contact according to IEC 61000-4-2, level 4.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- System ESD protection for USB 2.0 and USB SuperSpeed 3.0, HDMI 1.3 and HDMI 1.4, DisplayPort, eSATA and LVDS
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±8 kV according to IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.5 pF for each channel
- 4-channel, XSON10 Pb-free package
- Design-friendly ’pass-thru’ signal routing

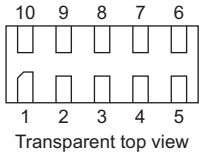
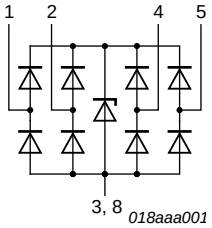
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- TVs, monitors
- DVD recorders and players
- Notebooks, mother boards, graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 **XSON10**	
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3F4-TBR	XSON10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 × 2.5 × 0.5 mm	SOT1176-1

4. Marking

Table 3. Marking codes

Type number	Marking code
PUSB3F4-TBR	F4

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			−0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4	[1]			
		contact discharge		-	±8	kV
		air discharge		-	±15	kV
T_{amb}	ambient temperature			−40	+85	°C
T_{stg}	storage temperature			−55	+125	°C

[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C unless otherwise specified.

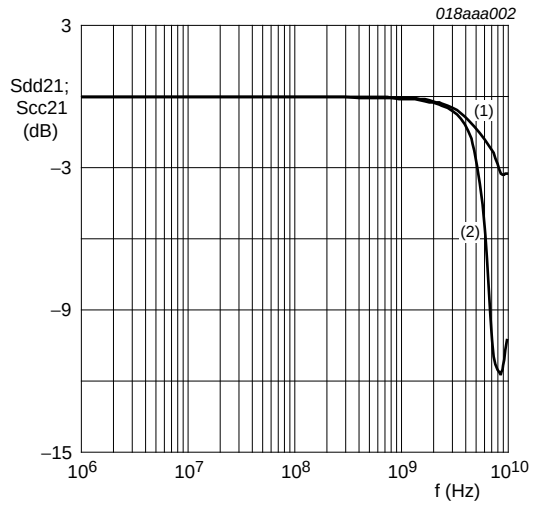
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BRzd}	Zener diode breakdown voltage	I_{test} = 1 mA		6	-	9	V
I_{LRzd}	Zener diode reverse leakage current	per TMDS channel; V_I = 3.0 V		-	-	1	μA
V_F	forward voltage			-	0.7	-	V
$C_{ch(TMDS)}$	TMDS channel capacitance	f = 1 MHz; V_{bias} = 2.5 V	[1]	0.4	0.5	0.7	pF
$\Delta C_{ch(TMDS)}$	TMDS channel capacitance difference	f = 1 MHz; V_{bias} = 2.5 V	[1]	-	0.05	-	pF
$C_{ch(mutual)}$	mutual channel capacitance	f = 1 MHz; V_{bias} = 2.5 V	[1][2]	-	0.07	-	pF
R_{dyn}	dynamic resistance	I = 1 A	[3]				
		positive transient		-	1	-	Ω
		negative transient		-	1	-	Ω
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	V_{ESD} = 8 kV	[4]	-	8	-	V

[1] This parameter is guaranteed by design.

[2] Between signal pin and pin n.c.

[3] According to IEC 61000-4-5 and IEC 61000-4-9.

[4] Human Body Model (HBM) according to JESD22-A-J114D.

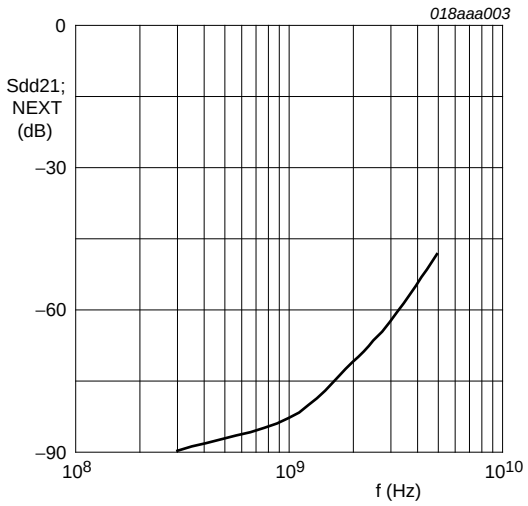


(1) Sdd21

(2) Scc21

Normalized to 100 Ω;
differential pairs at CH1/CH2 or at CH3/CH4

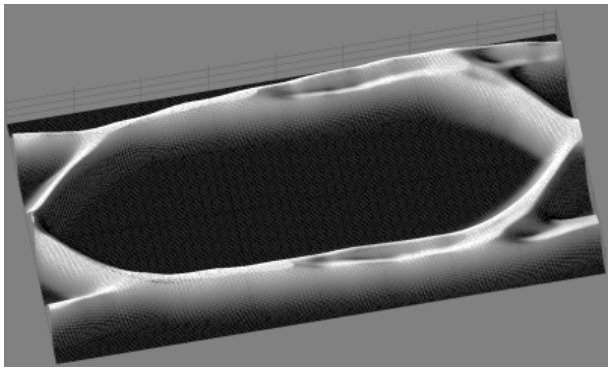
Fig 1. Mixed-mode differential and common-mode insertion loss; typical values



Sdd21

Normalized to 100 Ω;
differential pairs CH1/CH2 versus CH3/CH4

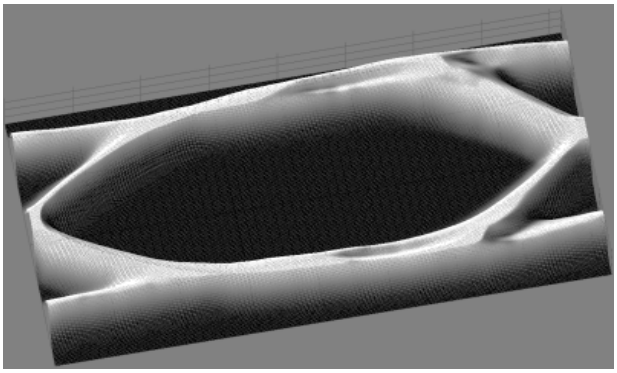
Fig 2. Mixed-mode differential NEXT crosstalk; typical values



018aaa004

5 Gbit/s; USB 3.0 CP0 pattern

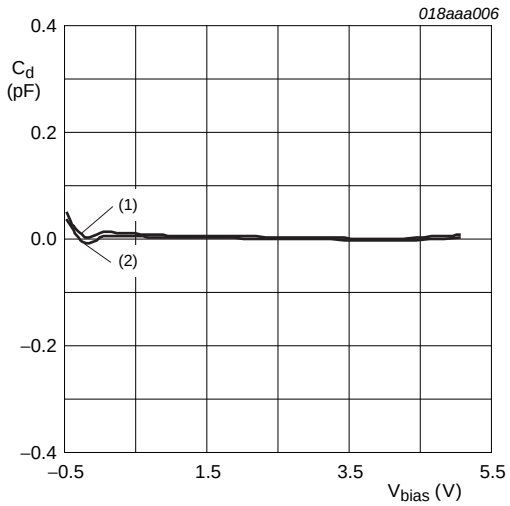
Fig 3. Eye diagram using reference PCB



018aaa005

5 Gbit/s; USB 3.0 CP0 pattern

Fig 4. Typical eye diagram for PUSB3F4-TBR

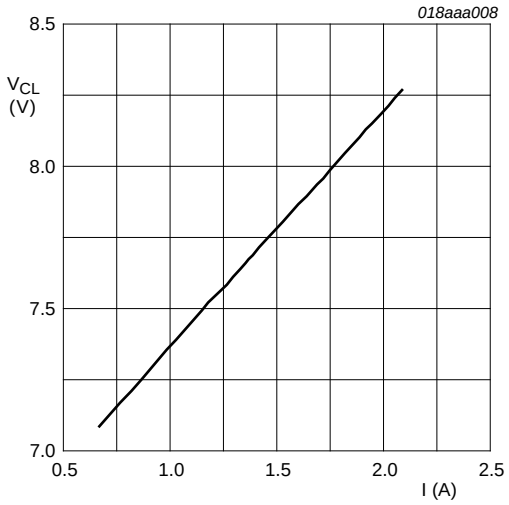


(1) Pin 2

(2) Pin 1

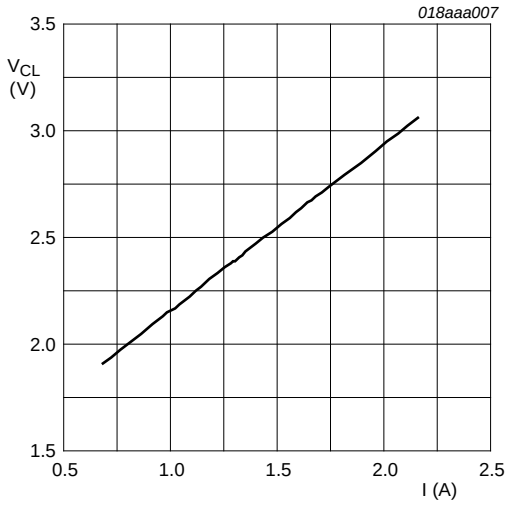
Deviation from typical capacitance normalized at V_{bias} = 2.5 V

Fig 5. Line capacitance as a function of bias voltage; typical values



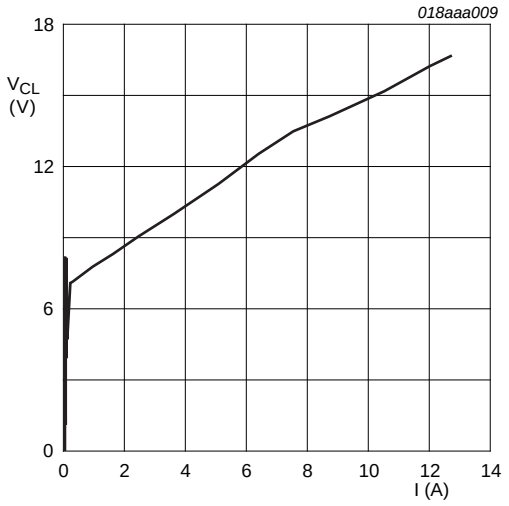
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 6. Dynamic resistance with positive clamping



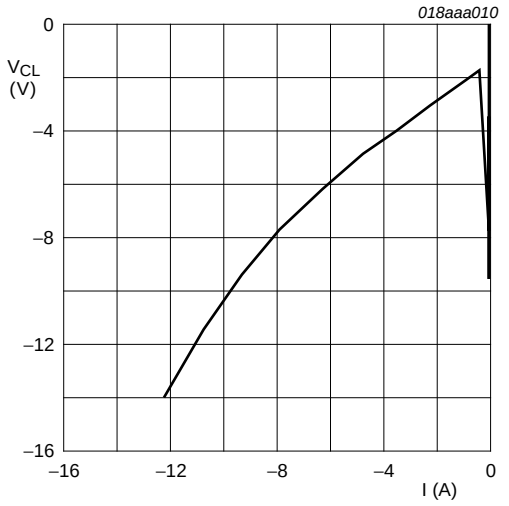
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 7. Dynamic resistance with negative clamping



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 8. Dynamic resistance with positive clamping



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 9. Dynamic resistance with negative clamping

7. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the Printed-Circuit Board (PCB), give careful consideration to basic high-speed routing guidelines, impedance matching, and signal coupling.

Basic application diagram for the ESD protection of an HDMI interface is shown in Figure 10.

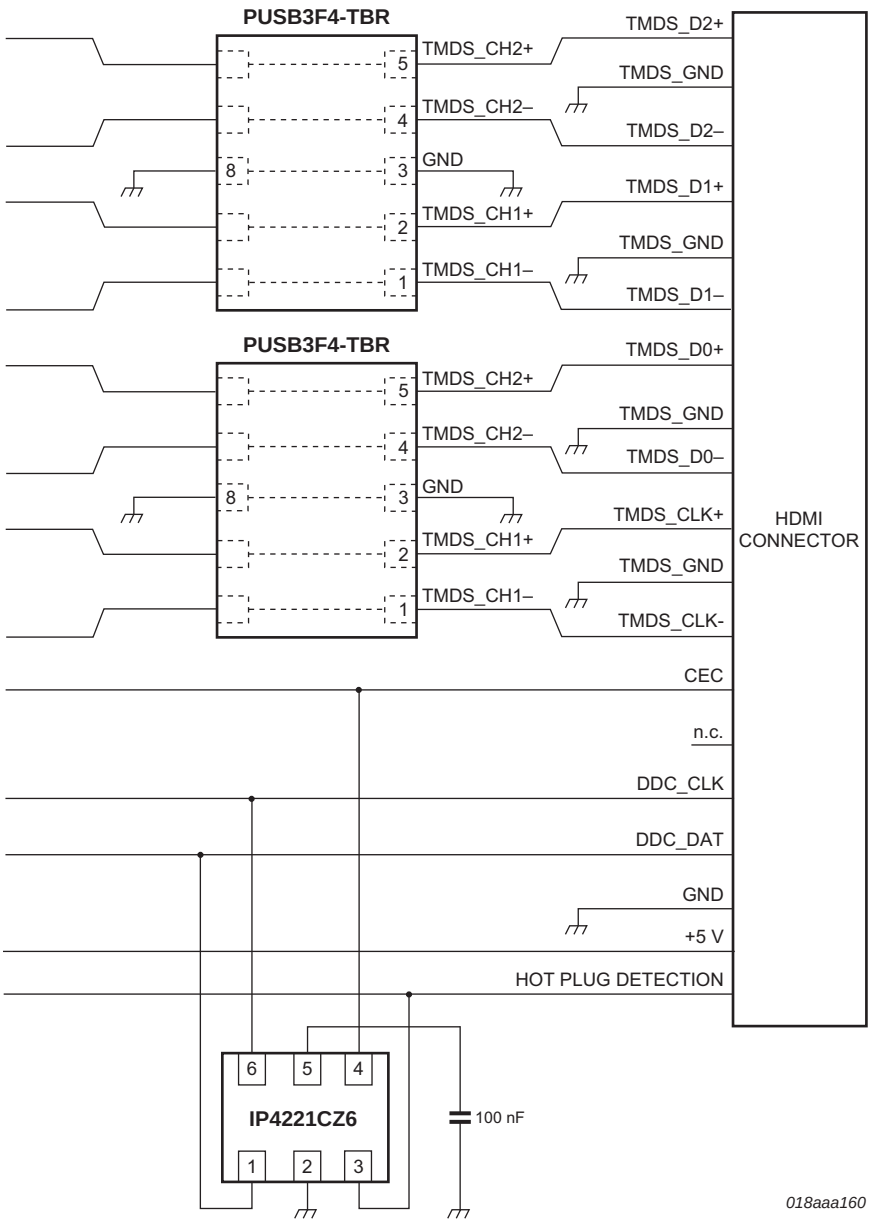
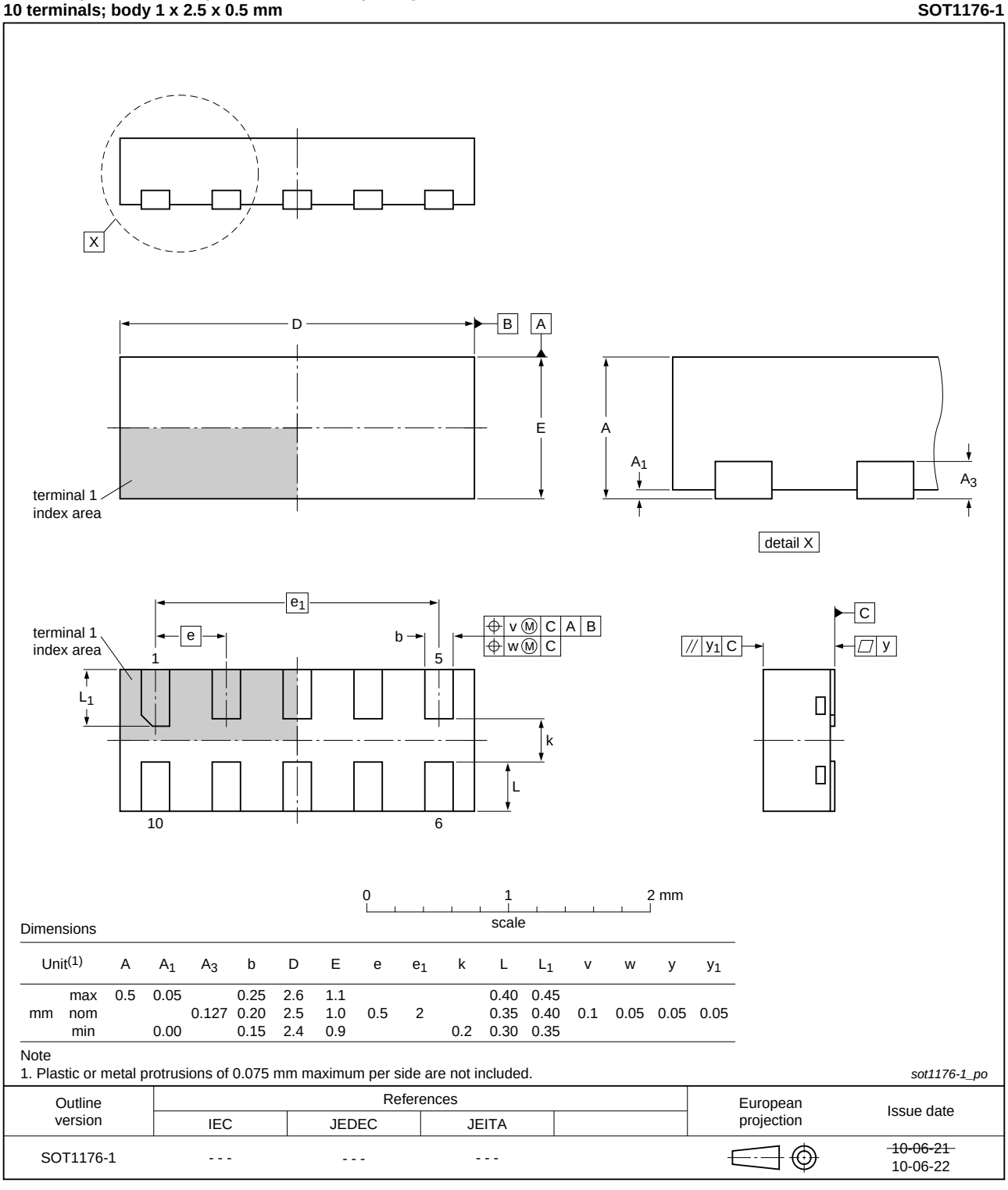


Fig 10. Application diagram of HDMI ESD protection using PUSB3F4-TBR

8. Package outline

XSON10: plastic extremely thin small outline package; no leads; 10 terminals; body 1 x 2.5 x 0.5 mm **SOT1176-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	k	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	2.6	1.1				0.40	0.45				
mm	nom			0.127	0.20	2.5	1.0	0.5	2		0.35	0.40	0.1	0.05	0.05	0.05
	min		0.00		0.15	2.4	0.9			0.2	0.30	0.35				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

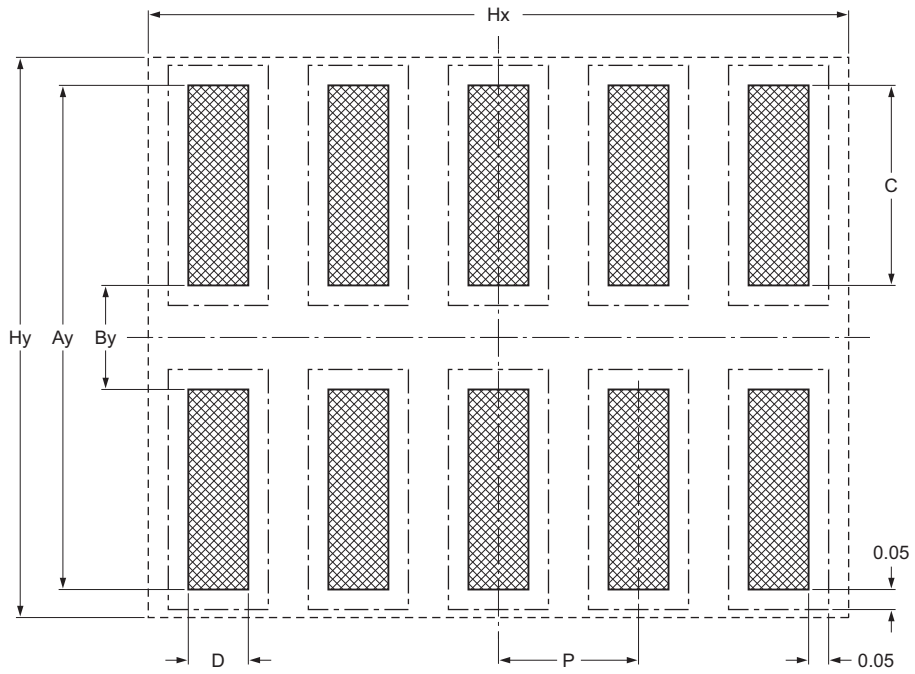
sot1176-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1176-1	- - -	- - -	- - -			~~10-06-21~~ 10-06-22

Fig 11. Package outline SOT1176-1 (XSON10)

9. Soldering

Footprint information for reflow soldering of XSON10 package **SOT1176-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

solder resist

Dimensions in mm

P	Ay	By	C	D	Hx	Hy
0.5	1.25	0.3	0.475	0.2	2.45	1.5

Remark:
Stencil of 75 µm is recommended.
A stencil of 75 µm gives an aspect ratio of 0.77
With a stencil of 100 µm one will obtain an aspect ratio of 0.58

sot1176-1_fr

Reflow soldering is the only recommended soldering method.

Fig 12. Reflow soldering footprint SOT1176-1 (XSON10)

10. Abbreviations

Table 6. Abbreviations

Acronym	Description
eSATA	external Serial Advanced Technology Attachment
ESD	ElectroStatic Discharge
HBM	Human Body Model
HDMI	High-Definition Multimedia Interface
LVDS	Low Voltage Differential Signaling
NEXT	Near End Crosstalk
RoHS	Restriction of Hazardous Substances
TLP	Transmission Line Pulse
TMDS	Transition Minimized Differential Signaling

11. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3F4-TBR v.1	20111006	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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