RL78/L13

RENESAS MCU

R01DS0168EJ0002
Rev.0.02
2012.10.31

Integrated LCD controller/driver, True Low Power Platform (as low as 112.5 μA/MHz, and 0.61 μA for RTC + LVD), 1.6 V to 5.5 V operation, 16 to 128 Kbyte Flash, 31 DMIPS at 24 MHz, for All LCD Based Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 1.6 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.25 μA, (LVD enabled): 0.33 μA
- Halt (RTC + LVD): 0.61 μA
- Supports snooze
- Operating: 112.5 μA/MHz
- LCD operating current (Capacitor split method): 0.29 μA
- LCD operating current (Internal voltage boost method): 0.68 μA

16-bit RL78 CPU Core
- Delivers 31 DMIPS at maximum operating frequency of 24 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory
- Density: 16 KB to 128 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory
- Data Flash with background operation
- Data flash size: 4 KB
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM
- 1 KB to 8 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 24 MHz with +/− 1% accuracy over voltage (1.8 V to 5.5 V) and temperature (−20 °C to +85 °C)
- Pre-configured settings: 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz & 1 MHz (TYP.)

<R>

Reset and Supply Management
- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 14 setting options (Interrupt and/or reset function)

LCD Controller/Driver

<R>
- Up to 51 seg x 4 com or 48 seg x 8 com
- Supports capacitor split method, internal voltage boost method and resistance division method
- Supports waveform types A and B
- Supports LCD contrast adjustment (18 steps)
- Supports LCD blinking

Data Memory Access (DMA) Controller
- Up to 4 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces
- Up to 2 x I^2C master
- Up to 1 x I^2C multi-master
- Up to 2 x CSI (7-, 8-bit)
- Up to 4 x UART (7-, 8-, 9-bit)
- Up to 1 x LIN

Extended-Function Timers
- Multi-function 16-bit timer TAU: Up to 8 channels (remote control output available)
- Multi-function 16-bit timer KB20: 1 channel
- High accuracy real-time clock (RTC005): 1 channel (full calendar and alarm function with watch correction function)
- 12-bit interval timer: 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog
- ADC: Up to 12 channels, 8/10-bit resolution, 2.1 μs minimum conversion time
- Supports 1.6 V
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/ frequency detection
- ADC self-test
- I/O port read back function (echo)

General Purpose I/O
- 5 V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature
- Consumer application: −40°C to + 85°C
- Industrial application: −40°C to + 105°C

Package Type and Pin Count
- 64-pin plastic LQFP (fine pitch) (10 x 10)
- 64-pin plastic LQFP (12 x 12)
- 80-pin plastic LQFP (fine pitch) (12 x 12)
- 80-pin plastic LQFP (14 x 14)

○ ROM, RAM capacities

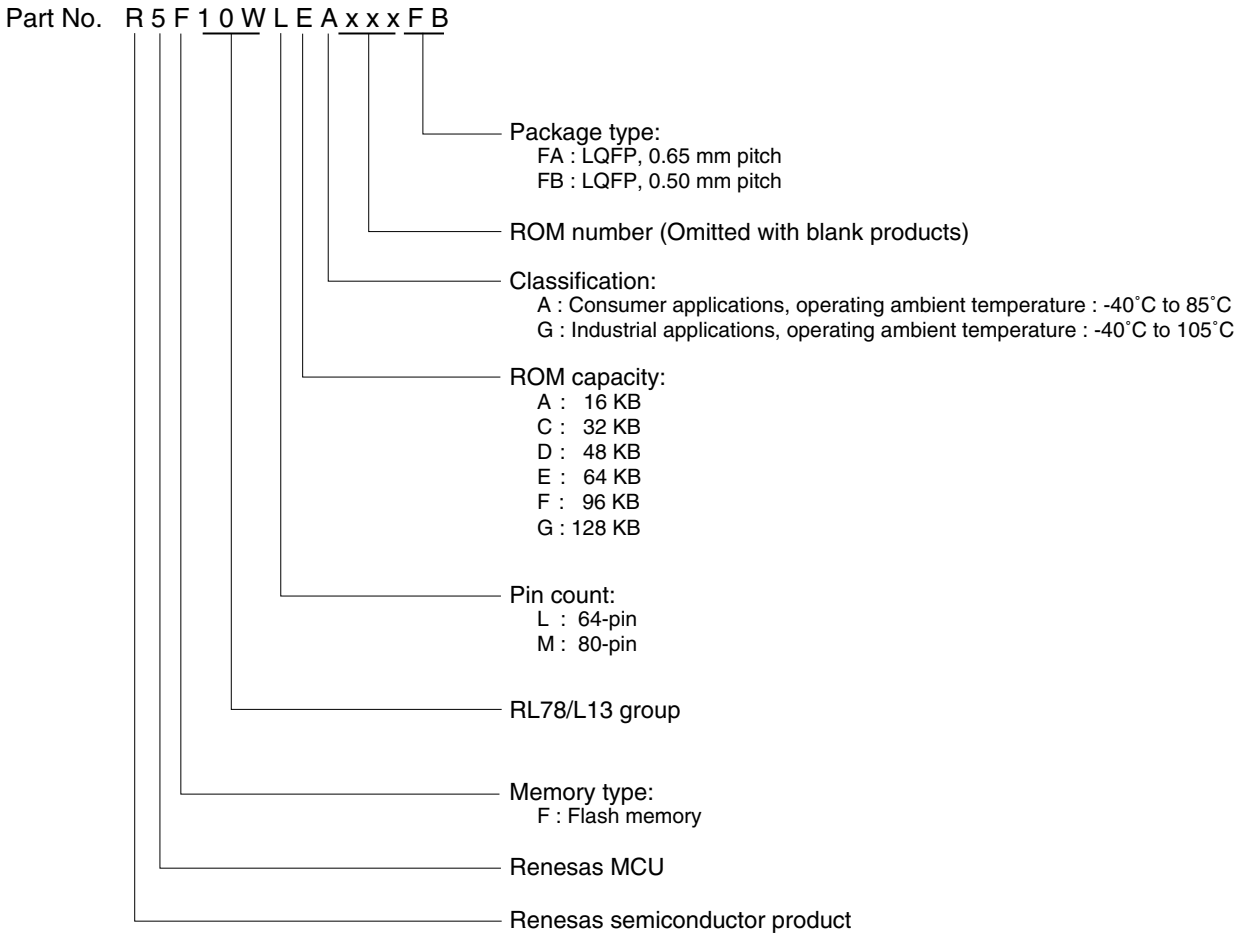
Flash ROM	Data flash	RAM	RL78/L13	
			64 pins	80 pins
128 KB	4 KB	8 KB Note	R5F10WLG	R5F10WMG
96 KB	4 KB	6 KB	R5F10WLF	R5F10WMF
64 KB	4 KB	4 KB	R5F10WLE	R5F10WME
48 KB	4 KB	2 KB	R5F10WLD	R5F10WMD
32 KB	4 KB	1.5 KB	R5F10WLC	R5F10WMC
16 KB	4 KB	1 KB	R5F10WLA	R5F10WMA

Note This is about 7 KB when the self-programming function and data flash function are used.

<R> 1.2 Ordering Information

Pin count	Package	Data flash	Part Number
64 pins	64-pin plastic LQFP (12 × 12)	Mounted	R5F10WLAAFA, R5F10WLCAFA, R5F10WLDAFA, R5F10WLEAFA, R5F10WLFAFA, R5F10WLGAFA, R5F10WLAGFA, R5F10WLCGFA, R5F10WLDGFA, R5F10WLEGFA, R5F10WLFGFA, R5F10WLGGFA
	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F10WLAAFB, R5F10WLCAFB, R5F10WLDAFB, R5F10WLEAFB, R5F10WLFAFB, R5F10WLGAFB, R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB, R5F10WLEGFB, R5F10WLFGFB, R5F10WLGGFB
80 pins	80-pin plastic LQFP (14 × 14)	Mounted	R5F10WMAAFA, R5F10WMCAFA, R5F10WMDAFA, R5F10WMEAFA, R5F10WMFAFA, R5F10WMGAFA, R5F10WMAGFA, R5F10WMCGFA, R5F10WMDGFA, R5F10WMEGFA, R5F10WMFGFA, R5F10WMGGFA
	80-pin plastic LQFP (fine pitch) (12 × 12)	Mounted	R5F10WMAAFB, R5F10WMCAFB, R5F10WMDAFB, R5F10WMEAFB, R5F10WMFAFB, R5F10WMGAFB, R5F10WMAGFB, R5F10WMCGFB, R5F10WMDGFB, R5F10WMEGFB, R5F10WMFGFB, R5F10WMGGFB

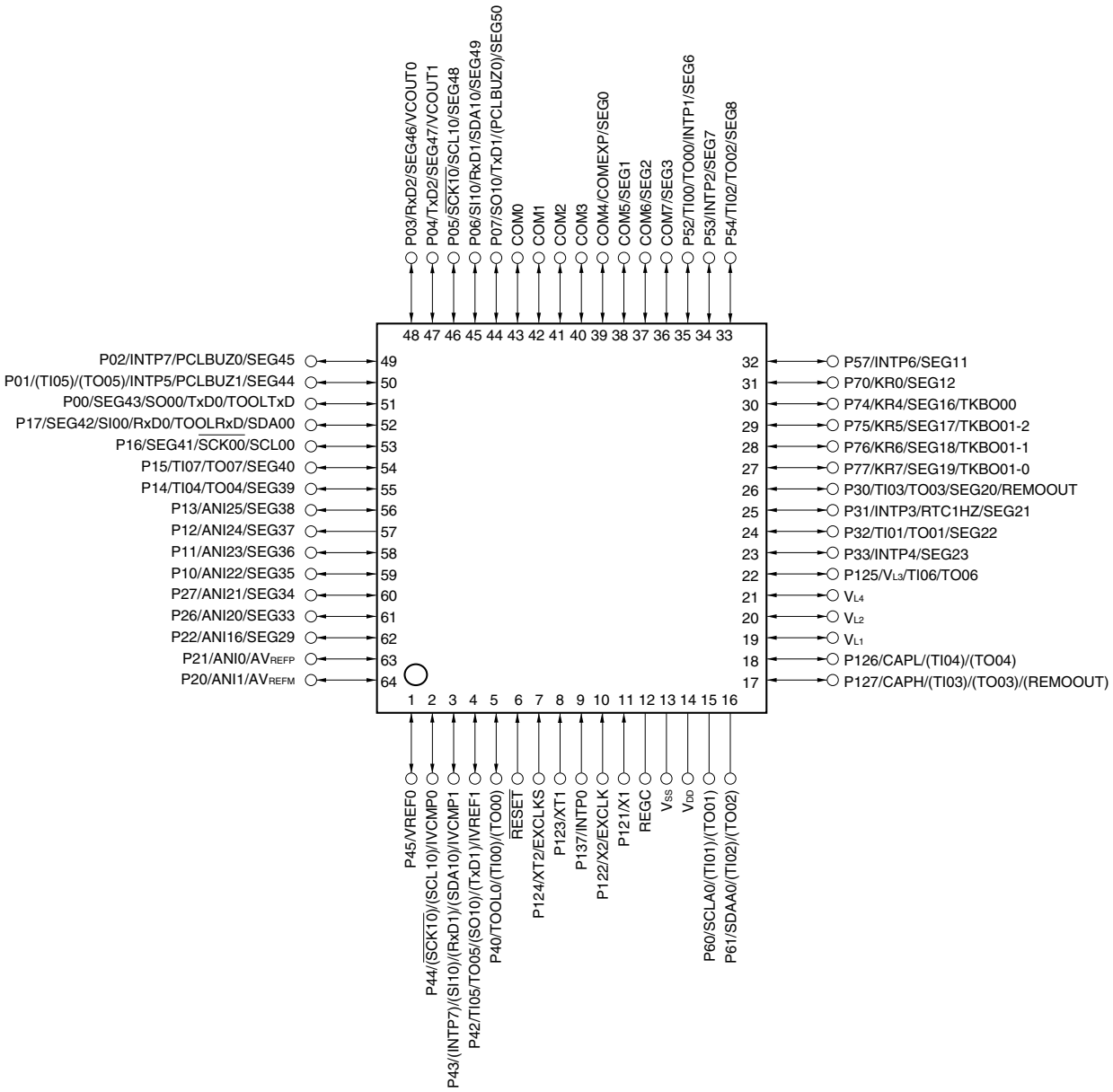
Figure 1-1. Part Number, Memory Size, and Package of RL78/L13



1.3 Pin Configuration (Top View)

1.3.1 64-pin products

- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)



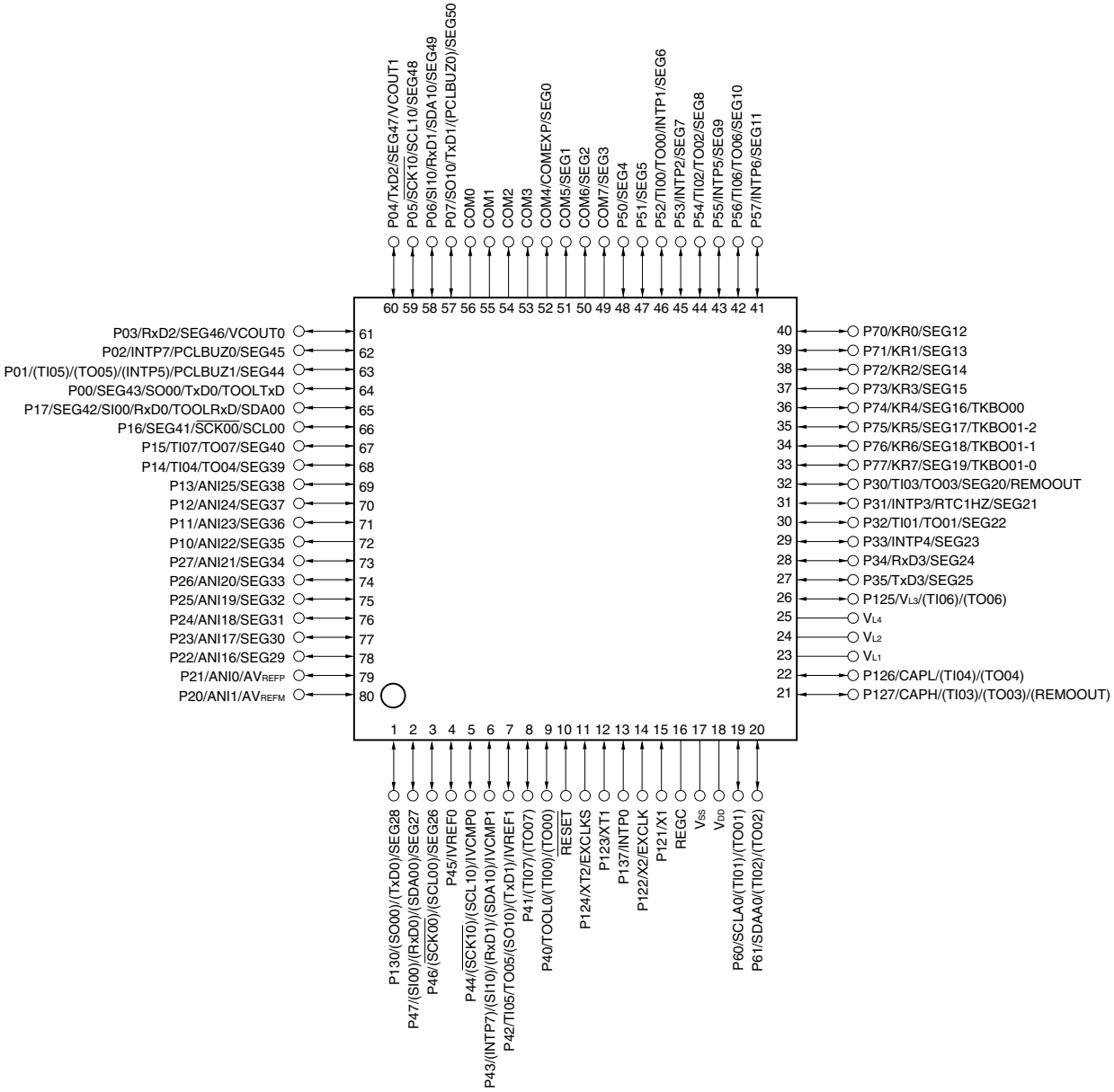
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 80-pin products

- 80-pin plastic LQFP (14 × 14)
- 80-pin plastic LQFP (fine pitch) (12 × 12)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

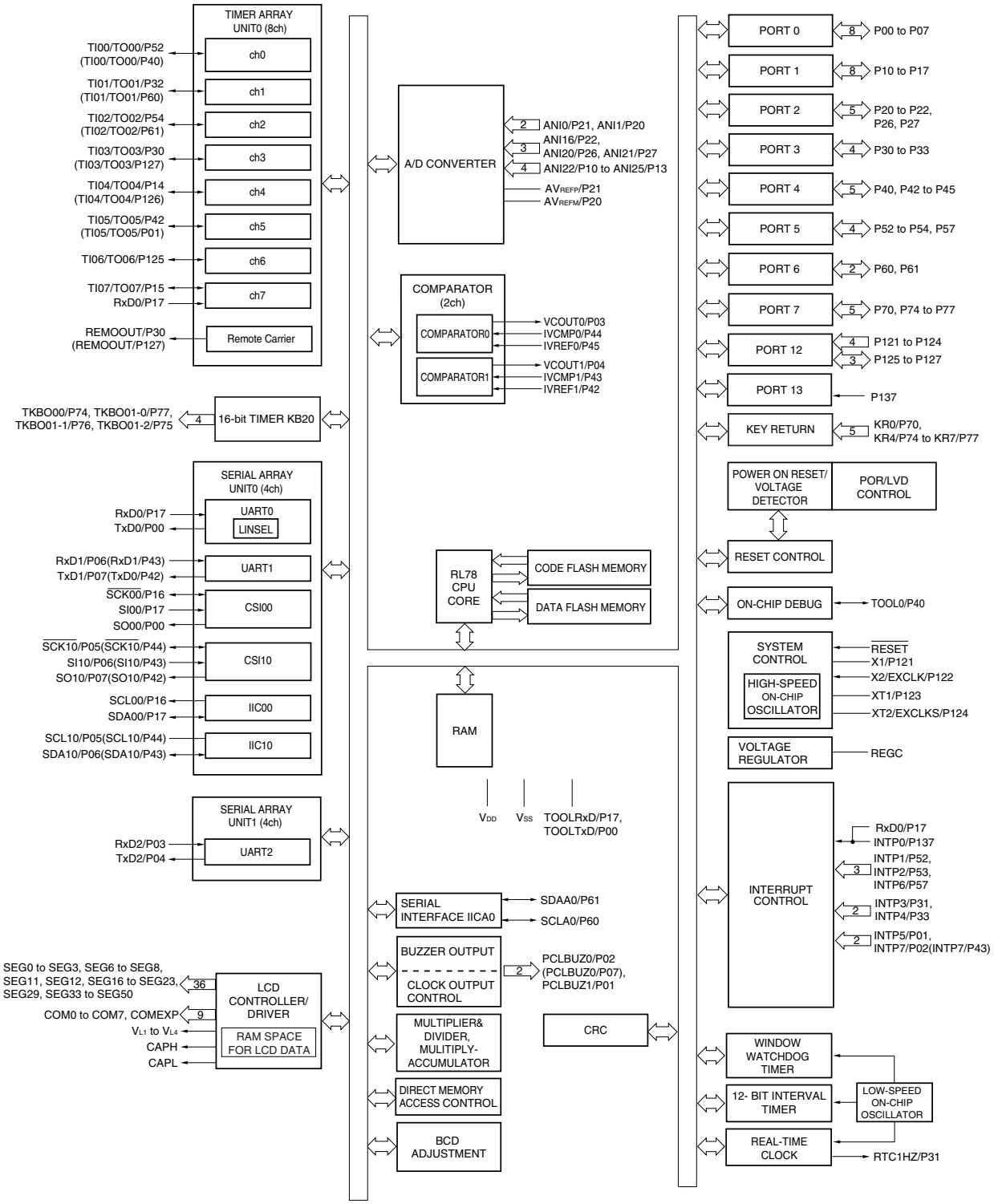
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

ANI0, ANI1,	:Analog Input	PCLBUZ0, PCLBUZ1	:Programmable Clock Output/
ANI16 to ANI25			Buzzer Output
AV_{REFM}	:Analog Reference Voltage	REGC	:Regulator Capacitance
	Minus	REMOOUT	:Remote control Output
AV_{REFP}	:Analog Reference Voltage	$\overline{RESET}$	:Reset
	Plus	RTC1HZ	:Real-time Clock Correction Clock
CAPH, CAPL	:Capacitor for LCD		(1 Hz) Output
COM0 to COM7,	:LCD Common Output	RxD0 to RxD3	:Receive Data
COMEXP		$\overline{SCK00}$, $\overline{SCK10}$	:Serial Clock Input/Output
EXCLK	:External Clock Input	SCLA0, SCL00, SCL10,	:Serial Clock Output
	(Main System Clock)	SDAA0, SDA00, SDA10,	:Serial Data Input/Output
EXCLKS	:External Clock Input	SEG0 to SEG50	:LCD Segment Output
	(Subsystem Clock)	SI00, SI10	:Serial Data Input
IVCMP0, IVCMP1	:Comparator Input	SO00, SO10	:Serial Data Output
IVREF0, IVREF1	:Comparator Reference Input	TI00 to TI07	:Timer Input
KR0 to KR7	:Key Return	TO00 to TO07,	:Timer Output
P00 to P07	:Port 0	TKBO00, TKBO01-0,	
P10 to P17	:Port 1	TKBO01-1, TKBO01-1,	
P20 to P27	:Port 2	TKBO01-2	
P30 to P35	:Port 3	TOOL0	:Data Input/Output for Tool
P40 to P47	:Port 4	TOOLRxD, TOOLTxD	:Data Input/Output for External Device
P50 to P57	:Port 5	TxD0 to TxD3	:Transmit Data
P60, P61	:Port 6	VCOUT0, VCOUT1	:Comparator Output
P70 to P77	:Port 7	V_{DD}	:Power Supply
P121 to P127	:Port 12	V_{L1} to V_{L4}	:LCD Power Supply
P130, P137	:Port 13	V_{SS}	:Ground
		X1, X2	:Crystal Oscillator (Main System Clock)
		XT1, XT2	:Crystal Oscillator (Subsystem Clock)

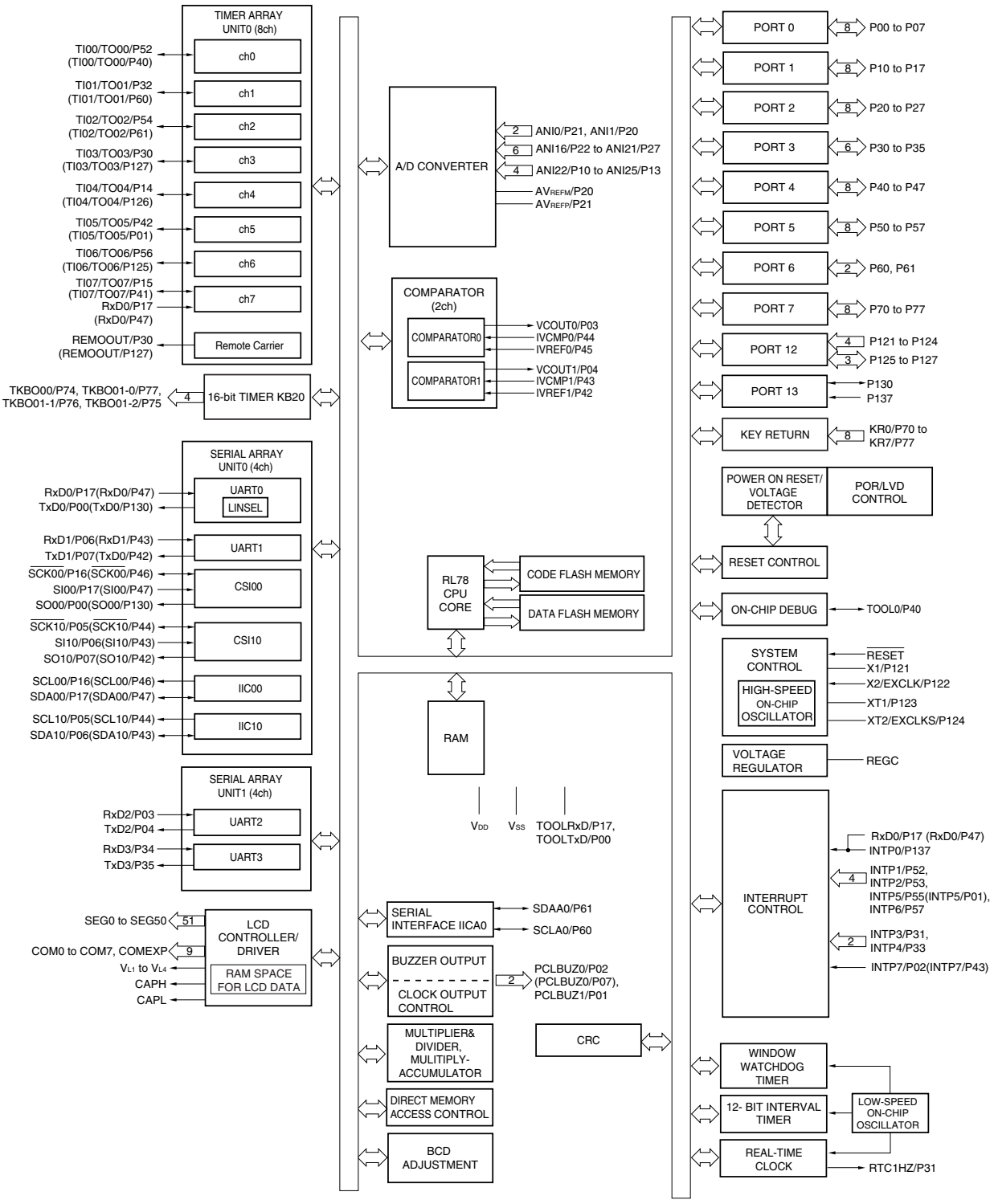
1.5 Block Diagram

1.5.1 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.2 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

(1/2)

Item		64-pin	80-pin
		R5F10WLx	R5F10WMx
Code flash memory (KB)		16 to 128	16 to 128
Data flash memory (KB)		4	4
RAM (KB)		1 to 8 Note 1	1 to 8 Note 1
Memory space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V	
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
Clock for 16-bit timer KB20		48 MHz (TYP.): V_{DD} = 2.7 to 5.5 V	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V_{DD} = 1.6 to 5.5 V	
Low-speed on-chip oscillator		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator: f_{IH} = 24 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	49	65
	CMOS I/O	42	58
	CMOS input	5	5
	CMOS output	–	–
	N-ch O.D I/O (6 V tolerance)	2	2
Timer	16-bit timer TAU	8 channels (with 1 channel remote control output function) (timer outputs 8, PWM outputs: 7 Note 2)	
	16-bit timer KB20	1 channel (PWM outputs: 2)	
	Watchdog timer	1 channel	
	12-bit interval timer (IT)	1 channel	
	High accuracy real-time clock (RTC005)	1 channel	
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz or)	

Notes1. In the case of the 8 KB, this is about 7 KB when the self-programming function and data flash function are used.

2. The number of outputs varies, depending on the setting of channels in use and the number of the master.

(2/2)

Item			64-pin	80-pin
			R5F10WLx	R5F10WMx
Clock output/buzzer output			2	
			• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter			9 channels	12 channels
Comparator			2 channels	
Serial interface			[64-pin] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART: 1 channel [80-pin] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART: 2 channels	
	I^2C bus		1 channel	
LCD controller/driver			Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
<R>	Segment signal output		36 (32) Note 1	51 (47) Note 1
	Common signal output		4 (8) Note 1	
Multiplier and divider/multiply-accumulator			• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)	
DMA controller			4 channels	
Vectored interrupt sources	Internal		32	35
	External		11	11
Key interrupt			8	8
Reset			• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit			• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V	
Voltage detector			• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)	
On-chip debug function			Provided	
Power supply voltage			V_{DD} = 1.6 to 5.5 V	
<R> Operating ambient temperature			Consumer application: T_A = –40 to +85 °C Industrial application: T_A =–40°C to + 105°C	

Notes 1. The values in parentheses are the number of signal outputs when 8 com is used.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Rev.	Date	Description	
		Page	Summary
0.01	Apr 13, 2012	-	First Edition issued
0.02	Oct 31, 2012	-	Change of the number of segment pins ● 64-pin products: 36 pins ● 80-pin products: 51 pins

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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