Data Sheet | July 1999 | File Number 3575.4

50A, 60V, 0.022 Ohm, N-Channel Power MOSFETs

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49018.

Ordering Information

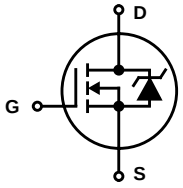
PART NUMBER	PACKAGE	BRAND
RFG50N06	TO-247	RFG50N06
RFP50N06	TO-220AB	RFP50N06
RF1S50N06SM	TO-263AB	F1S50N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S50N06SM9A.

Features

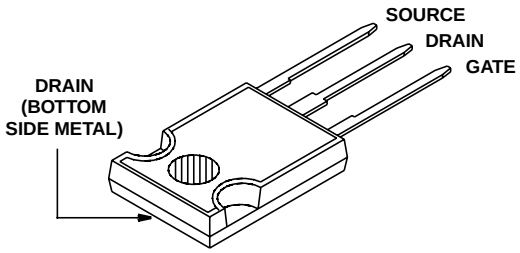
- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175^{o}C Operating Temperature

Symbol

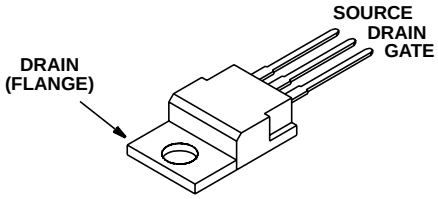


Packaging

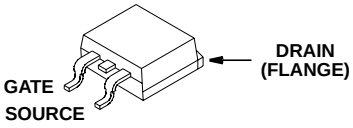
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFG50N06, RFP50N06 RF1S50N06SM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±20	V
Continuous Drain Current (Figure 2)	I_D	50	A
Pulsed Drain Current	I_{DM}	(Figure 5)	
Pulsed Avalanche Rating	E_{AS}	(Figure 6, 14, 15)	
Power Dissipation	P_D	131	W
Linear Derating Factor		0.877	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, see Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		60	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	$T_C = 25^oC$	-	-	1	μA
			$T_C = 150^oC$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 50A, V_{GS} = 10V (Figures 9)		-	-	0.022	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 50A R_L = 0.6Ω, V_{GS} = 10V R_{GS} = 3.6Ω (Figure 13)		-	-	95	ns
Turn-On Delay Time	$t_{d(ON)}$			-	12	-	ns
Rise Time	t_r			-	55	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	37	-	ns
Fall Time	t_f			-	13	-	ns
Turn-Off Time	t_{OFF}			-	-	75	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 48V, I_D = 50A, R_L = 0.96Ω $I_{g(REF)}$ = 1.45mA (Figure 13)	-	125	150	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0 to 10V		-	67	80	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to 2V		-	3.7	4.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V f = 1MHz (Figure 12)		-	2020	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	1.14	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^oC/W$
		TO-220, TO-263		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 50A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 50A, dI_{SD}/dt = 100A/μs	-	-	125	ns