

Distributed by:



www.Jameco.com ♦ 1-800-831-4242

The content and copyrights of the attached
material are the property of its owner.

Jameco Part Number 1071417

50A, 60V, 0.022 Ohm, N-Channel Power MOSFETs

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49018.

Ordering Information

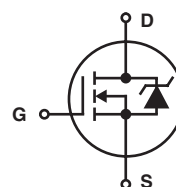
PART NUMBER	PACKAGE	BRAND
RFG50N06	TO-247	RFG50N06
RFP50N06	TO-220AB	RFP50N06
RF1S50N06SM	TO-263AB	F1S50N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S50N06SM9A.

Features

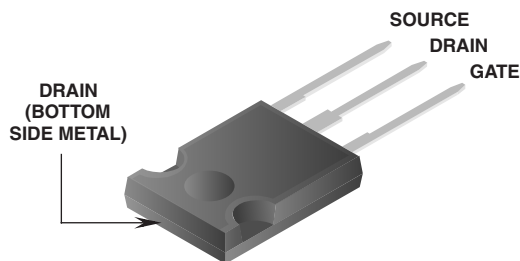
- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

Symbol

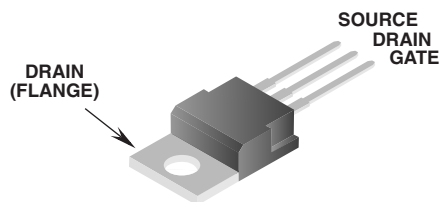


Packaging

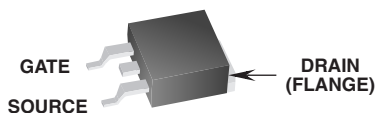
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



RFG50N06, RFP50N06, RF1S50N06SM

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	RFG50N06, RFP50N06 RF1S50N06SM	UNITS
Drain to Source Voltage (Note 1)	V_{DS} 60	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR} 60	V
Gate to Source Voltage	V_{GS} ± 20	V
Continuous Drain Current (Figure 2)	I_D 50	A
Pulsed Drain Current	I_{DM} (Figure 5)	
Pulsed Avalanche Rating	E_{AS} (Figure 6)	
Power Dissipation	P_D 131	W
Linear Derating Factor	0.877	$\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^{\circ}\text{C}$
Package Body for 10s, see Techbrief 334	T_{pkg} 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)		60	-	-	V
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V	T _C = 25°C	-	-	1	μA
			T _C = 150°C	-	-	50	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	r _{DS(ON)}	I _D = 50A, V _{GS} = 10V (Figures 9)		-	-	0.022	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 50A R _L = 0.6Ω, V _{GS} = 10V R _{GS} = 3.6Ω (Figure 13)		-	-	95	ns
Turn-On Delay Time	t _{d(ON)}			-	12	-	ns
Rise Time	t _r			-	55	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	37	-	ns
Fall Time	t _f			-	13	-	ns
Turn-Off Time	t _{OFF}			-	-	75	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0 to 20V	V _{DD} = 48V, I _D = 50A, R _L = 0.96Ω I _{g(REF)} = 1.45mA (Figure 13)	-	125	150	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0 to 10V		-	67	80	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0 to 2V		-	3.7	4.5	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V f = 1MHz (Figure 12)		-	2020	-	pF
Output Capacitance	C _{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	200	-	pF
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)		-	-	1.14	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-247		-	-	30	°C/W
		TO-220, TO-263		-	-	62	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 50\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 50\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

Typical Performance Curves Unless Otherwise Specified

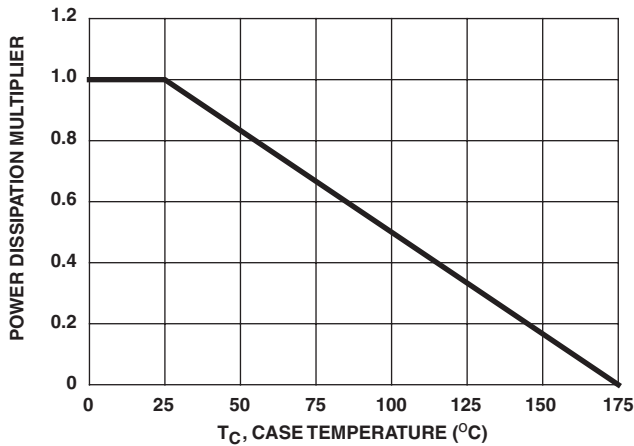


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

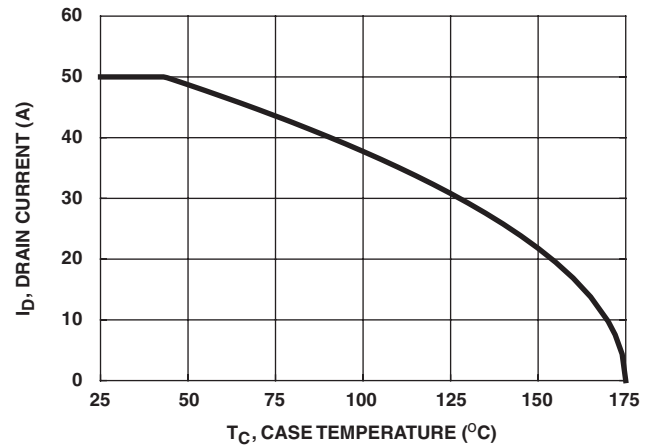


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

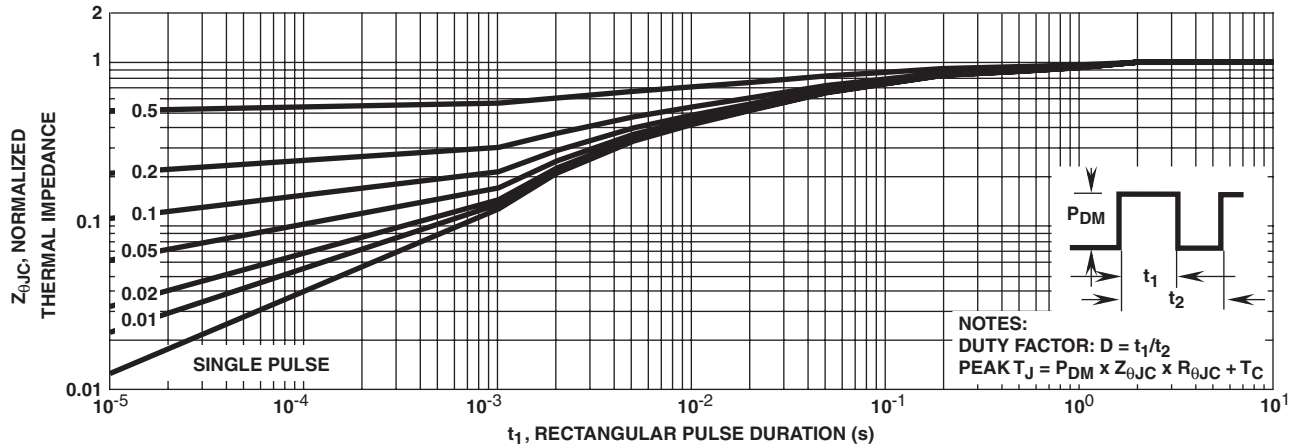


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

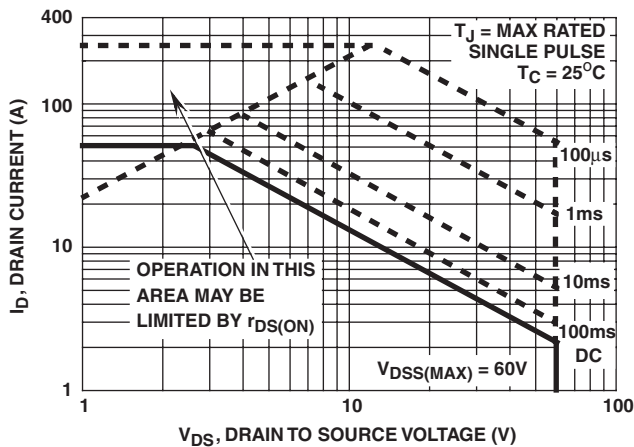


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

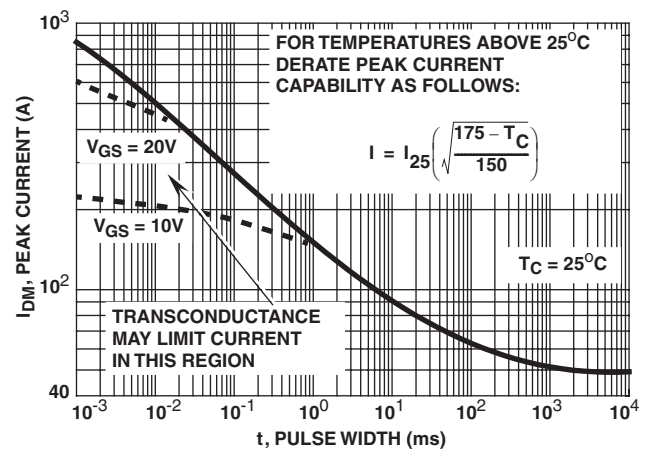
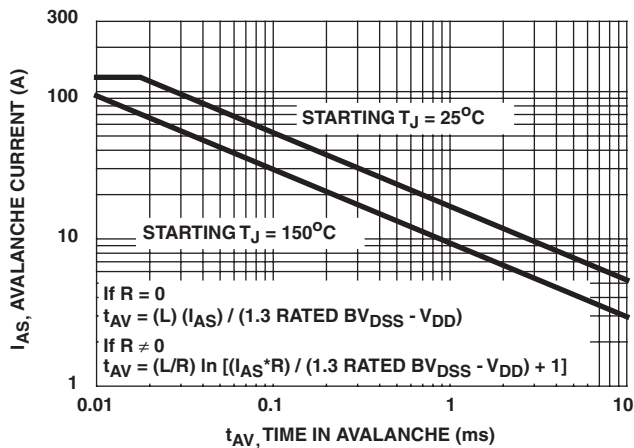


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Fairchild Application Notes 9321 and 9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

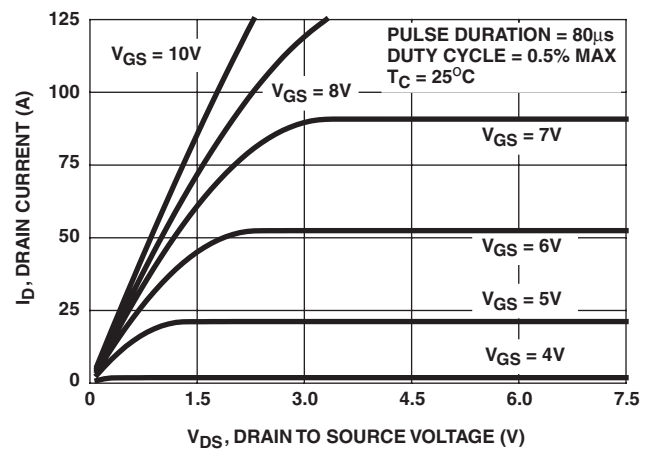


FIGURE 7. SATURATION CHARACTERISTICS

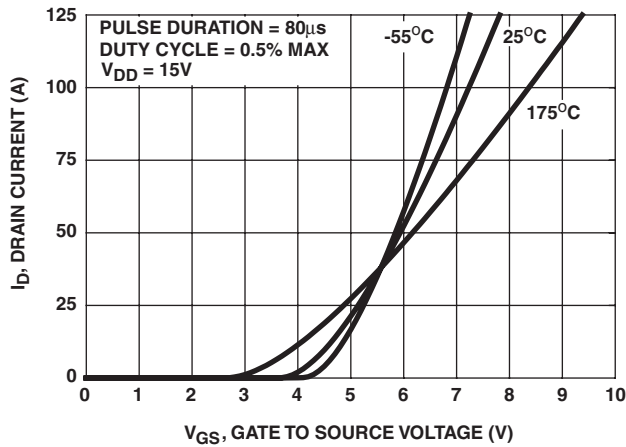


FIGURE 8. TRANSFER CHARACTERISTICS

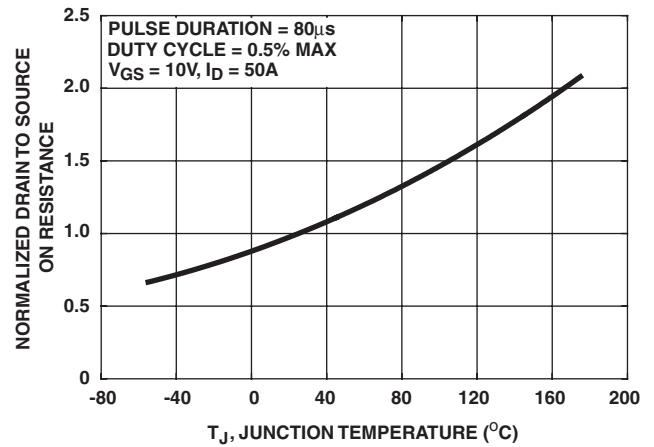


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

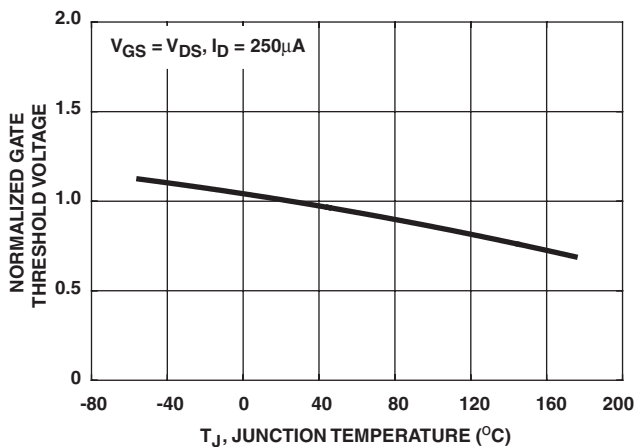


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

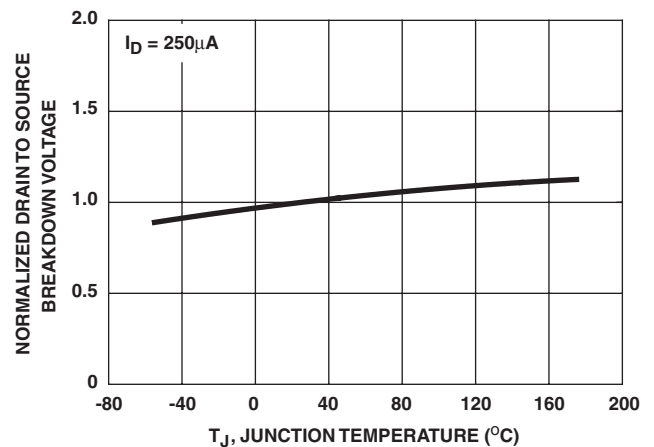


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

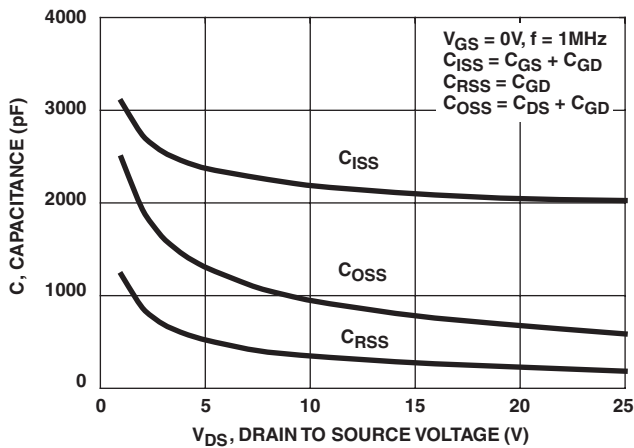
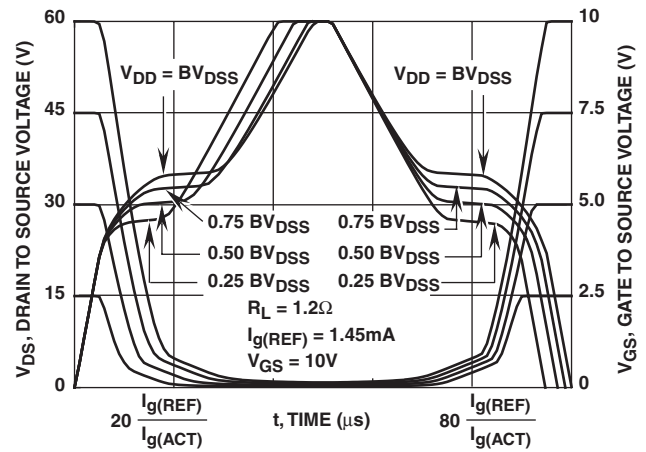


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

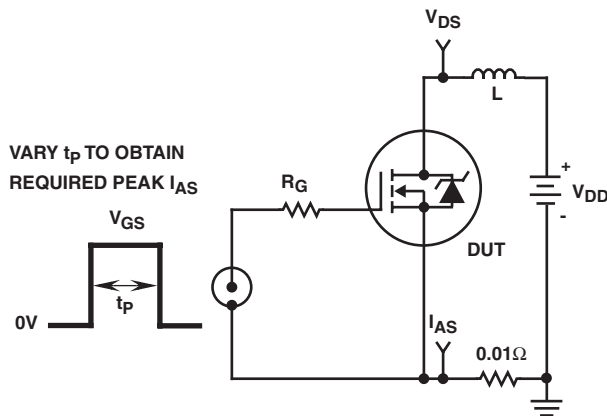


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

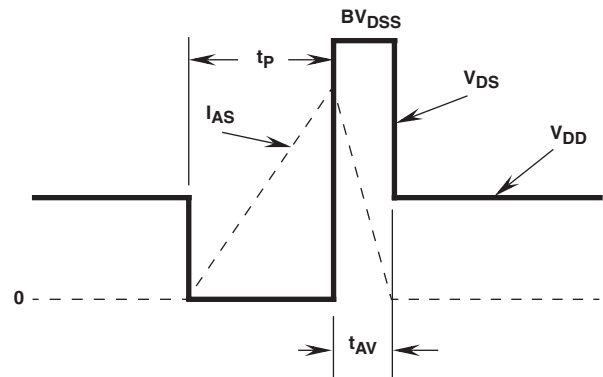


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

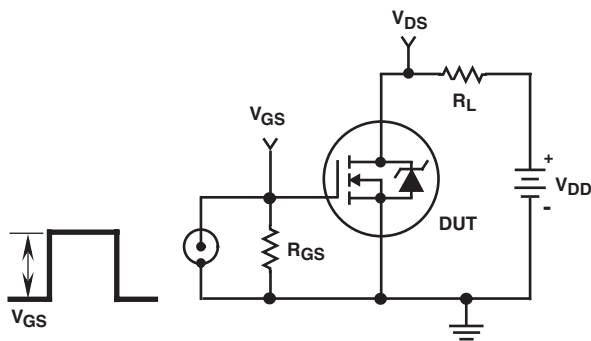


FIGURE 16. SWITCHING TIME TEST CIRCUIT

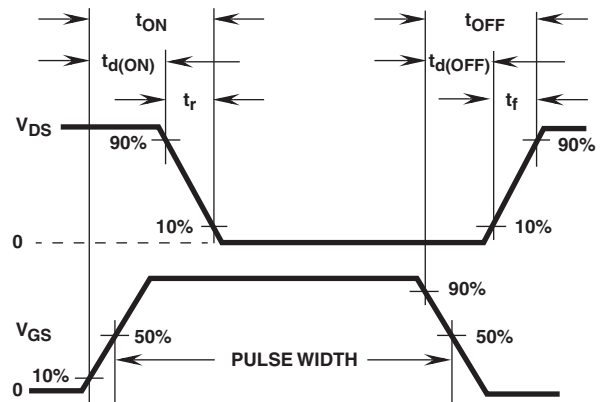


FIGURE 17. SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

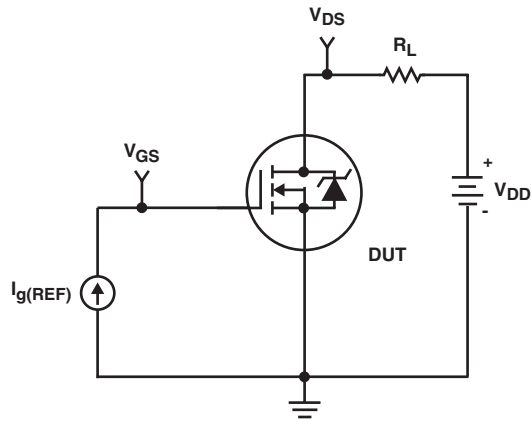


FIGURE 18. GATE CHARGE TEST CIRCUIT

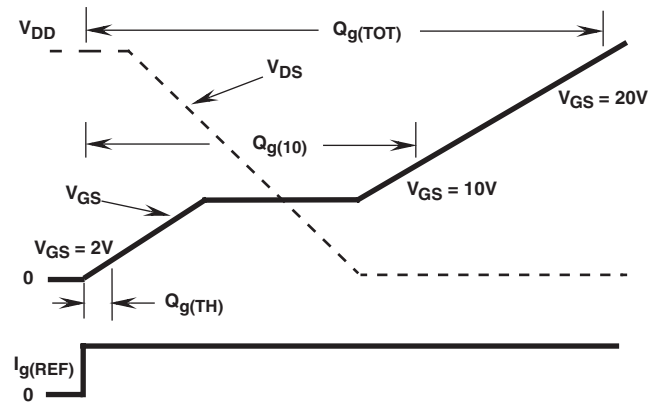


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

.SUBCKT RFP50N06 2 1 3

REV 2/22/93

*NOM TEMP = 25°C

CA 12 8 3.68e-9

CB 15 14 3.625e-9

CIN 6 8 1.98e-9

DBODY 7 5 DBDMOD

DBREAK 5 11 DBKMOD

DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.59

EDS 14 8 5 8 1

EGS 13 8 6 8 1

ESG 6 10 6 8 1

EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9

LGATE 1 9 5.65e-9

LSOURCE 3 7 4.13e-9

MOS1 16 6 8 8 MOSMOD M=0.99

MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1

RDRAIN 5 16 RDSMOD 1e-4

RGATE 9 20 0.690

RIN 6 8 1e9

RSOURCE 8 7 RDSMOD 12e-3

RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD

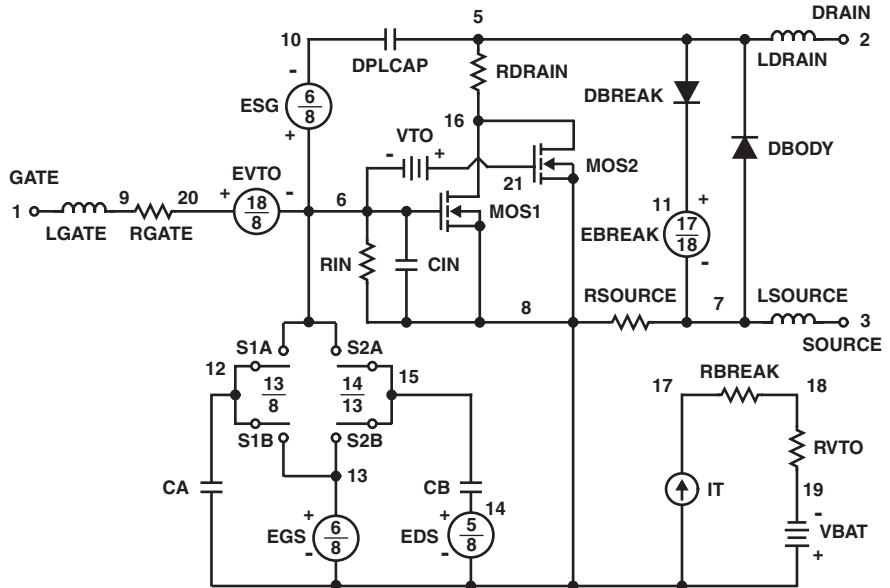
S1B 13 12 13 8 S1BMOD

S2A 6 15 14 13 S2AMOD

S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1

VTO 21 6 0.678



.MODEL DBDMOD D (IS=9.85e-13 RS=4.91e-3 TRS1=2.07e-3 TRS2=2.51e-7 CJO=2.05e-9 TT=4.33e-8)

.MODEL DBKMOD D (RS=1.98e-1 TRS1=2.35E-4 TRS2=-3.83e-6)

.MODEL DPLCAPMOD D (CJO=1.42e-9 IS=1e-30 N=10)

.MODEL MOSMOD NMOS (VTO=3.65 KP=35 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL RBKMOD RES (TC1=1.23e-3 TC2=-2.34e-7)

.MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.49e-5)

.MODEL RVTOMOD RES (TC1=-5.03e-3 TC2=-5.16e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.75 VOFF=-2.5)

.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.5 VOFF=-6.75)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.7 VOFF=2.3)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.3 VOFF=-2.7)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE ^{Ex} TM	FAST [®]	OPTOLOGIC TM	SMART START TM	VCX TM
Bottomless TM	FAST ^r TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.