RICOH RP155Z Series

200 mA LDO Regulator with Alternative Dual-Voltage Level Output

NO.EA-334-160126

OUTLINE

The RP155Z is a 200-mA LDO regulator with a selectable dual-voltage level output. It provides the VSEL pin that is used to select one of two preset output voltage levels.

Excellent ripple rejection, input transient response, and load transient response make the RP155Z ideal for the application for mobile communication equipment.

For protection, the RP155Z provides a short-current limiting circuit, a thermal shutdown circuit and an inrush current limiting circuit.

The RP155Z is offered in al 5-pin WLCSP-5-P1 package which achieves the smallest possible footprint solution on boards where area is limited.

FEATURES

- Input Voltage Range (Maximum Ratings) ····· 1.9 V to 5.25 V (6.0 V)
- Supply Current ····· Typ. 80 µA
- Standby Current ····· Typ. 0.1 µA
- Dropout Voltage ····· Typ. 0.085 V, I_{OUT} = 200 mA, V_{SET} = 2.5 V
- Ripple Rejection ····· Typ. 75 dB, f = 1 kHz,
  Typ. 70 dB, f = 10 kHz
- Output Voltage Accuracy ····· ±1.0%
- Output Voltage Temperature Coefficient ····· Typ. ±30 ppm/°C
- Output Voltage Range ····· 1.6 V to 3.6 V
- Line Regulation ····· Typ. 0.02%/V
- Short-current Limiting ····· Typ. 50 mA
- Overcurrent Protection ····· Fold-back Type
- Thermal Shutdown ····· Typ. 165°C
- Inrush Current Limiting ····· Typ. 160 mA during 180 µs after start-up
- Ceramic Capacitor Compatible ····· 1.0 µF or more
- Package ····· WLCSP-5-P1, 1.346 mm x 0.98 mm

APPLICATIONS

- Printers and PCs with SD Card Slots
- Battery-powered Equipment: Portable Music Players, IC Recorders, Cameras and Camcorders
- Portable Communication Equipment: Smartphones, Feature Phones
- Electronic Equipment System that Requires Two Levels of Output Voltage Regulation in Normal Mode/ Power-Saving Mode

SELECTION GUIDE

The set output voltage, the package type and the auto discharge function(1) are user-selectable options.

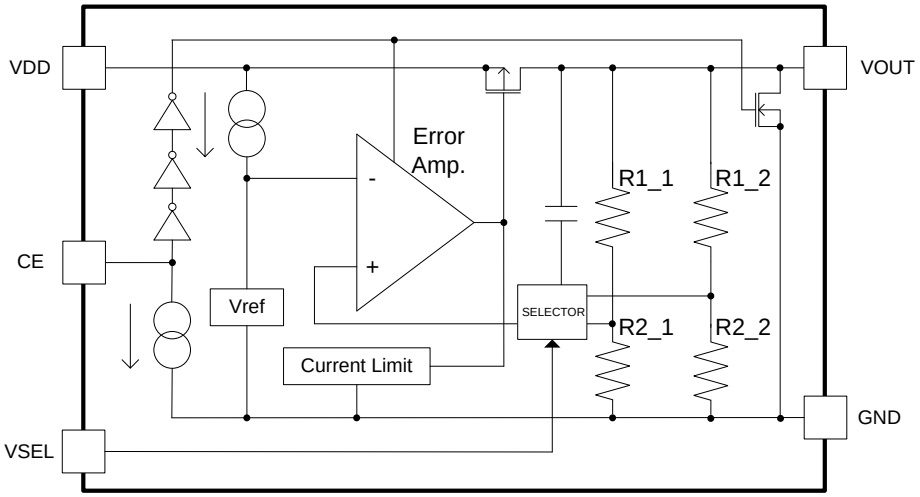
Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP155Zxxx∗-E2-F	WLCSP-5-P1	5,000 pcs	Yes	Yes

xxx: Specify a combination of two set output voltages (V_{SET1}/ V_{SET2}).
V_{SET1}/ V_{SET2} can be selected within the range of 1.6 V to 3.6 V.

∗: Specify the auto-discharge option.
B: Auto discharge function included

BLOCK DIAGRAM

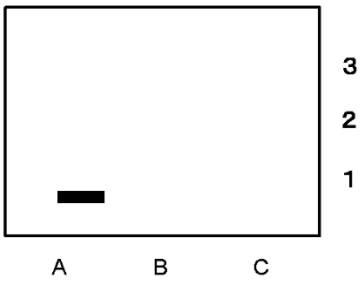


RP155Z Block Diagram

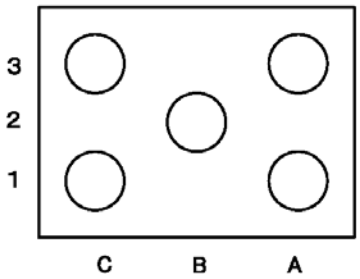
(1) Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

PIN DESCRIPTIONS

Top View



Bottom View



WLCSP-5-P1 Pin Configurations

WLCSP-5-P1 Pin Descriptions

Pin No.	Symbol	Description
A1	CE	Chip Enable Pin, Active-high
A3	VSEL	Output Voltage Selector Pin, V_{SET1}-low, V_{SET2}-high
B2	GND	Ground Pin
C1	VOUT	Output Pin
C3	VDD	Input Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	−0.3 to 6.0	V
V_{CE}	CE Pin Input Voltage	−0.3 to 6.0	V
V_{SEL}	VSEL Pin Input Voltage	−0.3 to 6.0	V
V_{OUT}	VOUT Pin Output Voltage	−0.3 to V_{IN}+0.3	V
I_{OUT}	Output Current	510	mA
P_D	Power Dissipation (JEDEC STD.51-9)(1)	430	mW
Tj	Junction Temperature	−40 to 125	°C
Tstg	Storage Temperature	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage(2)	1.9 to 5.25	V
Ta	Operating Temperature	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* for detailed information.
(2) In case of operating the device beyond 5.25 V, do not exceed 5.5 V with 500 total operating hours.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{SET} +1.0 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 µF, V_{SEL} = low/ high, unless otherwise noted.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP155Z Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	Ta = 25°C	x0.990		x1.010	V
		−40°C ≤ Ta ≤ 85°C	[x0.985]		[x1.015]	V
I_{OUT}	Output Current		[200]			mA
ΔV_{OUT} /ΔI_{OUT}	Load Regulation	1 mA ≤ I_{OUT} ≤ 200 mA		1	[10]	mV
V_{DIF}	Dropout Voltage	I_{OUT} = 200 mA	Refer to *Product-specific Electrical Characteristics*			
I_{SS}	Supply Current	I_{OUT} = 0 mA		80	[125]	µA
Istandby	Standby Current	V_{CE} = 0 V		0.1	1.0	µA
ΔV_{OUT} /ΔV_{IN}	Line Regulation	V_{SET} + 0.5 V ≤ V_{IN} ≤ 5.25 V		0.02	[0.10]	%/V
RR	Ripple Rejection	f = 1 kHz, Ripple 0.2 Vp-p, V_{IN} = V_{SET} +1.0 V, I_{OUT} = 30 mA (V_{OUT} ≤ 2.0 V, V_{IN} = 3.0 V)		75		dB
ΔV_{OUT} /ΔTa	Output Voltage Temperature Coefficient	−40°C ≤ Ta ≤ 85°C		±30		ppm /°C
I_{SC}	Short Current Limit	V_{OUT} = 0 V		50		mA
I_{PD}	CE Pull-down Current			0.3	[0.6]	µA
V_{CEH}	CE Input Voltage "H"		[1.0]			V
V_{CEL}	CE Input Voltage "L"				[0.4]	V
V_{VSELH}	VSEL Input Voltage "H"		[1.0]			V
V_{VSELL}	VSEL Input Voltage "L"				[0.4]	V
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature		165		°C
T_{TSR}	Thermal Shutdown Released Temperature	Junction Temperature		100		°C
en	Output Noise	BW = 10 Hz to 100 kHz		21 x V_{SET}		µVrms
R_{LOW}	Low Output Nch Tr. ON Resistance	V_{IN} = 4.0 V, V_{CE} = 0 V		60		Ω

All test items listed under *ELECTRICAL CHARACTERISTICS* are done under the pulse load condition (Tj ≈ Ta = 25°C) except Output Voltage Temperature Coefficient, Output Noise and Ripple Rejection.

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = V_{SET} +1.0 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 µF, V_{SEL} = low/high, unless otherwise noted.

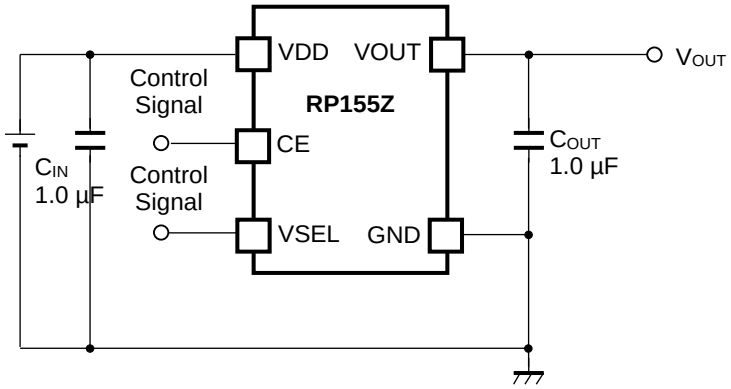
The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP155Z Product-specific Electrical Characteristics (Ta = 25°C)

Product Name	V_{SET1}/ V_{SET2}	V_{OUT} [V]						V_{DIF} [V]	
		Ta = 25°C			−40°C ≤ Ta ≤ 85°C				
		Min.	Typ.	Max.	Min.	Typ.	Max.	Typ.	Max.
RP155Z001B	V_{SET1}	1.782	1.800	1.818	[1.773]	1.800	[1.827]	0.100	[0.138]
	V_{SET2}	2.822	2.850	2.878	[2.808]	2.850	[2.892]	0.085	[0.117]
RP155Z003B	V_{SET1}	1.584	1.600	1.616	[1.576]	1.600	[1.624]	-(1)	-1
	V_{SET2}	3.564	3.600	3.636	[3.546]	3.600	[3.654]	0.071	[0.105]
RP155Z004B	V_{SET1}	1.782	1.800	1.818	[1.773]	1.800	[1.827]	0.100	[0.138]
	V_{SET2}	3.267	3.300	3.333	[3.251]	3.300	[3.349]	0.071	[0.105]
RP155Z005B	V_{SET1}	3.267	3.300	3.333	[3.251]	3.300	[3.349]	0.071	[0.105]
	V_{SET2}	1.782	1.800	1.818	[1.773]	1.800	[1.827]	0.100	[0.138]
RP155Z006B	V_{SET1}	2.871	2.900	2.929	[2.857]	2.900	[2.943]	0.085	[0.117]
	V_{SET2}	1.782	1.800	1.818	[1.773]	1.800	[1.827]	0.100	[0.138]

(1) The input voltage should be equal or more than the minimum operating voltage (1.9 V).

APPLICATION INFORMATION



RP155Z Typical Application Circuit

External Components Example

Symbol	Description
C_{IN}, C_{OUT}	Ceramic Capacitor, 1.0 µF, GRM155B31A105KE15, MURATA

Technical Notes on the External Components

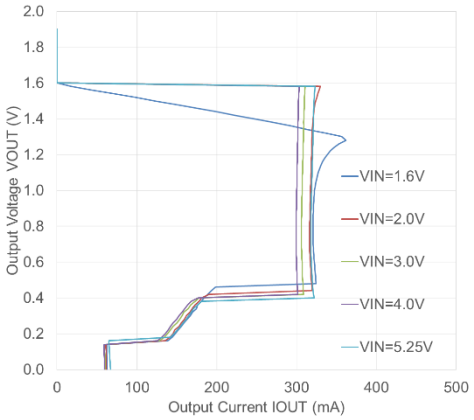
- In this device, phase compensation is provided to secure stable operation even when the load current is varied. For this purpose, use a 1.0 µF or more output capacitor (C_{OUT}). In case of using a tantalum type capacitor with a large ESR (Equivalent Series Resistance), the output might become unstable. Evaluate your circuit including consideration of frequency characteristics.
- Ensure the VDD and GND lines are sufficiently robust. If their impedances are too high, noise pickup or unstable operation may result. Connect a 1.0 µF or more input capacitor (C_{IN}) between the VDD and GND pins with shortest-distance wiring. Also, connect an output capacitor (C_{OUT}) between the VOUT and GND pins with shortest-distance wiring.

TYPICAL CHARACTERISTICS

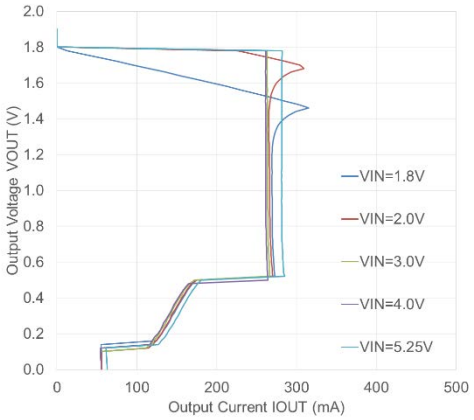
Note: Typical Characteristics are intended to be used as reference data, they are not guaranteed.

1) Output Voltage vs. Output Current (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

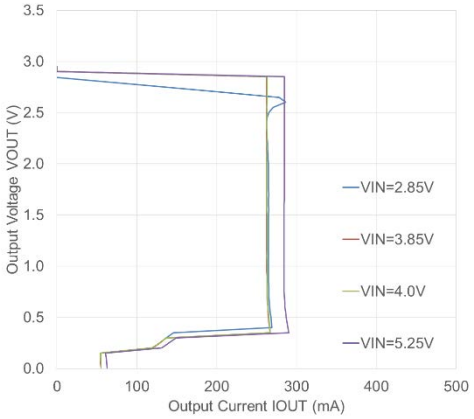
1.6 V (V_{SET1}/ V_{SET2})



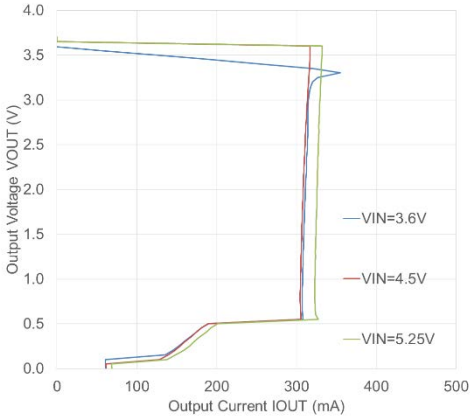
1.8 V (V_{SET1}/ V_{SET2})



2.85 V (V_{SET1}/ V_{SET2})

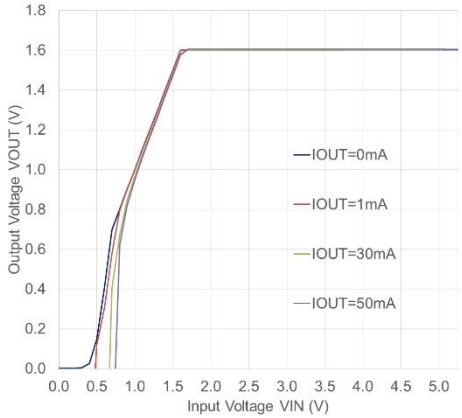


3.6 V (V_{SET1}/ V_{SET2})



2) Output Voltage vs. Input Voltage (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

1.6 V (V_{SET1}/ V_{SET2})



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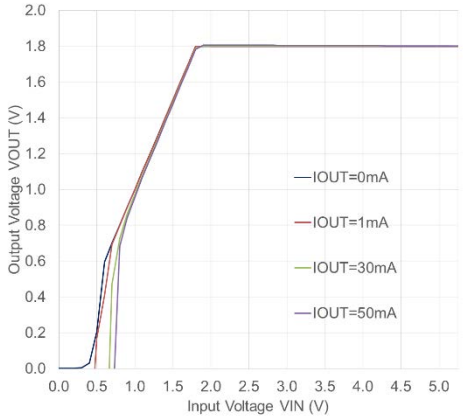

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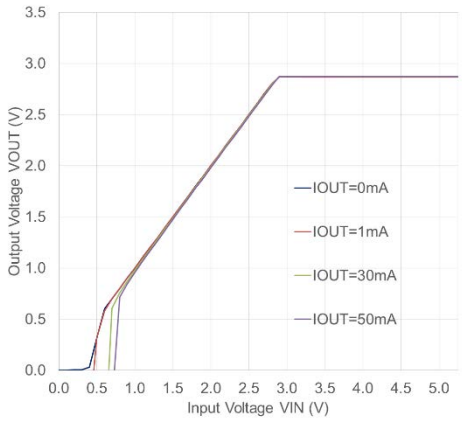
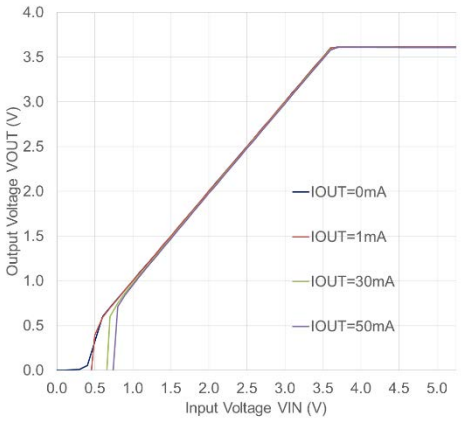
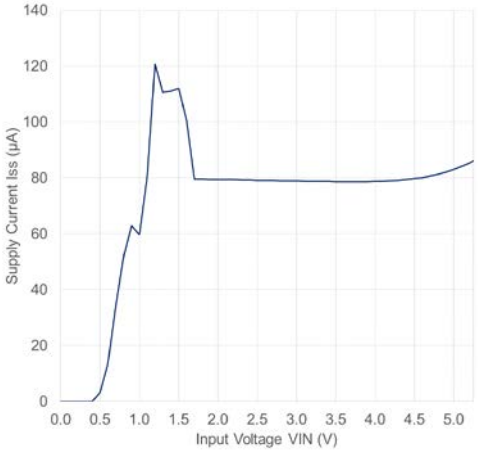


3.6 V (V_{SET1}/ V_{SET2})

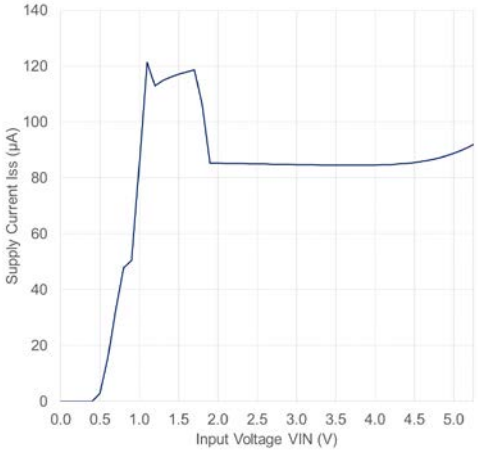


3) Supply Current vs. Input Voltage (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

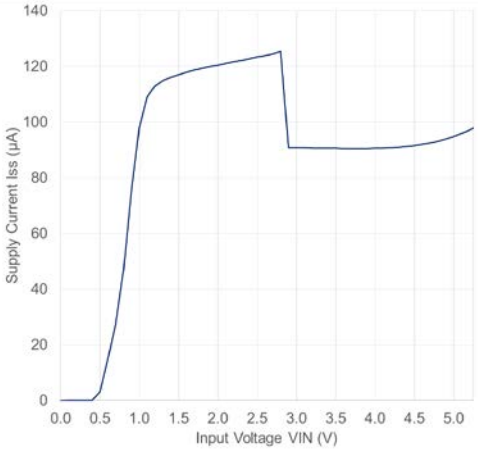
1.6 V (V_{SET1}/ V_{SET2})



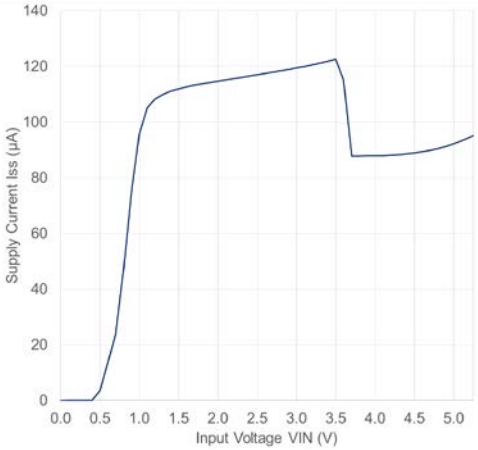
1.8 V (V_{SET1}/ V_{SET2})



2.85 V (V_{SET1}/ V_{SET2})

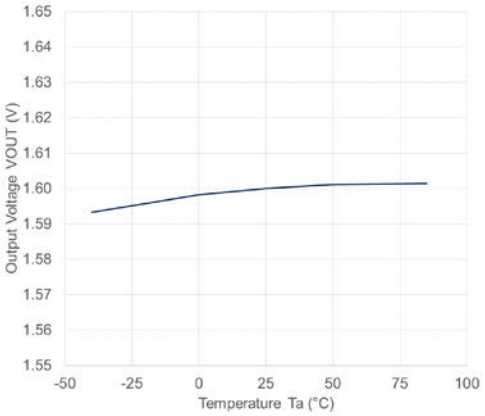


3.6 V (V_{SET1}/ V_{SET2})

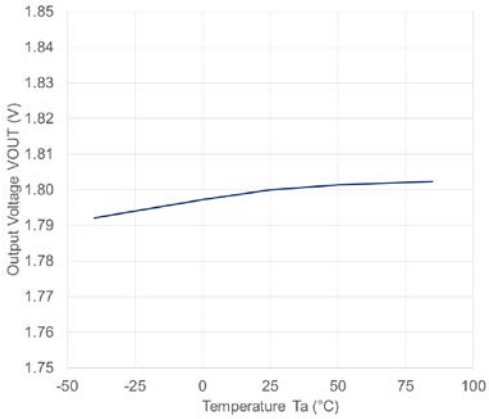


4) Output Voltage vs. Temperature (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF)

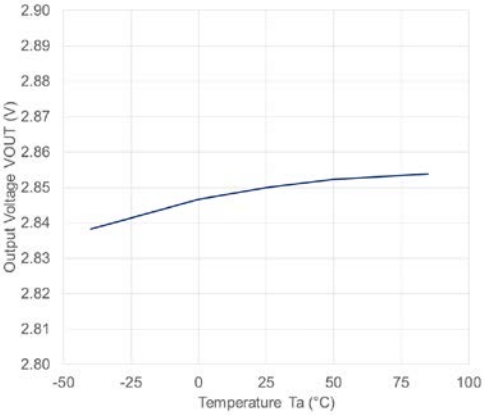
1.6 V (V_{SET1}/ V_{SET2})
V_{IN} = 2.6 V, I_{OUT} = 1 mA



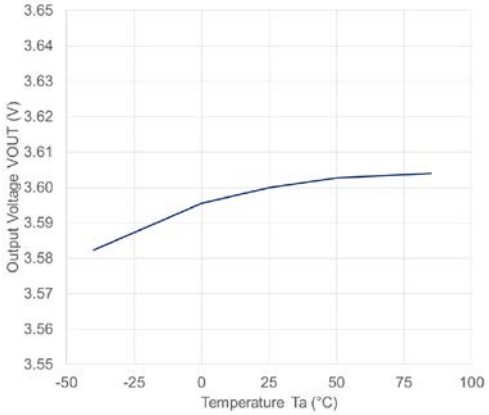
1.8 V (V_{SET1}/ V_{SET2})
V_{IN} = 2.8 V, I_{OUT} = 1 mA



2.85 V (V_{SET1}/ V_{SET2})
V_{IN} = 3.85 V, I_{OUT} = 1 mA

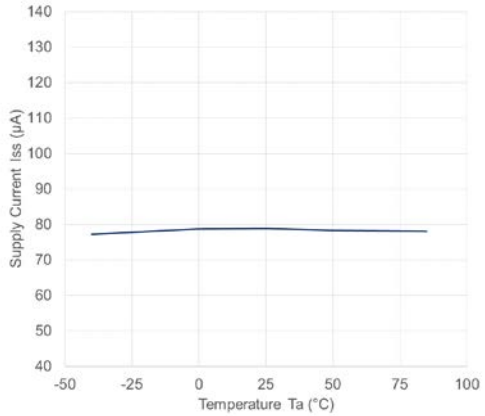


3.6 V (V_{SET1}/ V_{SET2})
V_{IN} = 4.6 V, I_{OUT} = 1 mA

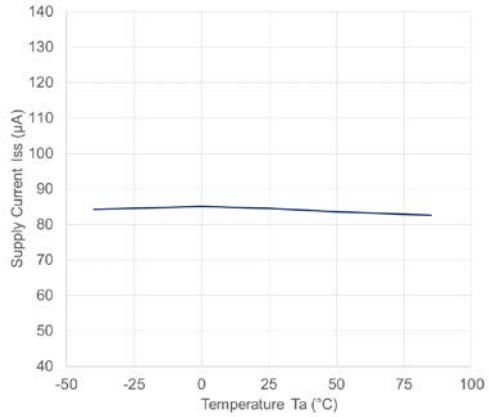


5) Supply Current vs. Temperature

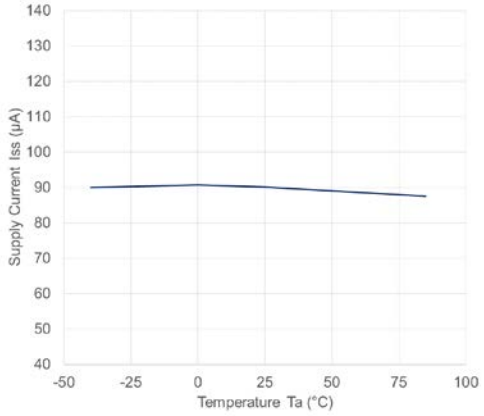
1.6 V (V_{SET1}/ V_{SET2})
V_{IN} = 2.6 V, I_{OUT} = 0 mA



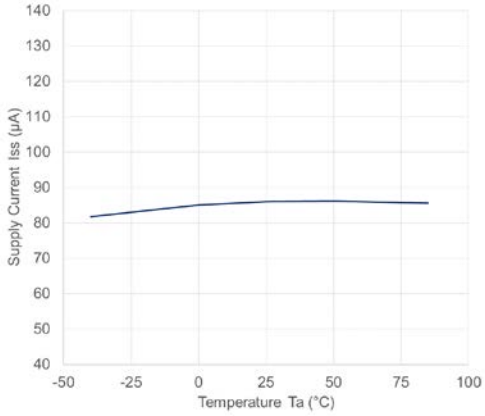
1.8 V (V_{SET1}/ V_{SET2})
V_{IN} = 2.8 V, I_{OUT} = 0 mA



2.85 V (V_{SET1}/ V_{SET2})
V_{IN} = 3.85 V, I_{OUT} = 0 mA

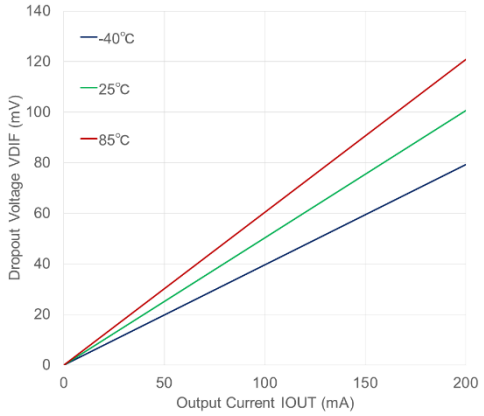


3.6 V (V_{SET1}/ V_{SET2})
V_{IN} = 4.6 V, I_{OUT} = 0 mA

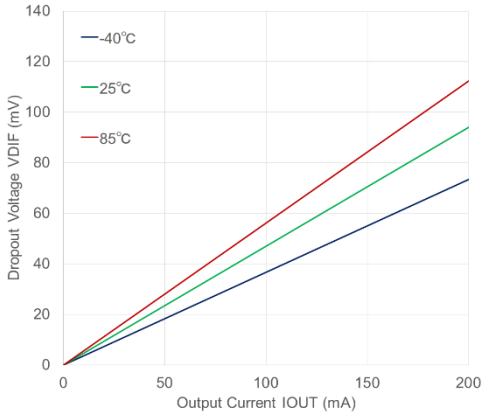


6) Dropout Voltage vs. Output Current (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF)

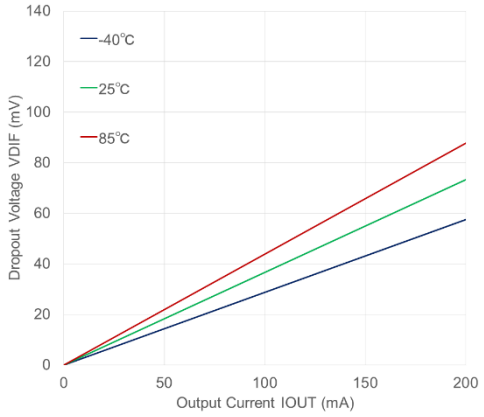
1.6 V (V_{SET1}/ V_{SET2})



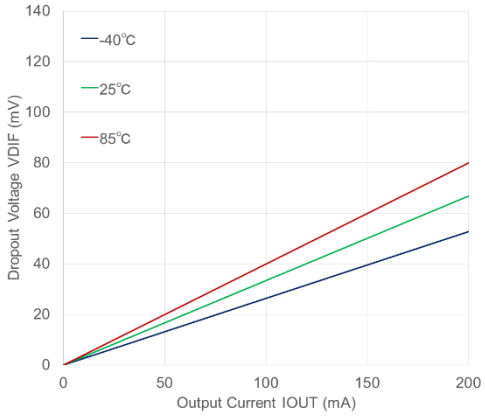
1.8 V (V_{SET1}/ V_{SET2})



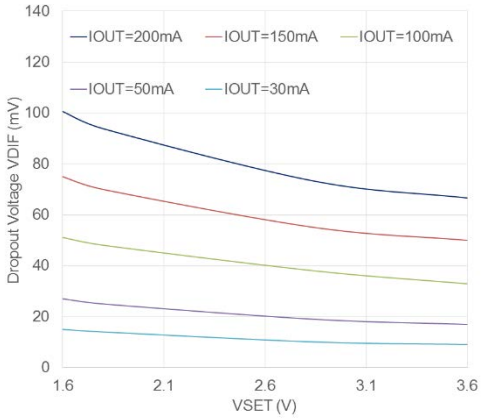
2.85 V (V_{SET1}/ V_{SET2})



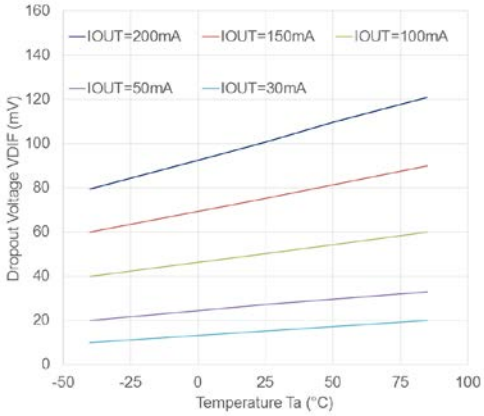
3.6 V (V_{SET1}/ V_{SET2})



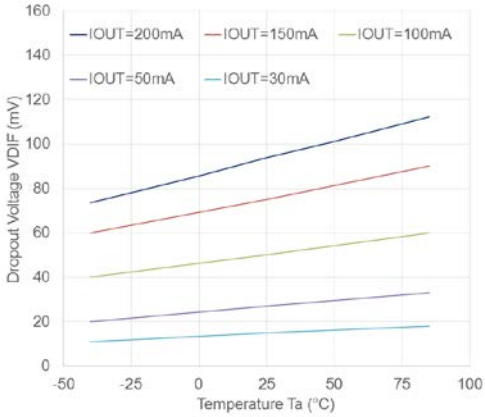
7) Dropout Voltage vs. VR_V_{SET} (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)
V_{SET1}/ V_{SET2}



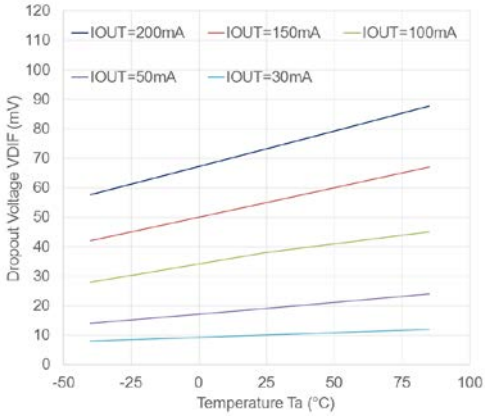
8) Dropout Voltage vs. Temperature (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF)
1.6 V (V_{SET1}/ V_{SET2})



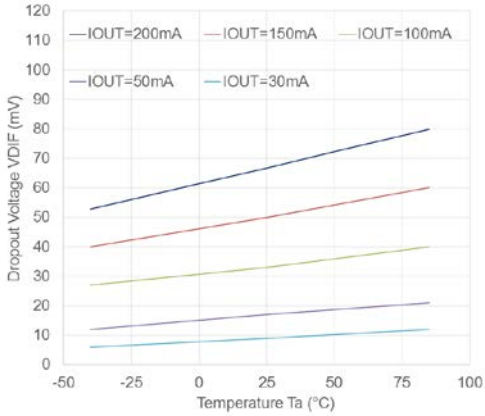
1.8 V (V_{SET1}/ V_{SET2})



2.85 V (V_{SET1}/ V_{SET2})



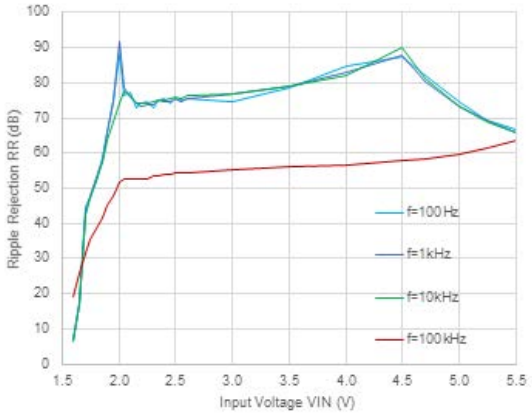
3.6 V (V_{SET1}/ V_{SET2})



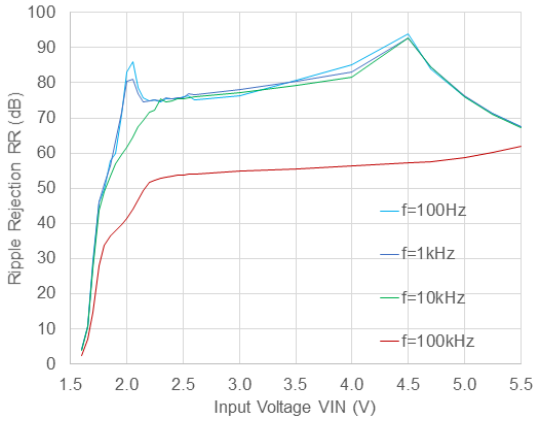
9) Ripple Rejection vs. Input Bias (C_{IN} = none, C_{OUT} = Ceramic 1.0 µF, Input Ripple = 0.2 Vp-p, Ta = 25°C)

1.6 V (V_{SET1}/ V_{SET2})

I_{OUT} = 1 mA

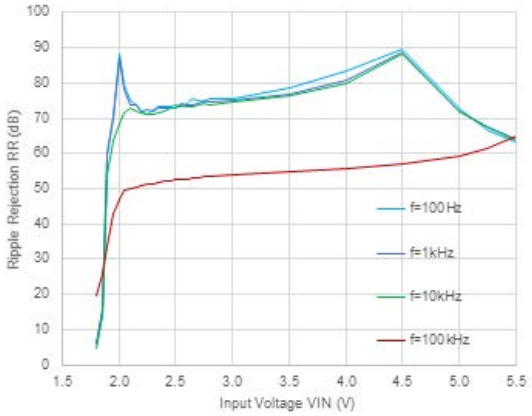


I_{OUT} = 30 mA

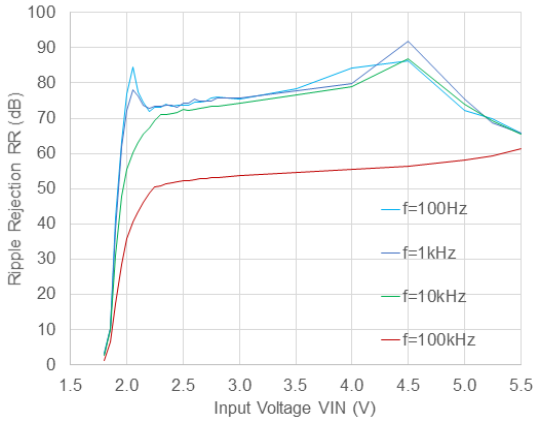


1.8 V (V_{SET1}/ V_{SET2})

I_{OUT} = 1 mA

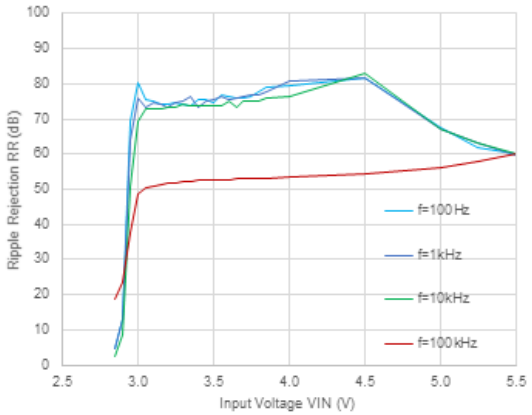


I_{OUT} = 30 mA

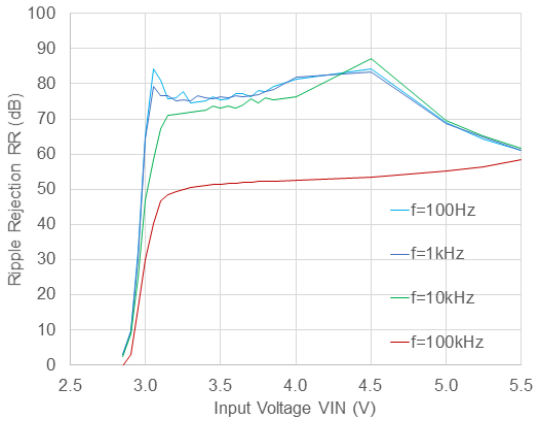


2.85 V (V_{SET1}/ V_{SET2})

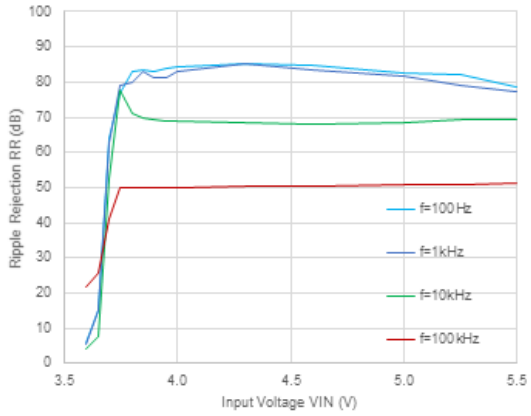
I_{OUT} = 1 mA



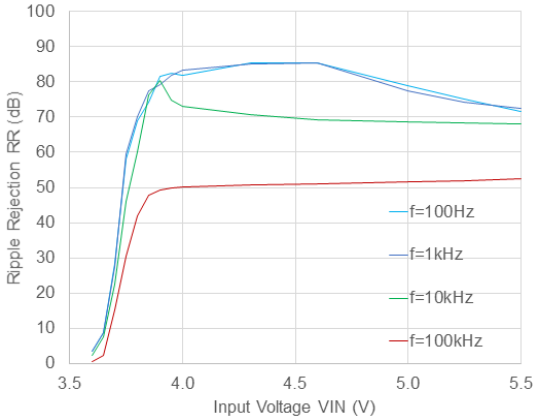
I_{OUT} = 30 mA



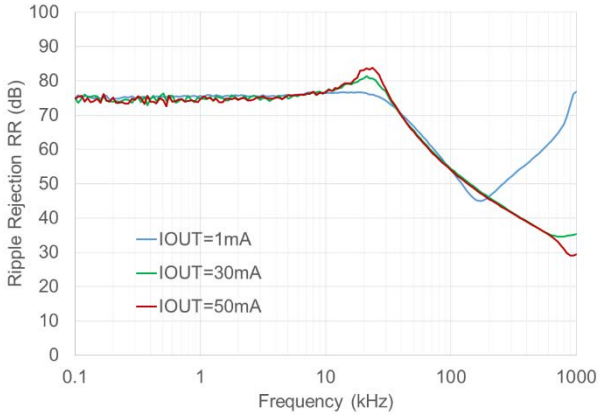
3.6 V (V_{SET1}/ V_{SET2})
I_{OUT} = 1 mA



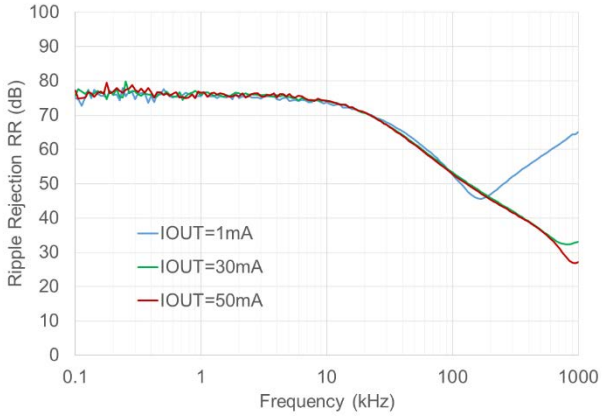
I_{OUT} = 30 mA



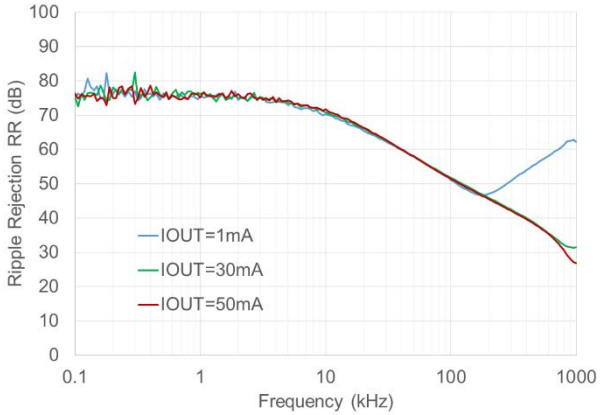
10) Ripple Rejection vs. Frequency (C_{IN} = none, C_{OUT} = Ceramic 1.0 µF, Input Ripple = 0.2 Vp-p, Ta = 25°C)
1.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.6 V



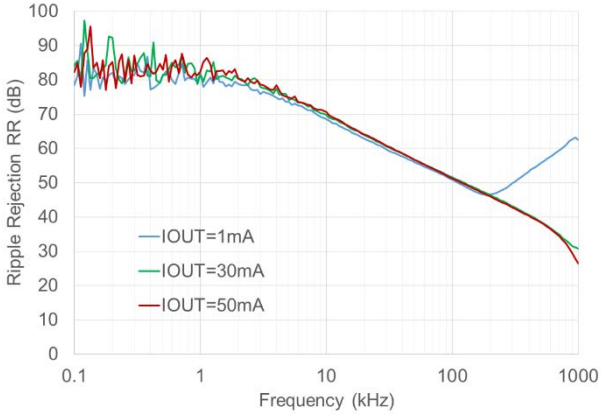
1.8 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.8 V



2.85 V (V_{SET1}/ V_{SET2}), V_{IN} = 3.85 V

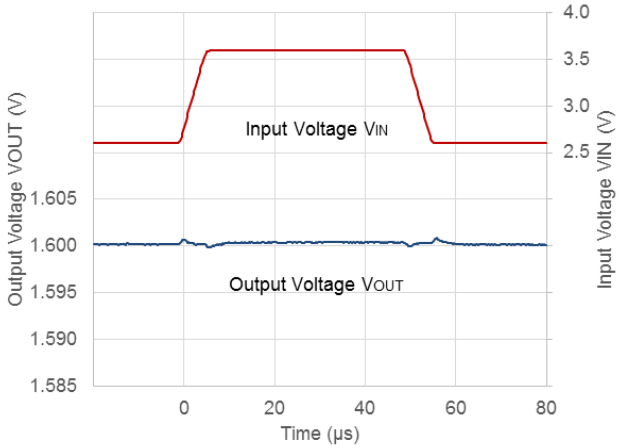


3.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 4.6 V

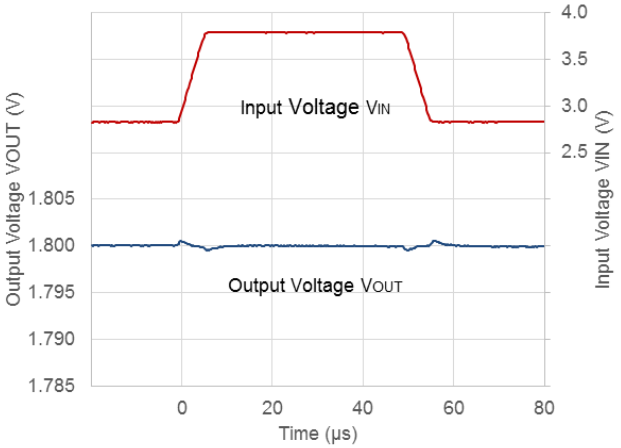


11) Input Transient Response (C_{IN} = none, C_{OUT} = Ceramic 1.0 µF, I_{OUT} = 30 mA, tr = tf = 5 µs, Ta = 25°C)

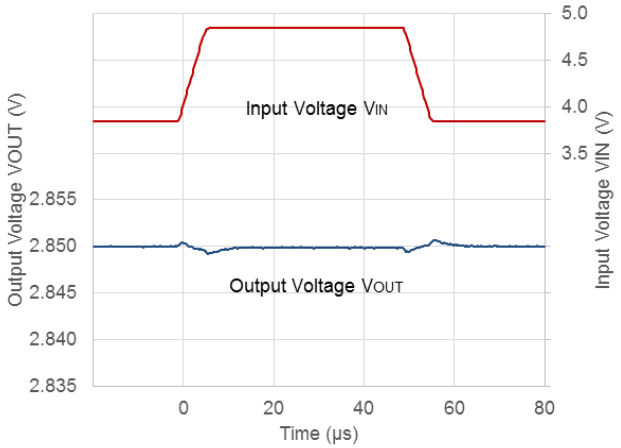
1.6 V (V_{SET1}/ V_{SET2})



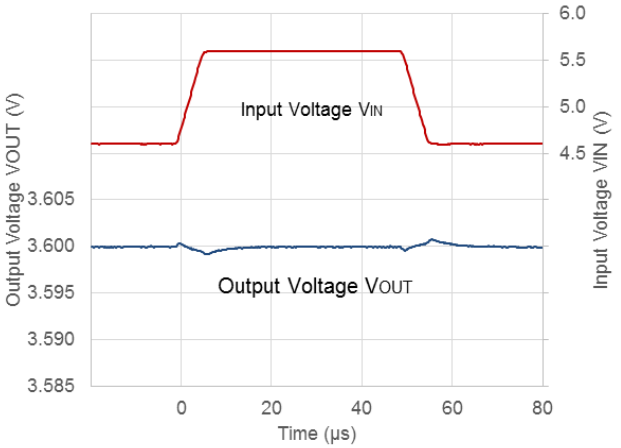
1.8 V (V_{SET1}/ V_{SET2})



2.85 V (V_{SET1}/ V_{SET2})



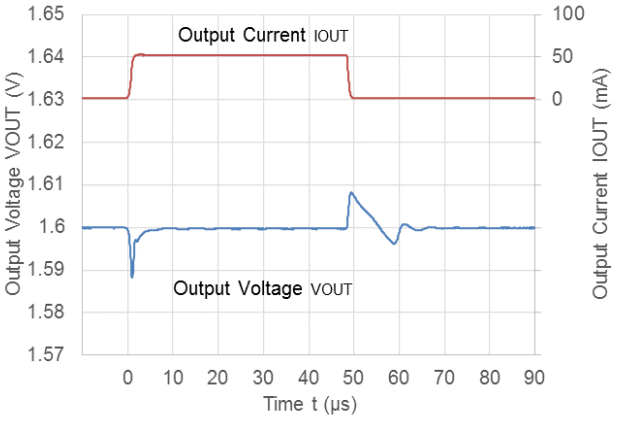
3.6 V (V_{SET1}/ V_{SET2})



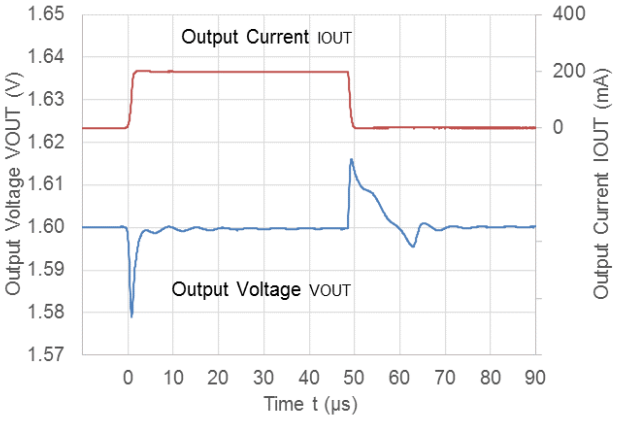
12) Load Transient Response (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, tr = tf = 0.5 µs, Ta = 25°C)

1.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.6 V

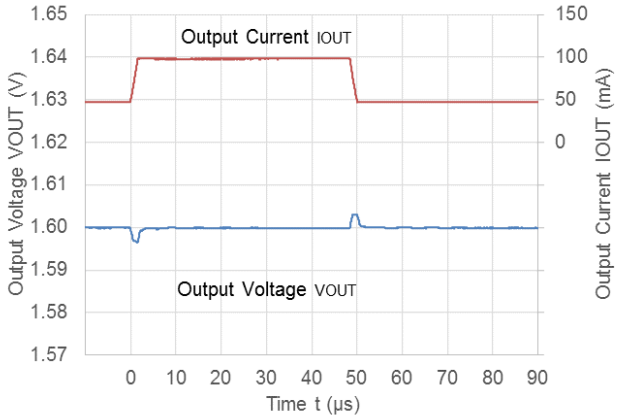
1 mA ⇔ 50 mA



1 mA ⇔ 200 mA

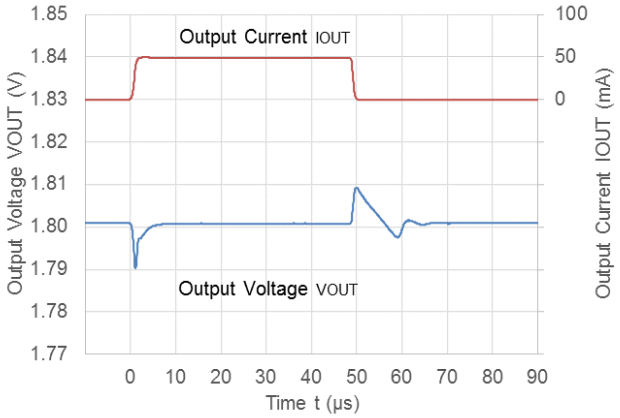


50 mA ⇔ 200 mA

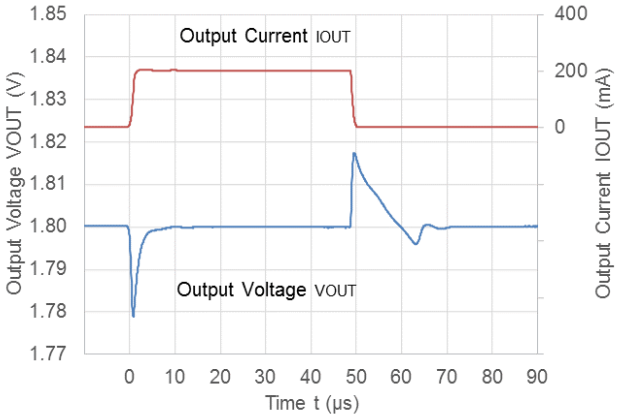


1.8 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.8 V

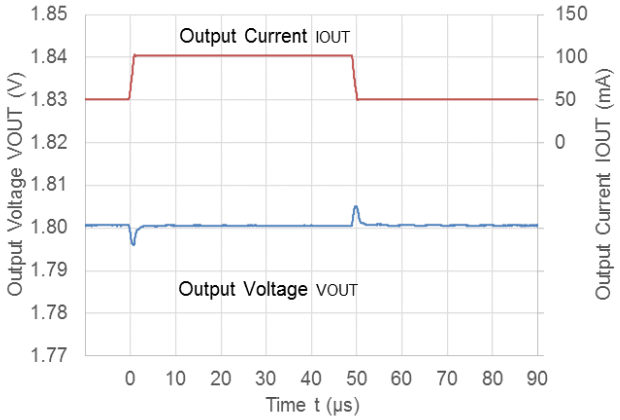
1 mA ⇔ 50 mA



1 mA ⇔ 200 mA

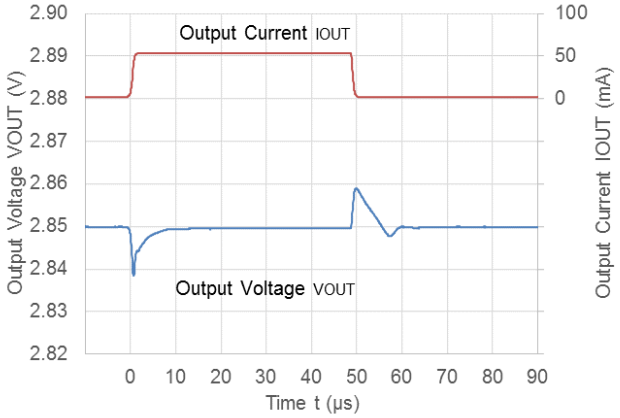


50 mA ⇔ 200 mA

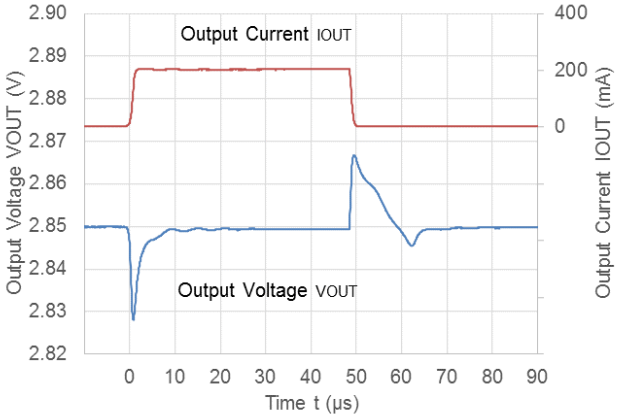


2.85 V (V_{SET1}/ V_{SET2}), V_{IN} = 3.85 V

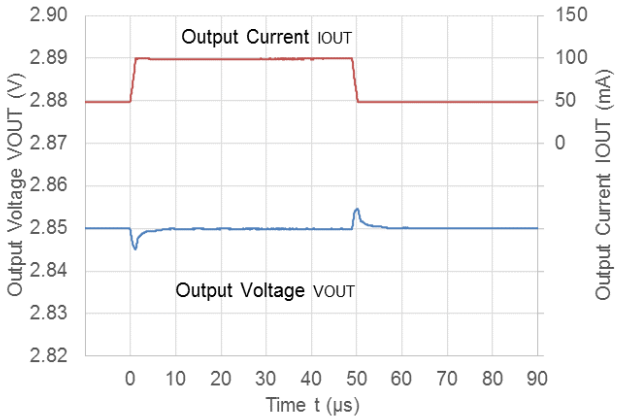
1 mA ⇔ 50 mA



1 mA ⇔ 200 mA

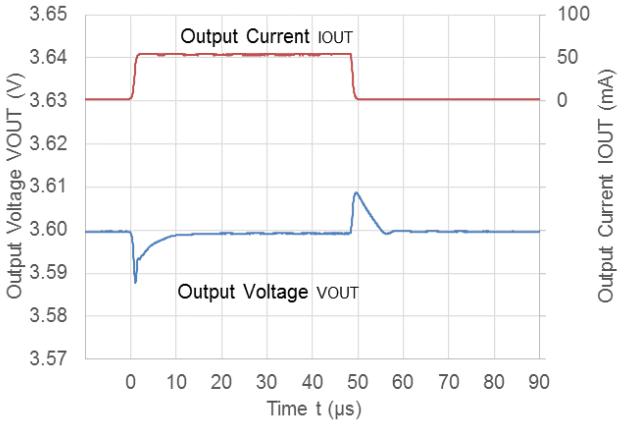


50 mA ⇔ 200 mA

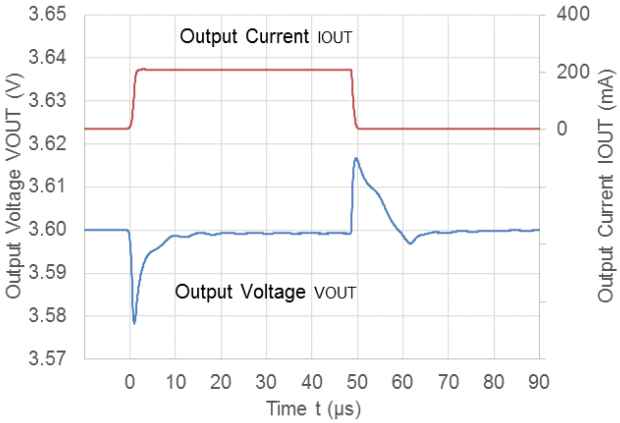


3.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 4.6 V

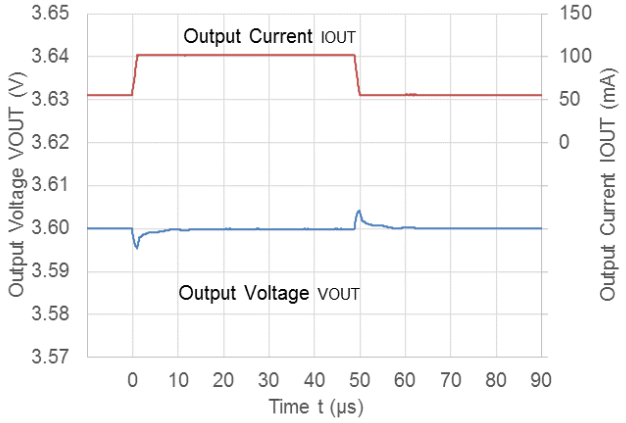
1 mA ⇔ 50 mA



1 mA ⇔ 200 mA

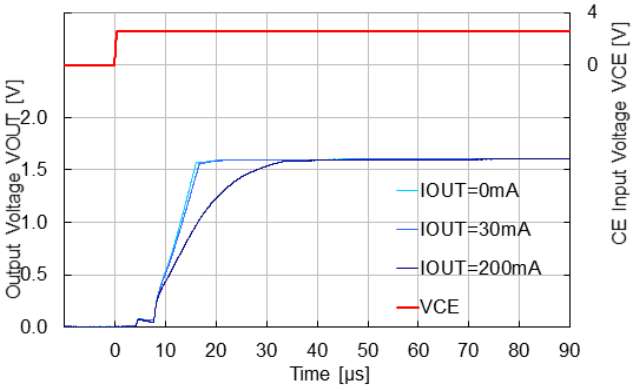


50 mA ⇔ 200 mA

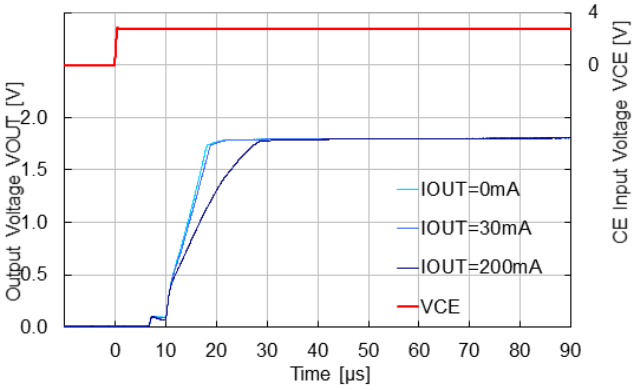


13) Turn On Speed with CE pin (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

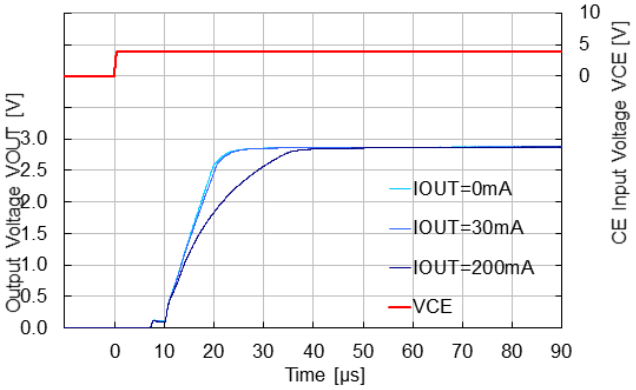
1.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.6 V



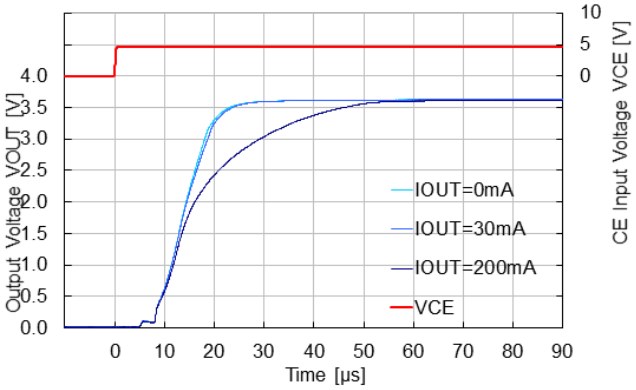
1.8 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.8 V



2.85 V (V_{SET1}/ V_{SET2}), V_{IN} = 3.85 V

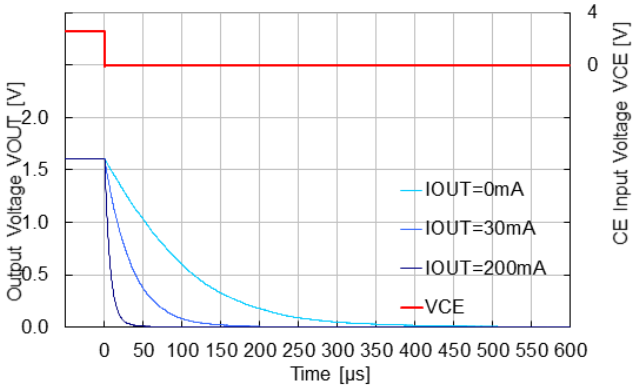


3.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 4.6 V

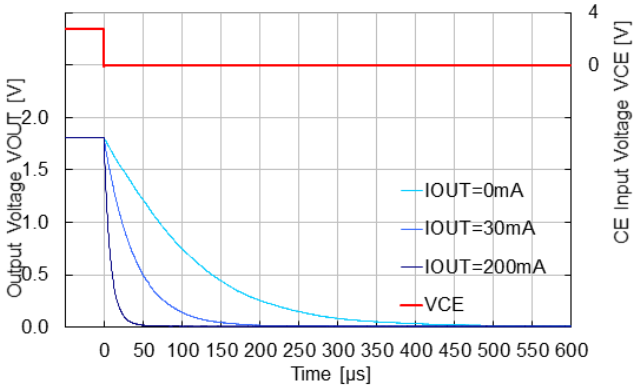


14) Tum Off Speed with CE pin (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

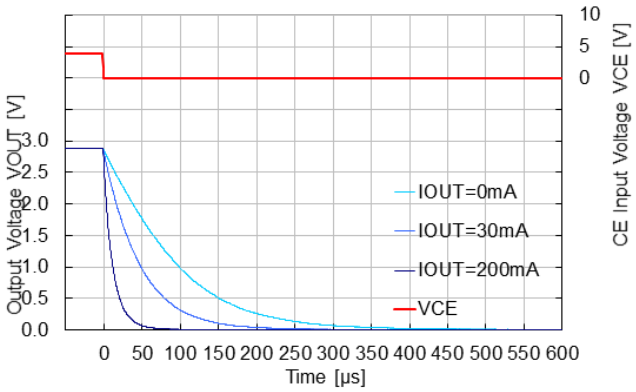
RP155ZxxxB
1.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.6 V



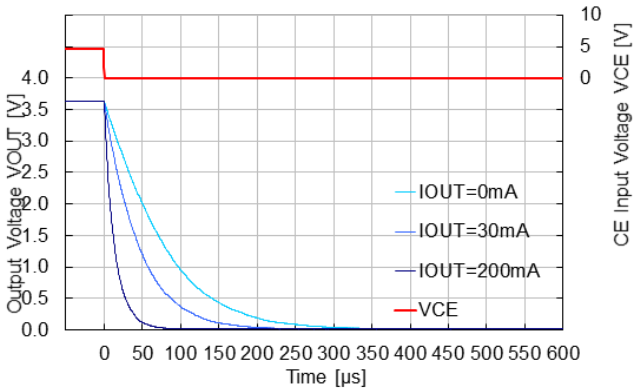
RP155ZxxxB
1.8 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.8 V



RP155ZxxxB
2.85 V (V_{SET1}/ V_{SET2}), V_{IN} = 3.85 V

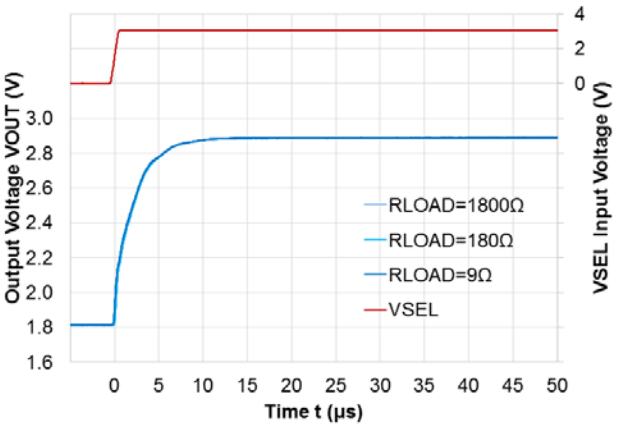


RP155ZxxxB
3.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 4.6 V

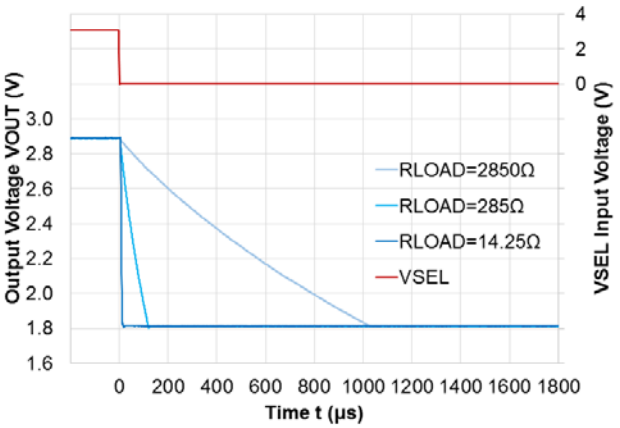


15) V_{OUT} Transient Response with VSEL Pin (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, tr = tf = 5 µs, Ta = 25°C)

RP155Z001B
V_{SET1} (1.8 V) ⇒ V_{SET2} (2.85 V)

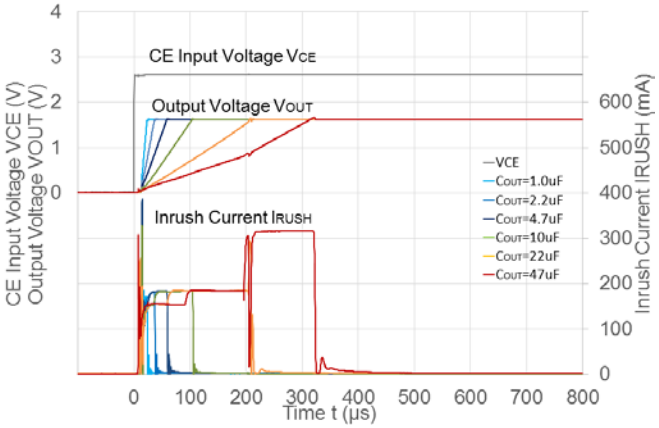


RP155Z001B
V_{SET2} (2.85 V) ⇒ V_{SET1} (1.8 V)

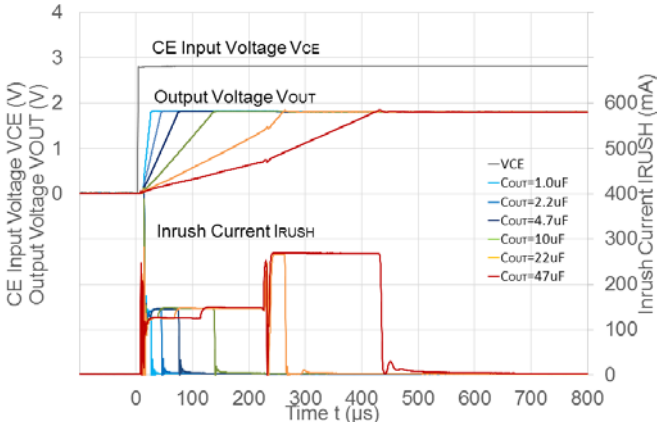


16) Inrush Current (C_{IN} = Ceramic 1.0 µF, I_{OUT} = 0 mA, Ta = 25°C)

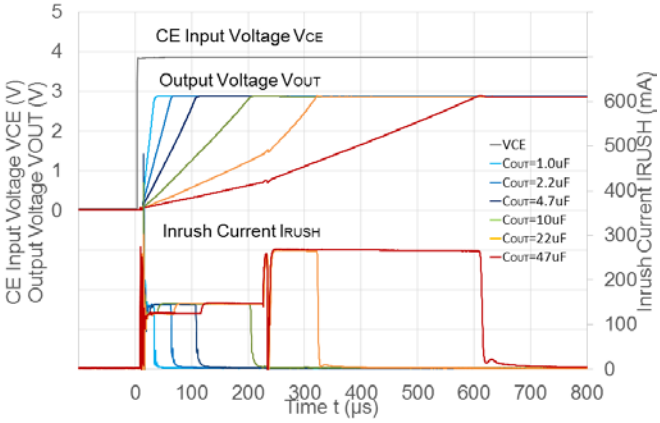
1.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.6 V



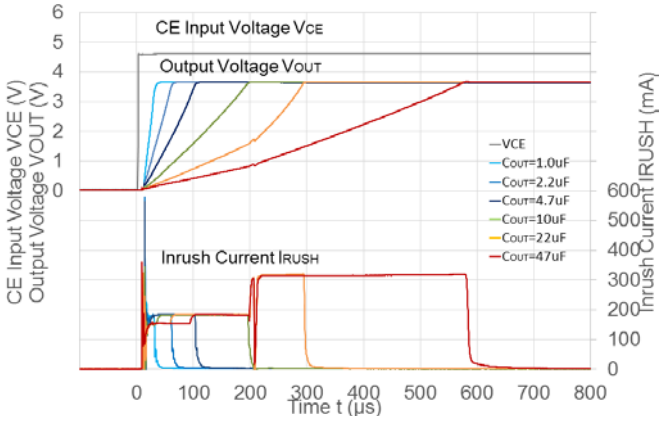
1.8 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.8 V



2.85 V (V_{SET1}/ V_{SET2}), V_{IN} = 3.85 V



3.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 4.6 V



EQUIVALENT SERIES RESISTANCE VS. OUTPUT CURRENT

A ceramic output capacitor is recommended to be used but any output capacitor with low ESR could also be used. The graphs below show the relations between output current and ESR of an output capacitor when the average white noise level is 40 µV or less.

1.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 1.9 V to 5.25 V

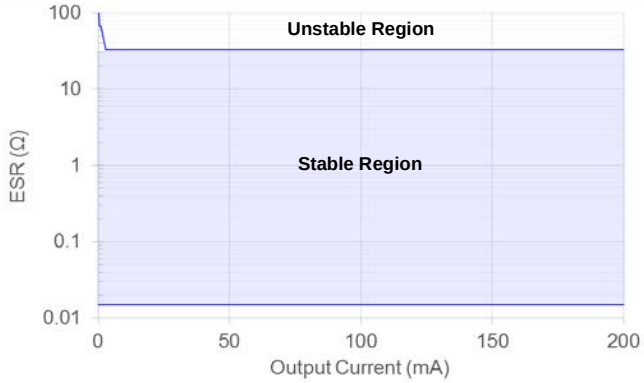


Fig. 1 Range of Stable ESR Values

1.8 V (V_{SET1}/ V_{SET2}), V_{IN} = 1.9 V to 5.25 V

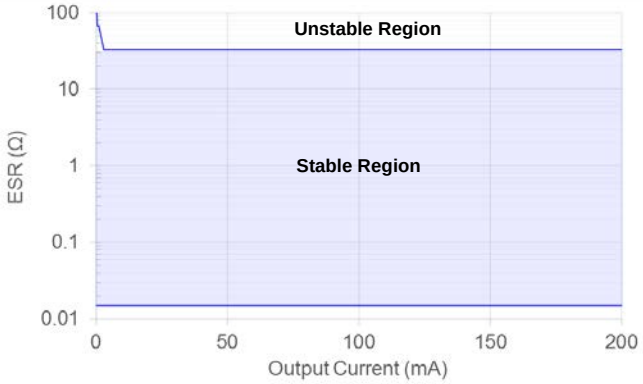


Fig. 2 Range of Stable ESR Values

2.85 V (V_{SET1}/ V_{SET2}), V_{IN} = 2.85 V to 5.25 V

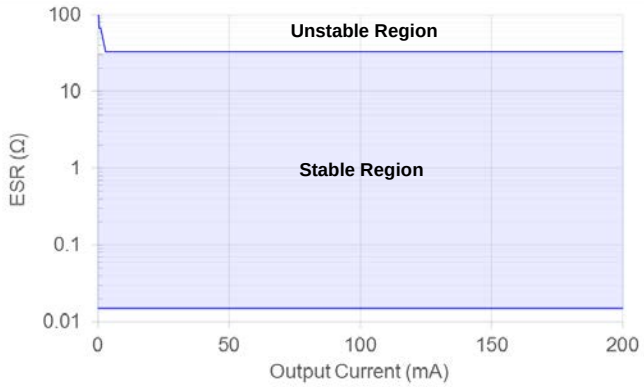


Fig. 3 Range of Stable ESR Values

3.6 V (V_{SET1}/ V_{SET2}), V_{IN} = 3.6 V to 5.25 V

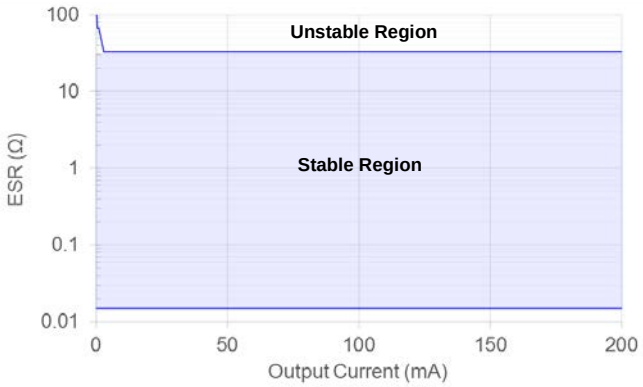


Fig. 4 Range of Stable ESR Values

Ver. A

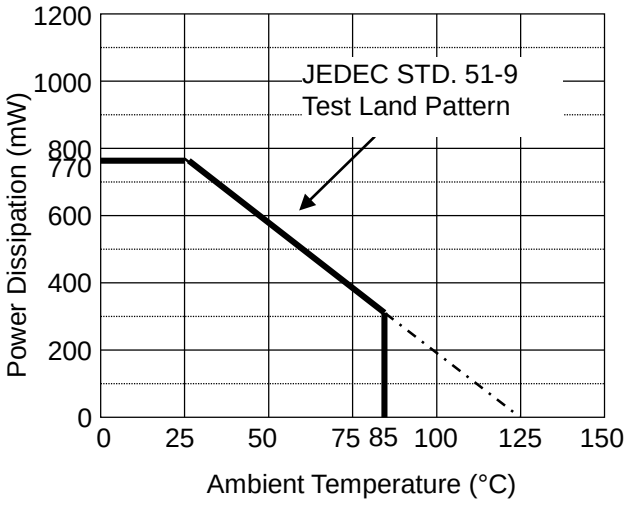
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

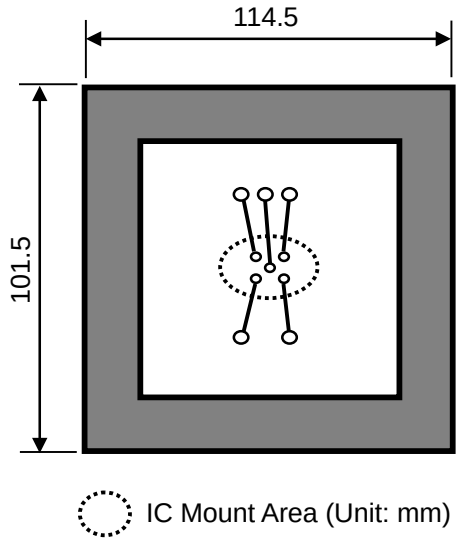
	JEDEC STD. 51-9 Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (4-Layer Boards)
Board Dimensions	101.5 mm x 114.5 mm x 1.6 mm
Copper Ratio	Outer Layers (First and Fourth Layers): Approx. 60% Inner Layers (Second and Third Layers): Approx. 100%

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	JEDEC STD. 51-9 Test Land Pattern
Power Dissipation	770 mW
Thermal Resistance	θja = (125 − 25°C) / 0.77 W = 129°C/W



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

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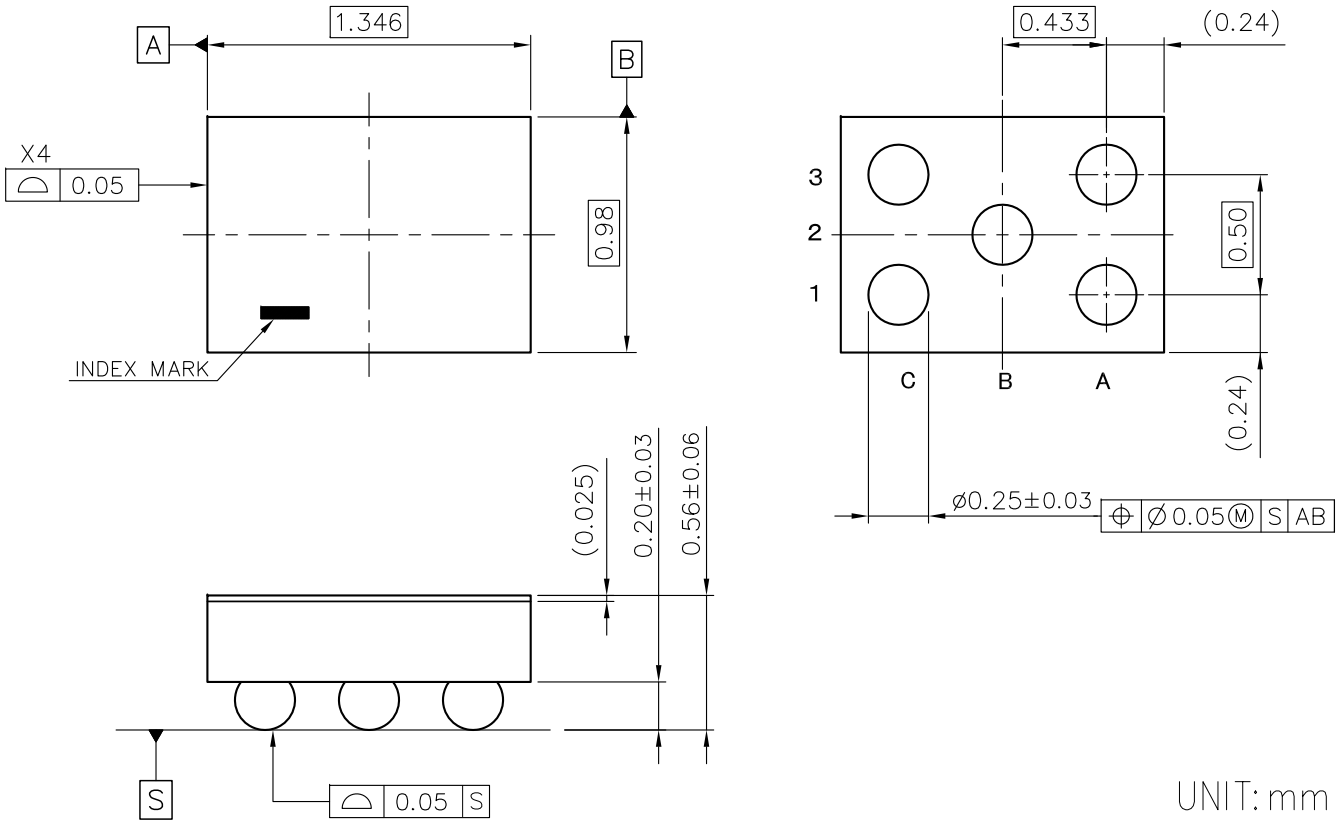

WLCSP-5-P1 Package Dimensions

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