RS2051

Green-Mode PWM Controller with Frequency Jiggling

General Description

The RS2051 is a highly integrated low cost current mode PWM controller, which is ideal for small power current mode of offline AC-DC fly-back converter applications. Making use of external resistors, the IC changes the operating frequency and automatically enters the Burst/CRM (Cycle Reset Mode) under light-load/zero-load conditions. This can minimize standby power consumption and achieve power-saving functions. With a very low start-up current, the RS2051 could use a large value start-up resistor (2MΩ). Built-in synchronized slope compensation enhances the stability of the system and avoids sub-harmonic oscillation. Dynamic peak current limiting circuit minimizes output power change caused by delay time of the system over a universal AC input range. Leading edge blanking circuit on current sense input could remove the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design. Cycle-by-Cycle current limiting ensures safe operation even during short-circuit.

Excellent EMI performance is achieved built-in soft start with 1.2ms、soft driver and frequency jiggling to reduce EMI.

The RS2051 offers perfect protection like OVP, OLP, SCP, Sense Fault Protection, Latch Mode and OCP. The RS2051's output driver is soft clamped to maximum 18V to protect the power MOSFET. RS2051 is offered in SOT-26, SOP-8 and DIP-8 packages.

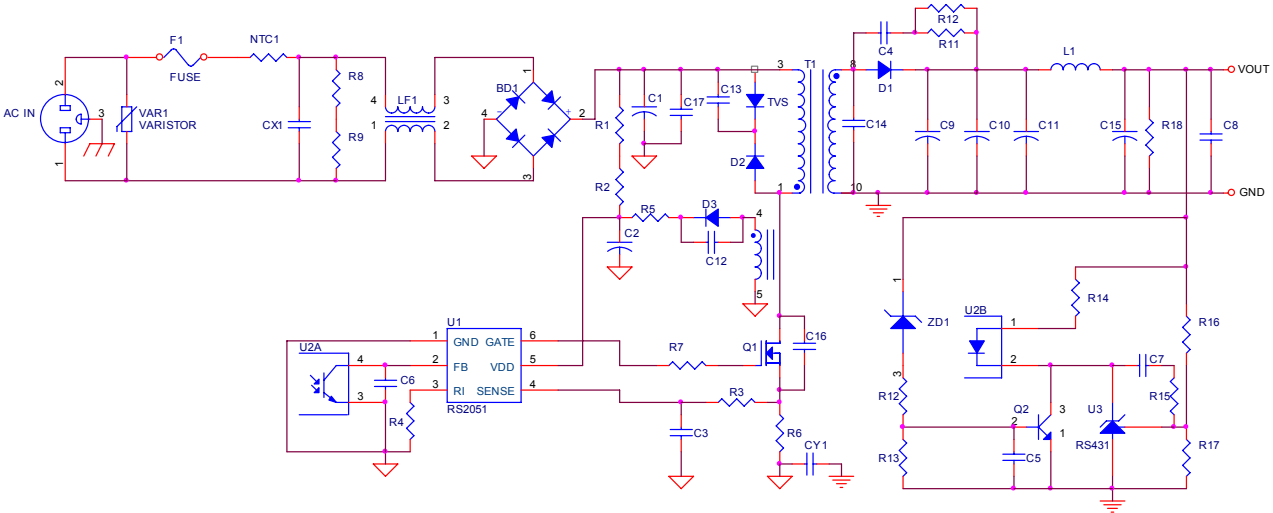
Features

- Low Cost, PWM, Burst & CRM (Cycle Reset Mode)
- Low Operating Current (1.2mA)
- Low Start-up Current (about 3μA)
- Under Voltage Lockout (UVLO)
- Built-in Synchronized Slope Compensation
- Built-in Frequency Jiggling for better EMI Signature
- Programmable PWM Frequency
- Audio Noise Free Operation
- Soft Clamped GATE output voltage 18V
- VDD over voltage protect 34V
- Cycle-by-cycle current limiting
- Sense Fault Protect ion
- Latch mode After OLP&SCP
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Switching AC/DC Adaptor
- Battery Charger
- Open Frame Switching Power Supply
- Standby Power Supplies
- VCR, SVR, STB, DVD & DVCD Player SMPS
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

Application Circuits

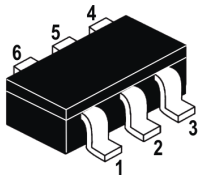


This integrated circuit can be damaged by ESD. Orister Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

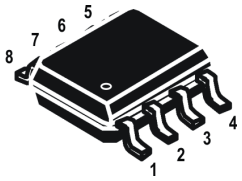
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Pin Assignments

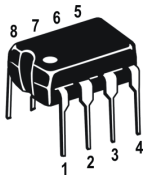
SOT-26



SOP-8



DIP-8



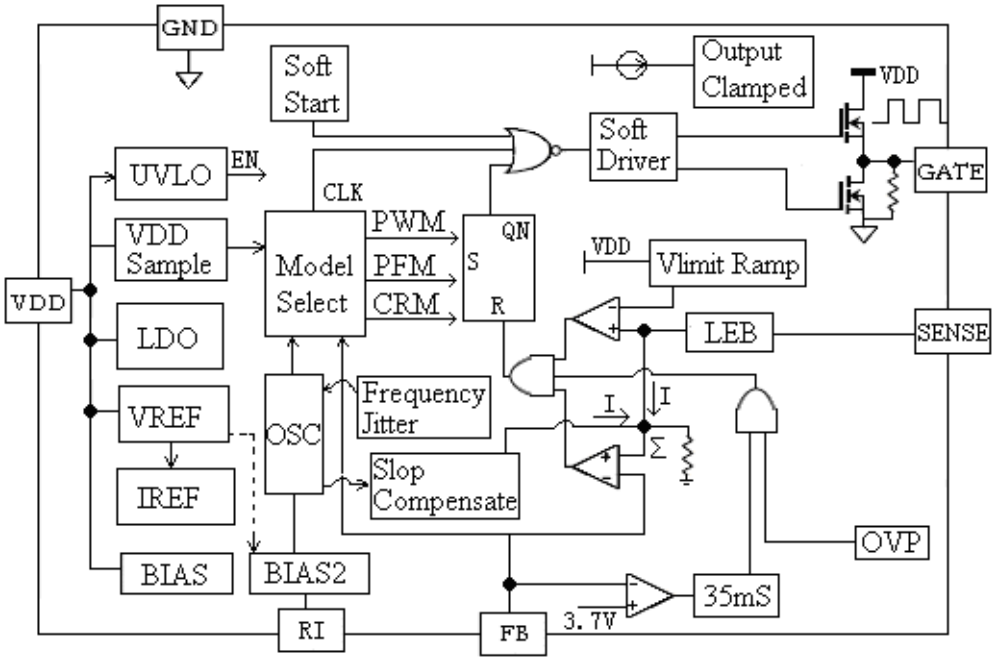
PACKAGE	PIN	SYMBOL	DESCRIPTION
SOT-26	1	GND	GND Pin
	2	FB	Voltage feedback pin. Output current of this pin could controls the PWM duty cycle、OLP and SCP.
	3	RI	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency
	4	SENSE	Current sense pin, connect to sense the MOSFET current
	5	VDD	Supply voltage pin
	6	GATE	Totem output to drive the external Power MOSFET.

PACKAGE	PIN	SYMBOL	DESCRIPTION
SOP-8 / DIP-8	1	GATE	Totem output to drive the external Power MOSFET.
	2	VDD	Supply voltage pin
	3, 6	NC	No Connect
	4	SENSE	Current sense pin, connect to sense the MOSFET current
	5	RI	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency
	7	FB	Voltage feedback pin. Output current of this pin could controls the PWM duty cycle、OLP and SCP.
	8	GND	GND Pin

Ordering Information

DEVICE	DEVICE CODE
RS2051 Y Z	**Y** is package & Pin Assignments designator : NF : SOT-26 S : SOP-8 P : DIP-8 **Z** is Lead Free designator : P: Commercial Standard, Lead (Pb) Free and Phosphorous (P) Free Package

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter		Range	Units
V_{DD}	Supply voltage Pin Voltage		40	V
I_{OVP}	VDD OVP maximal enter current		20	mA
V_{FB}	Input Voltage to FB Pin		-0.3 to 6V	V
V_{SEN}	Input Voltage to SEN Pin		-0.3 to 6V	V
P_D	Power Dissipation		300	mW
ESD	ESD Capability, HBM Model		2500	V
	ESD Capability, Machine Model		250	V
T_{LEAD}	Lead Temperature (Soldering)	SOT-26 (20 second)	220	°C
		DIP-8 (10 second)	260	
		SOP-8 (10 second)	230	
T_{OPR}	Operating Temperature Range		-20 to +85	°C
T_{STG}	Storage Temperature Range		-55 to + 150	°C

Recommended Operation Condition

Symbol	Parameter	Range	Units
V_{DD}	VDD Supply Voltage	10 to 30	V
RI	RI Pin Resistor Value	100	KΩ
T_{OA}	Operation Ambient Temperature	-20 to 85	°C
P_O	Output Power	60	W
F_{PWM}	Frequency of PWM	30 to 150	KHz

Electrical Characteristics (V_{DD}=15V, T_A=25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD} Pin)						
I_{ST}	Startup Current	-	-	3.0	20.0	μA
I_{SS}	Operating Current	V_{FB}=0V	-	3.0	-	mA
		V_{FB}=3V	-	1.2	-	
		V_{FB}=Open	-	0.8	-	
VDD_{ON}	Turn-on Threshold Voltage	-	13.0	14.0	15.0	V
VDD_{OFF}	Turn-off Threshold Voltage	-	7.8	8.8	9.8	V
VD_{CLAMP}	VDD Clamp Voltage	I_{VDD}=20mA	-	34.0	-	V
VDD_{AIS}	Anti Intermission Surge VDD Voltage	-	-	9.4	-	V
Voltage Feedback (FB Pin)						
I_{FB}	Short Circuit Current	V_{FB}=0V	-	0.7	-	mA
V_{FB}	Open Loop Voltage	V_{FB}=Open	-	4.8	-	V
I_{FB_0D}	Zero Duty Cycle FB current	-	-	0.59	-	mA
I_{Burst}	Enter Burst & PWM, FB current	-	-	0.50	-	mA
I_{CRM}	Enter CRM, FB current	-	-	0.55	-	mA
V_{Burst}	Burst Threshold V_{FB}	-	-	1.80	-	V
V_{CRM}	Enter CRM Threshold V_{FB}	-	-	1.40	-	V
$I_{OLP\&SCP}$	Enter OLP&SCP FB current	-	-	170	-	uA
$V_{OLP\&SCP}$	Enter OLP&SCP FB voltage	-	-	3.7	-	V
$T_{OLP\&SCP}$	OLP&SCP min. delay Time	RI=100KΩ	33	35	50	ms
Current Sensing (SEN Pin)						
V_{TH_L}	Minimum Voltage Lever ($D_{MIN.}$= 0%)	-	-	0.80	-	V
V_{TH_H}	Maximum Voltage Lever ($D_{MAX.}$= 78%)	-	-	1.05	-	V
T_{PD}	Delay to Output	-	-	75	-	ns
R_{CS}	Input Impedance	-	-	40	-	KΩ
T_{LEB}	Leading edge blanking time	-	-	300	-	ns
Oscillator (RI Pin)						
F_{OSC}	Normal Frequency	RI=100KΩ	60	65	70	KHz
F_{Burst}	Burst Frequency	RI=100KΩ	-	22	-	KHZ
DC_{MAX_W}	Maximum Duty Cycle PWM	RI=100KΩ	-	78	-	%
DC_{MAX_F}	Maximum Duty Cycle Burst	RI=100KΩ	-	78	-	%
ΔF_{TEMP}	Frequency Temp. Stability	-30 to 100°C	-	5	-	%
T_{BLANK}	Leading-Edge Blanking Time	-	-	300	-	ns
$F_{JIGGLING}$	Frequency Jiggling	RI=100KΩ	-4	-	4	%
GATE Drive Output (GATE Pin)						
V_{OL}	Output Low Level	V_{DD}=16V, I_O=20mA	-	-	0.8	V
V_{OH}	Output High Level	V_{DD}=16V, I_O=20mA	10	-	-	V
T_{R1}	Rising Time	C_L=500pF	-	123	-	ns
T_{F1}	Falling Time	C_L=500pF	-	71	-	ns
T_{R2}	Rising Time	C_L=1000pF	-	248	-	ns
T_{F2}	Falling Time	C_L=1000pF	-	116	-	ns
T_{R3}	Rising Time	C_L=1500pF	-	343	-	ns
T_{F3}	Falling Time	C_L=1500pF	-	153	-	ns
T_{R4}	Rising Time	C_L=2000pF	-	508	-	ns
T_{F4}	Falling Time	C_L=2000pF	-	209	-	ns
VG_{CLAMP}	Output Clamp Voltage	VDD=20V	-	18.0	-	V
Frequency Jiggling						
f_{EMI}	Low EMI frequency	RI=100KΩ	-	65	-	KHz
Δf_osc	Frequency modulation range / Base frequency	RI=100KΩ	-3	-	3	%

Notice: The drive current of GATE pin is a variable value, which is decided by $I = K(V_{VDD} - V_{GATE} - 2.8)^2$ (Among these, K is a invariable coefficient，V_{GATE} is the voltage of GATE pin, V_{VDD} is the voltage of VDD pin)；So the higher the VDD voltage is and the lower the output voltage is, the bigger the drive transient current is. When the GATE voltage is 0V and the VDD voltage is 13V, the output drive current would over 120mA. The output driver current would decrease with increasing of the GATE voltage.

Detail Description

Current Mode

Compared to voltage mode control, current mode control has a current feedback loop. When the voltage of the Sense resistor peak current of the primary winding reaches the internal setting value V_{TH}, the register resets and the power MOSFET cuts off. So, to detect and modulate the peak current cycle-by-cycle could control the output of the power supply. The current feedback has a good linear modulation rate and a fast input and output dynamic impact, and avoid the pole that the output filter inductance brings and the two-class system descends to the one-class. So it widens the frequency range and optimizes overload protection and short circuit protection.

Startup Current and Under Voltage Lockout

The startup current of RS2051 is set to be very low so that a large value startup resistor can be used to minimize the power loss. For AC to DC adaptor with universal input range design, a 2mΩ, 1/8W startup resistor and a 10uF/25V VDD hold capacitor could be used.

The turn-on and turn-off threshold of the RS2051 is designed to 14V/8.8V. During startup, the hold-up capacitor must be charge to 14V through the startup resistor. The hysteresis is implemented to prevent the shutdown from the voltage dip during startup.

Internal Bias and OSC Operation

A resistor connected between RI pin and GND pin sets the internal constant current source to charge or discharge the internal fixed capacitor. The charge time and discharge time determines the internal clock speed and the switching frequency. Increasing the resistance will reduce the value of the input current and reduce the switching frequency. The relationship between RI and PWM switching frequency follows the below equation within the RI allowed range.

$$F_{OSC} = \frac{6500}{RI(K\Omega)}(kHz)$$

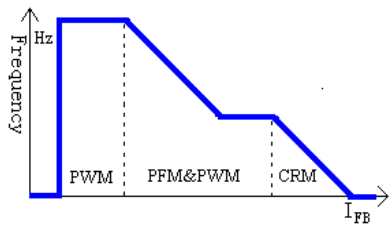
For example, a 100KΩ resistor RI could generate a 20uA constant current and a 65KHz PWM switching frequency. The suggested operating frequency range of RS2051 is within 50KHz to 150KHz.

Green Power Operation

The power dissipation of switching mode power supply is very important in zero load or light load condition. The major dissipation results from conduction loss、switching loss and consume of the control circuit. However, all of them relates to the switching frequency. There are many difference topologies has been implemented in different chip. The basic operation theory of all these approaches intends to reduce the switching frequency under light-load or no-load condition.

The RS2051's green power function adapts PWM、Burst and CRM combining modulation. When RI resistor is 100KΩ, the PWM frequency is 65KHz in medium or heavy load operation. Through modifying the pulse width, The RS2051 could control output voltage. The current of FB pin increases when the load is in light condition and the internal mode controller enters Burst&PWM when the feedback current is over 1.37mA. The operation frequency of oscillator is to descend gradually. When the feedback current is over 0.5mA, the frequency of oscillator is invariable, namely 22KHz.

To decrease the standby consumption of the power supply, Chip-Rail introduces the Cycle Reset Mode technology (CRM). If the feedback current is over 0.59mA, mode controller of the RS2051 would reset internal register all the time and cut off the GATE pin. While the output voltage is lower than the set value, the register would be set, the GATE pin operate again. So the frequency of the internal OSC is invariable, the register would reset some pulses so that the practical frequency is decreased at the GATE pin.

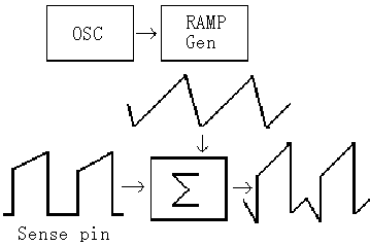


RS2051 Green-Power Function

Internal Synchronized Slope Compensation

Although there are more advantages of the current mode control than conventional voltage mode control, there are still several drawbacks of peak-sensing current-mode converter, especially the open loop instability when it operates in higher than 50% of the duty-cycle. To solve this problem, the RS2051 is introduced an internal slope compensation adding voltage ramp to the current sense input voltage for PWM generation. It improves the close loop stability greatly at CCM, prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

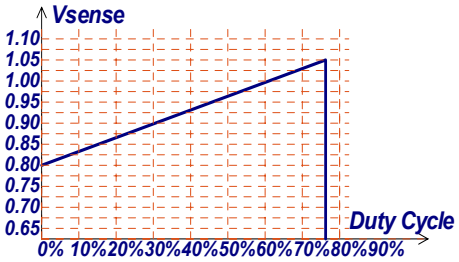
$$V_{SLOP} = 0.33 \times \frac{DUTY}{DUTY_{MAX}} = 0.4389 \times DUTY$$



Slope Compensation

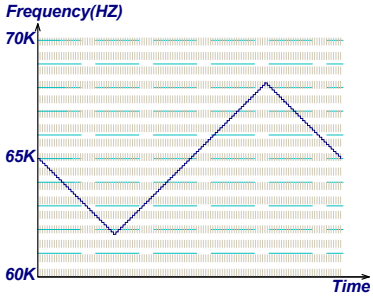
Current Sensing & Dynamic peak limiting

The current flowing by the power MOSFET comes into being a voltage V_{SENSE} on the Sense pin cycle-by-cycle, which compares to the internal reference voltage, and controls the reverse of the internal register, limits the peak current IMAX of the primary of the transformer. The transformer energy is $E = \frac{1}{2} \times L \times I_{MAX}^{2}$ So adjusting the R_{SENSE} can set the maximal output power of the power supple. The current flowing by the power MOSFET has an extra value ($\Delta I = \frac{V_{IN}}{L_P} \times T_D$) due to the system delay time that is from detecting the current through the Sense pin to power MOSFET off in the RS2051 (Among these, V_{IN} is the primary winding voltage of the transformer and L_P is the primary wind inductance). V_{IN} ranges from 85VAC to 264VAC. To guarantee the output power is a constant for universal input AC voltage, there is a dynamic peak limit circuit to compensate the system delay T that the system delay brings on.



Frequency Jiggling for EMI improvement

The Frequency Jiggling Technique is introduced in the RS2051. As following figure, the internal oscillation frequency is modulated by itself. A whole surge cycle includes 128 pulses and the Jiggling ranges from -4% to +4%. Thus, the function could minimize the electromagnetic interferer from the power supply module.



Frequency Jiggling to reduce EMI

OLP & SCP

To protect the circuit from being damaged under the over load or short circuit condition, a smart OLP&SCP function is implemented in the RS2051. When short circuit or over load occurs in the output end, the feedback cycle would enhance the voltage of FB pin, while the voltage is over 3.7V or the current from FB is below 170uA, the internal detective circuit would send a signal to shut down the GATE and pull down the VDD voltage, then the circuit is restart. To avoid the wrong operation when circuit starts, the delay time is set. When the RI resistance is 100Kohm, the delay time $T_{OLP\&SCP}$ is between 33ms and 50ms. The relationship between RI and $T_{OLP\&SCP}$ follows the below equation.

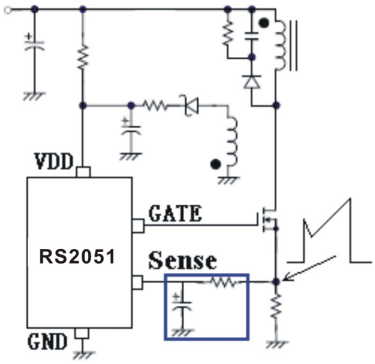
$$\frac{RI\times 2}{6\times 10^3}(ms) < T_{OLP\&SCP} < \frac{RI\times 3}{6\times 10^3}(ms)$$

Anti Intermission Surge

When the power supplies change the heavy load to light load immediately, there could be tow phenomena caused by system delay. They are output voltage overshot and intermission surge. To avoid it, the anti intermission surge is built in the RS2051. If it occurs, the FB current is to increase rapidly, the GATE would be cut off for a while, VDD pin voltage descends gradually. When VDD reaches 9.4V, the GATE pin would operate again, which the frequency is 22KHz.

Leading-edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the Sense pin, which would disturb the internal signal from the sampling of the R_{SENSE}. There is a 300ns leading edge blanking time built in to avoid the effect of the turn-on spike, and the power MOSFET cannot be switched off during the moment. So that the conventional external RC filtering on sense input is no longer required.



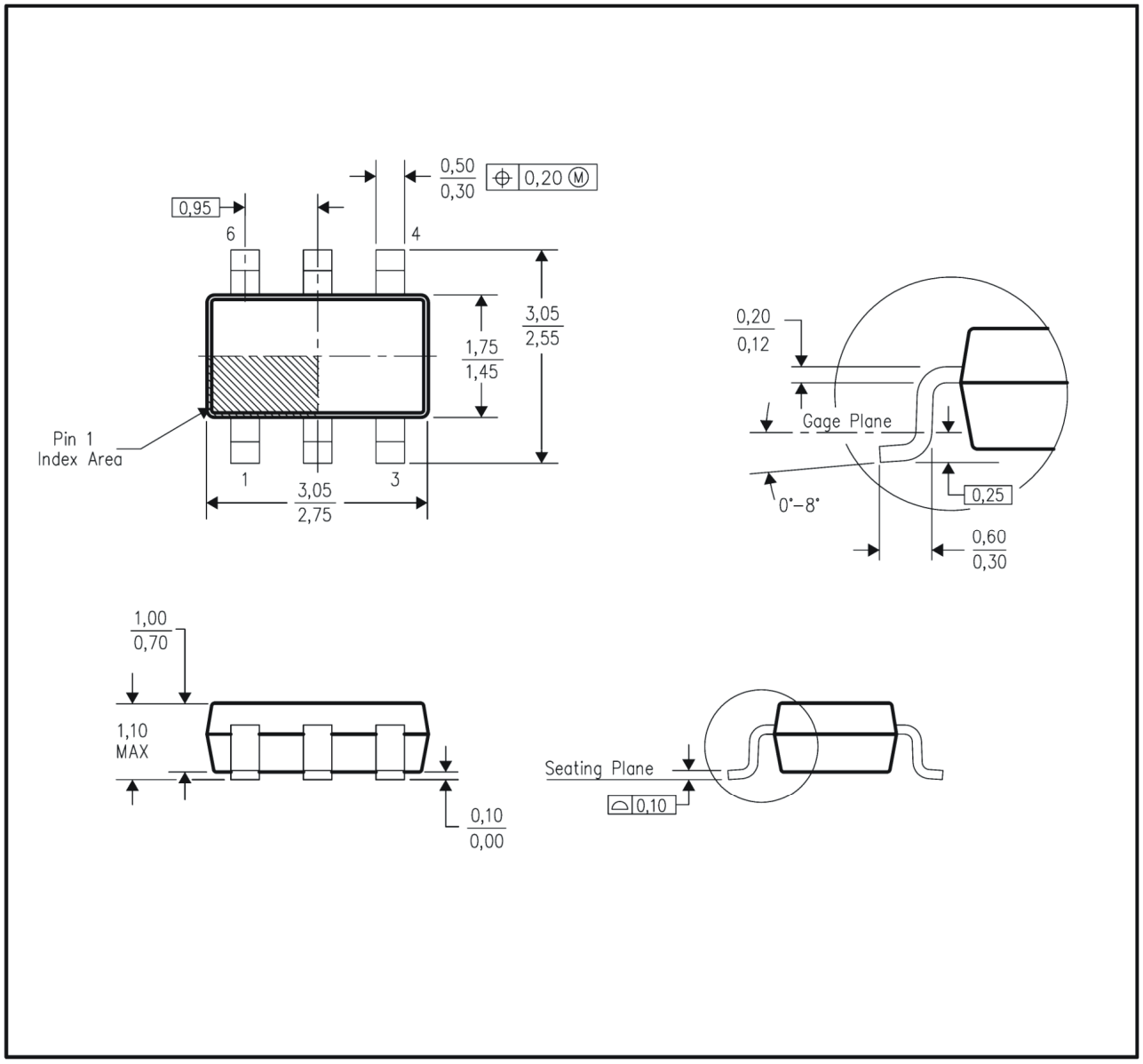
OVP

There is a 25.6V over-voltage protection circuit in the RS2051 to improve the credibility and extend the life of the chip. When the VDD voltage is over 25.6V, the GATE pin is to shutdown immediately and the VDD voltage is to descend rapidly.

GATE Driver & Soft Clamped

The RS2051 output designs a totem pole to drive a periphery power MOSFET. The dead time is introduced to minimize the transfixion current during the output operating. The novel soft clamp technology is introduced to protect the periphery power MOSFET from breaking down and current saturation of the Zener.

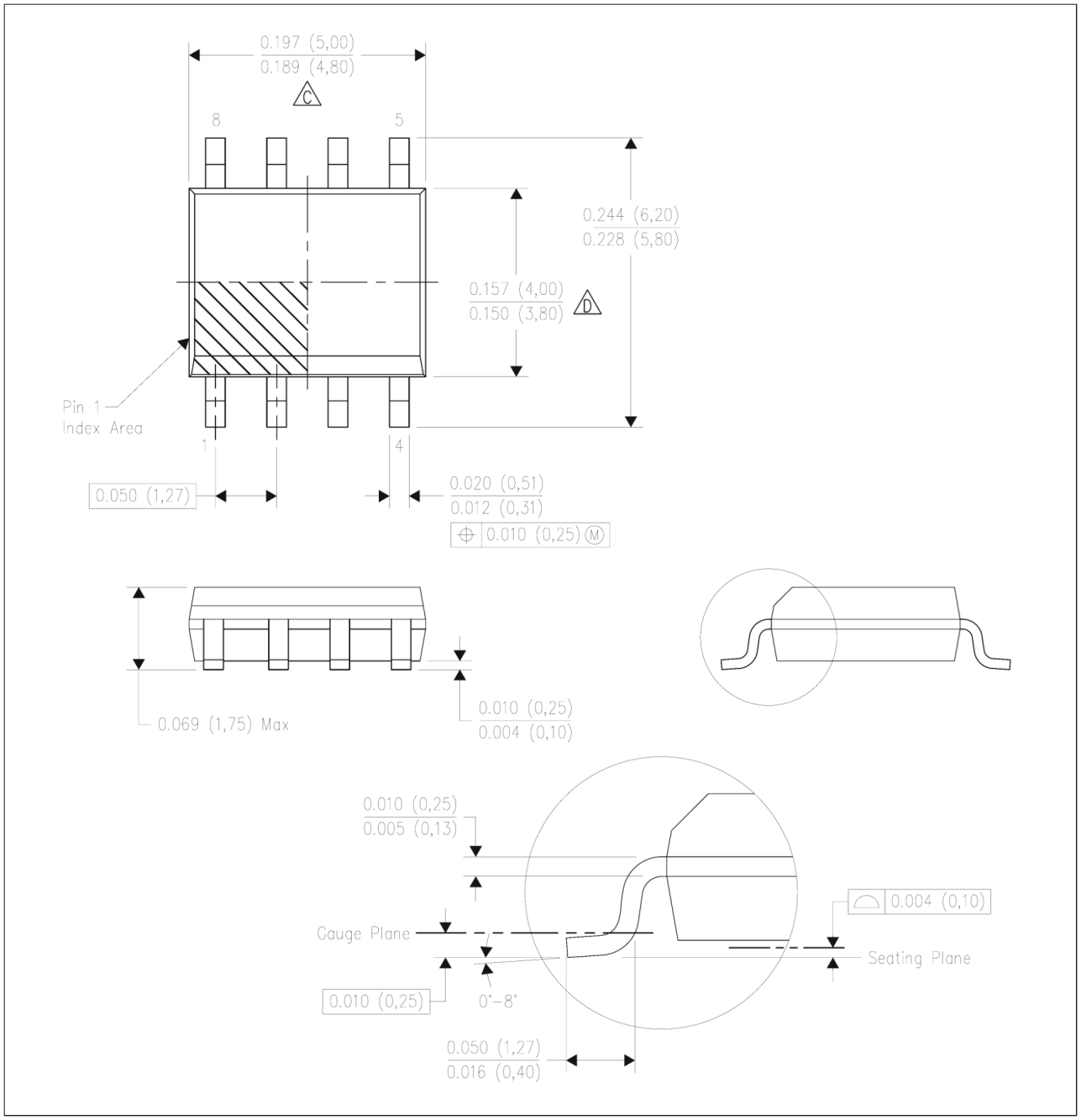
SOT-26 Dimension



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
E. Falls within JEDEC MO-178 variation AB, except minimum lead width.

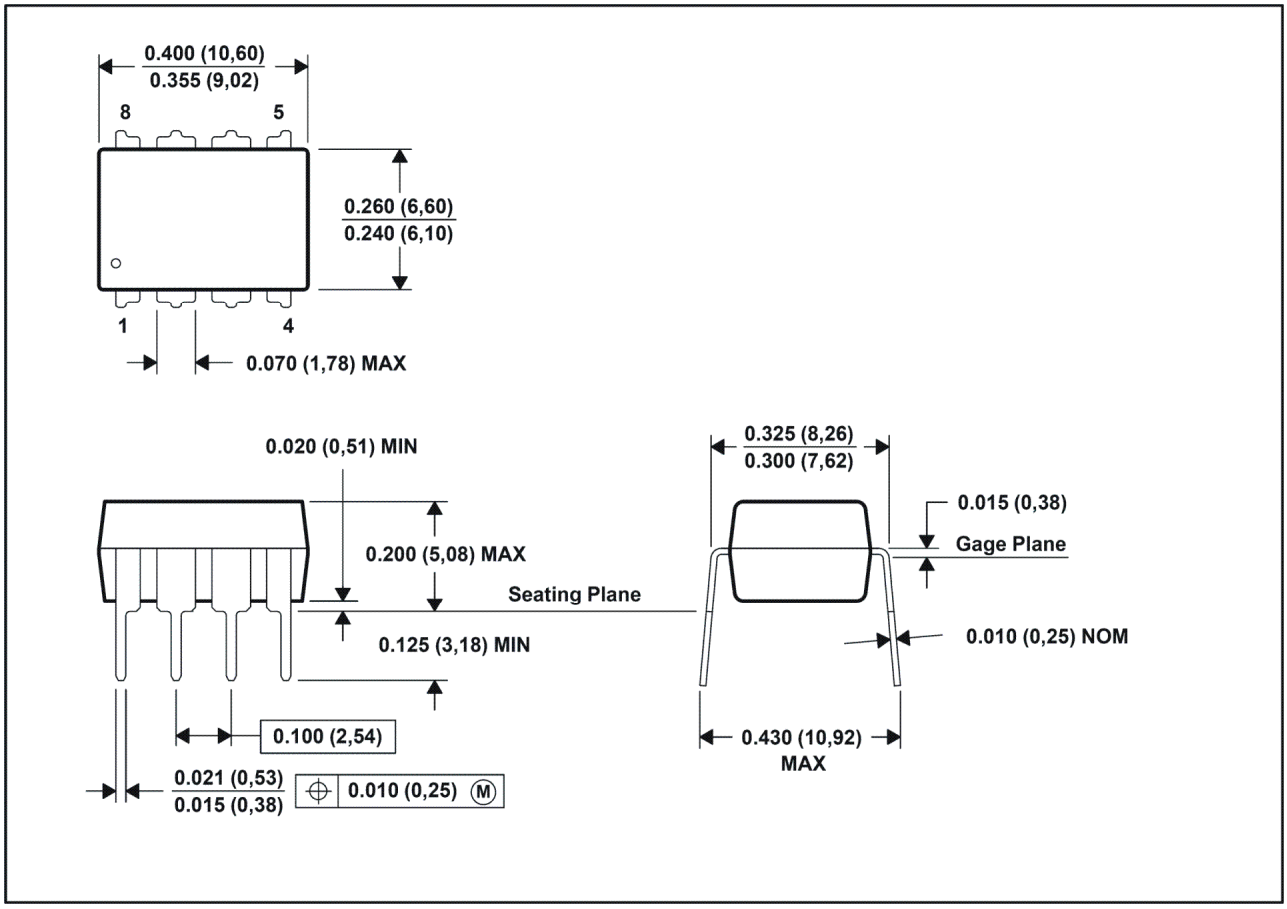
SOP-8 Dimension



NOTES:

A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) per side.
E. Falls within JEDEC MS-012 variation AA.

DIP-8 Dimension



NOTES:

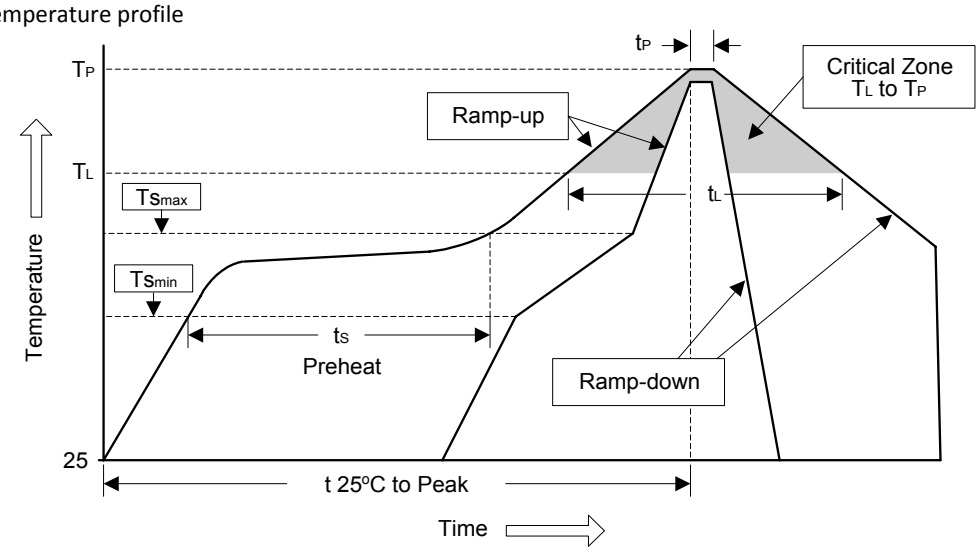
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001.

Soldering Methods for Orister's Products

1. Storage environment: Temperature=10°C~35°C Humidity=65%±15%

2. Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (min to max) (ts)	 100°C 150°C 60~120 sec	 150°C 200°C 60~180 sec
Tsmax to T_L - Ramp-up Rate	 <3°C/sec	 <3°C/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60~150 sec	 217°C 60~150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak temperature	Dipping time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

Important Notice: