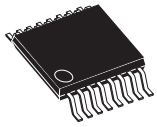
STLVDS105

4-port LVDS and 4-port TTL-to LVDS repeaters

General feature

- Receiver and drivers meet or exceed the requirements of ansi EIA/TIA-644 standard: receivers low-voltage TTL (LVTTL) levels designed for signaling rates up to 630Mbps
- Operates from a single 3.3V supply
- Low voltage differential signaling with typical output voltage of 350mV and a 100Ω load
- Propagation delay time: 2.2ns (typ)
- Electrically compatible with LVDS, PECL, LVPECL, LVTTL, LVCOMOS, GTL, BTL, CTT, SSTL, or HSTL outputs with external network
- Bus terminal ESD (HBM) exceeds 7kV
- TSSOP package



TSSOP

Description

The STLVDS105 is a differential line receiver and a LVTTL input connected to four differential line drivers that implement the electrical characteristics of low voltage differential signaling, for point to point baseband data transmission over controlled impedance media of approximately 100W. The transmission media can be printed-circuit board traces, backplanes, or cable.

LVDS, as specified in EIA/TIA-644 is a data signaling technique that offers low-power, low noise coupling, and switching speed to transmit data at a speed up to 630Mbps at relatively long distances.

The drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allow extremely precise timing alignment of the signals repeated from the input.

The device allows extremely precise timing alignment of the signal repeated from the input. This is particularly advantageous in distribution or expansion of signals such as clock or serial data stream.

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Order code

Part number	Temperature range	Package	Comments
STLVDS105BTR	-40 to 85 °C	TSSOP16 (Tape & Reel)	2500 parts per reel

Contents

1 Pin configuration

Figure 1. Pin connections and functional diagram

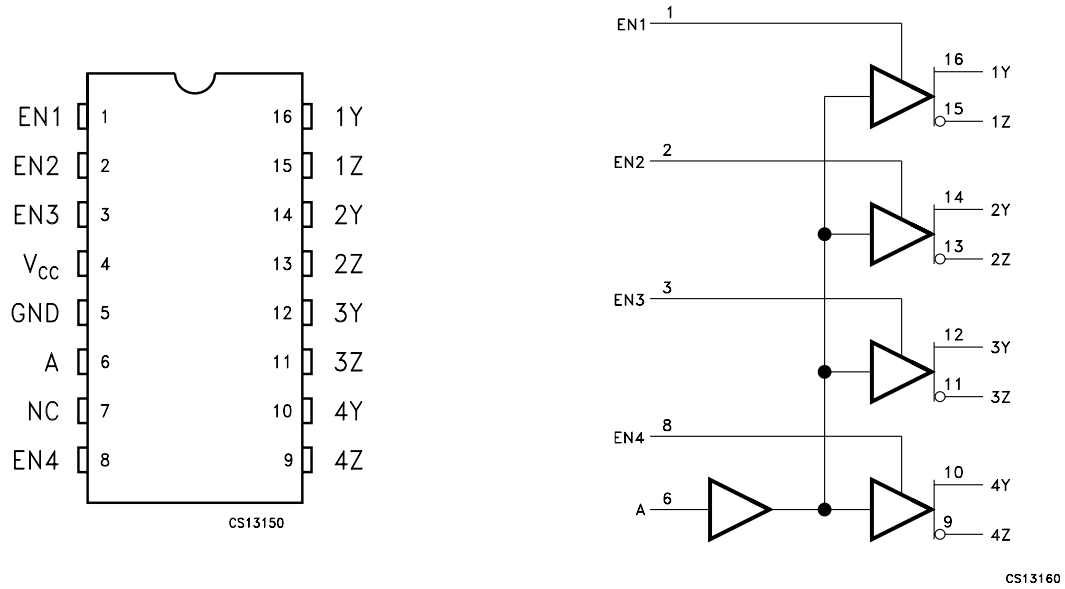


Table 1. Pin description

Pin n°	Symbol	Name and function
1, 2, 3, 8	EN1 to EN4	Enable driver inputs
6	A	Receiver input
7	NC	Not connected
9, 11, 13, 15	1Z to 4Z	Driver inputs
10, 12, 14, 16	1X to 4X	Driver inputs
5	GND	Ground
4	V_{CC}	Supply voltage

Table 2. Functional table

Input	Enables	Outputs	
A	**#EN**	**#Y**	**#Z**
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z
X	X	Z	Z

L=Low level, H=High level, X=Don't care, Z= High impedance

2 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (Note 1)		-0.5 to 4	V
V_R	Voltage range	Enable inputs	-0.5 to 6	V
		A, Y or Z	-0.5 to 4	V
ESD	ESD Protection voltage (HBM)	Y, Z, to GND	7	KV
		All Pins	2	KV
T_{stg}	Storage temperature range		-65 to +150	°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Note: 1 All voltages except differential I/O bus voltage, are with respect to the network ground terminal.

Table 4. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	HIGH level input voltage	2.0			V
V_{IL}	LOW level input voltage			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	0.1		3.6	V
V_{IC}	Common mode input voltage	$\|V_{ID}\|/2$		$24-\|V_{ID}\|/2$	V
				$V_{CC}-0.8$	
T_A	Operating temperature range	-40		85	°C

3 Electrical characteristics

Table 5. Electrical characteristics
(T_A = -40 to 85°C, and V_{CC} = 3.3V ±10% over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100Ω, V_{ID} = ±100mV	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic state		-50		50	mV
$\Delta V_{OC(SS)}$	Change in steady-state common mode output voltage between logic state		-50		50	mV
$V_{OC(SS)}$	Steady-state Common Mode Output Voltage		1.125	1.2	1.375	V
$V_{OC(PP)}$	Peak to peak common mode output voltage			25	150	mV
I_{CC}	Supply current	Enabled, R_L = 100Ω		18	28	mA
		Disabled		0.3	1	mA
I_{IH}	High level input current	V_{IH} = 2V		7	20	µA
I_{IL}	Low level input current	V_{IL} = 0.8V		3	10	µA
I_{OC}	Short circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0V			± 10	mA
		V_{OD} = 0			± 10	mA
I_{OZ}	High Impedance output current	V_O = 0 or 2.4V			± 1	µA
$I_{O(OFF)}$	Power OFF output current	V_{CC} = 1.5V, V_O = 2.4V		0.3	± 1	µA
C_{IN}	Input capacitance (A or B inputs)	V_I = 0.4 sin ($4e^{6\pi t}$)+0.5V		5		pF
C_O	Output capacitance (Y or Z outputs)	V_I = 0.4 sin ($4e^{6\pi t}$)+0.5V, Disabled		9.4		pF

Table 6. Switching characteristics

(T_A = -40 to 85°C, and V_{CC} = 3.3V unless otherwise noted. All typical values are at T_A = 25°C).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time, low to high output	R_L = 100Ω C_L = 10pF	1.7	2.2	3	ns
t_{PHL}	Propagation delay time, high to low output		1.7	2.2	3	ns
t_r	Differential output signal rise time		0.3	0.7	1.2	ns
t_f	Differential output signal fall time		0.3	0.7	1.2	ns
$t_{sk(P)}$	Pulse skew ($\|t_{THL} - t_{TLH}\|$)			50	200	ps
$t_{sk(O)}$	Channel-to-channel output skew (1)			30	100	ps
$t_{sk(pp)}$	Part to part skew (2)				1.5	ns
t_{PZH}	Propagation delay time, high impedance to high level output			5	15	ns
t_{PZL}	Propagation delay time, high impedance to low level output			5	15	ns
t_{PHZ}	Propagation delay time, high level to high impedance output			4	15	ns
t_{PLZ}	Propagation delay time, low level to high impedance output			5	15	ns

1. $t_{sk(O)}$ is the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all their inputs connected together
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuit

4 Typical performance characteristics

(Unless otherwise specified T_J = 25°C)

Figure 2. Output current vs output high voltage

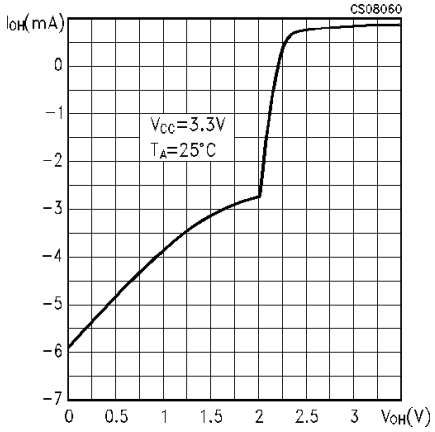


Figure 3. Output current vs output low voltages

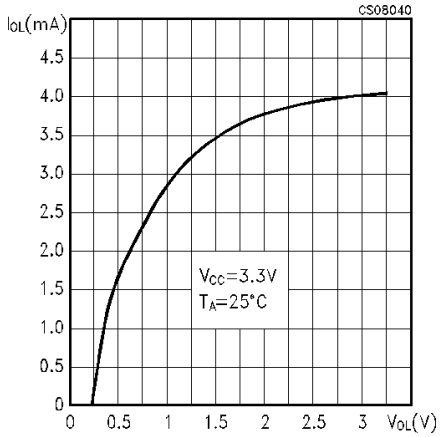


Figure 4. High to low propagation delay time

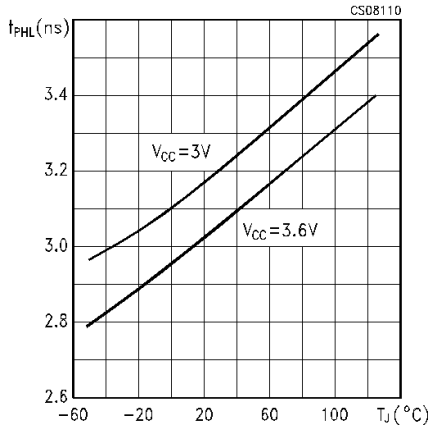
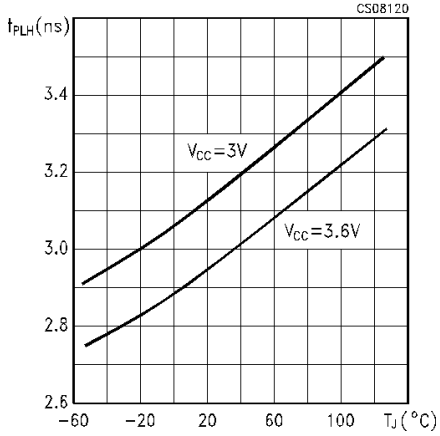


Figure 5. Low to high propagation delay time r

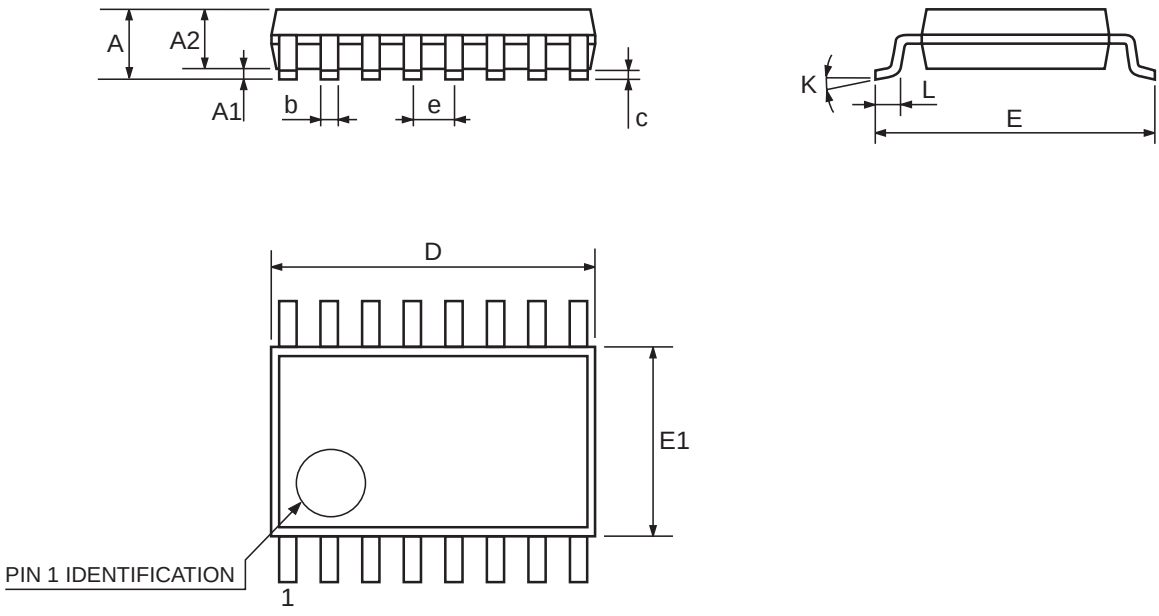


5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

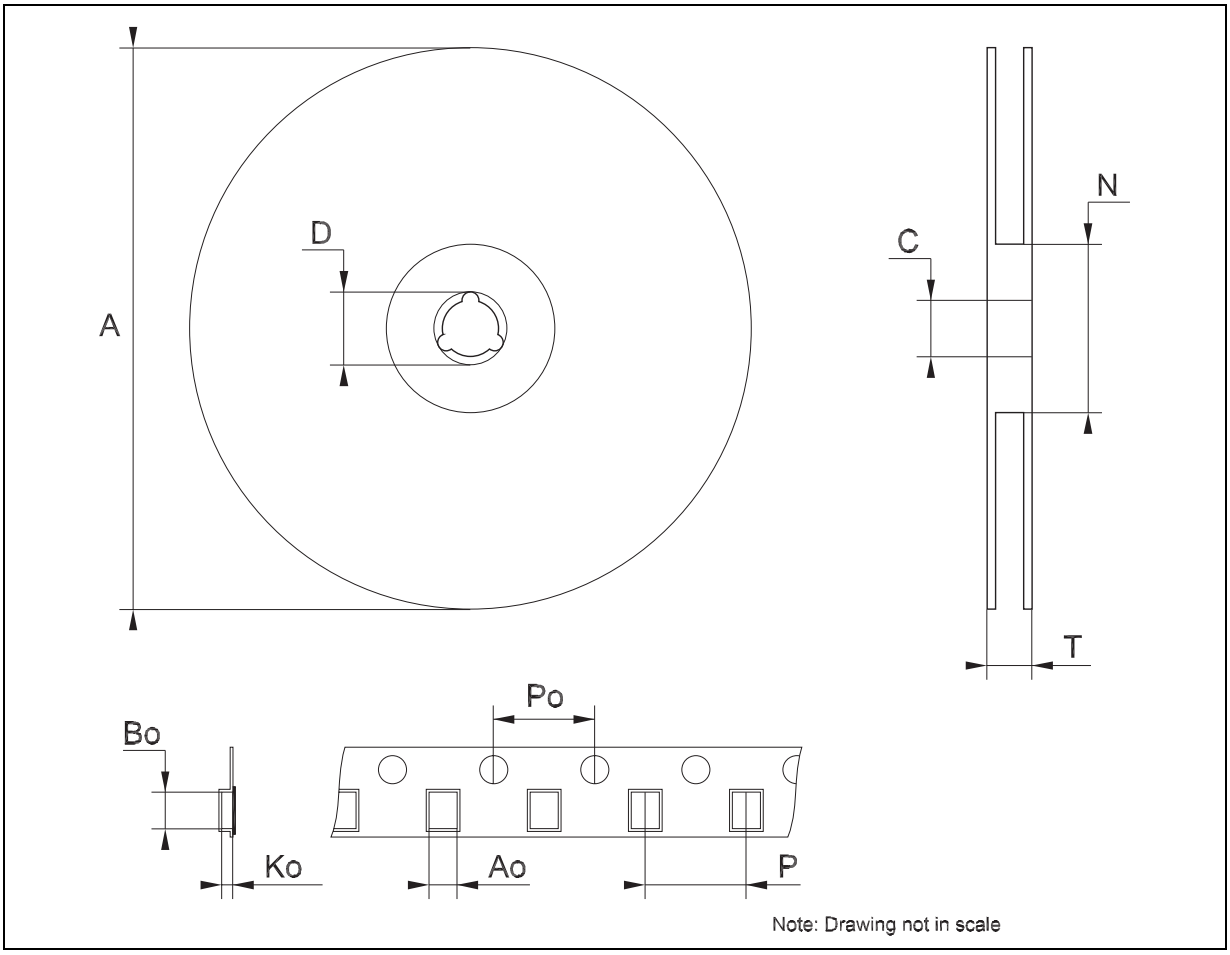
TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

6 Revision history

Table 7. Revision history

Date	Revision	Changes
22-Mar-2006	4	Order codes has been updated and new template.

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