SC4809A/B/C
High Performance Current Mode PWM Controller

Description

The SC4809A/B/C is a 10 pin BICMOS primary side current mode controller for use in Isolated DC-DC and off-line switching power supplies. It is a highly integrated solution, requiring few external components. It features a high frequency of operation, accurately programmable maximum duty cycle, current mode control, line voltage monitoring, supply UVLO, low start-up current, and programmable soft start with user accessible reference. It operates in a fixed frequency, highly desirable for Telecom applications. Features a separate sync pin which simplifies synchronization to an external clock. Feeding the oscillator of one device to the sync of another forces biphase operation which reduces input ripple and filter size.

The SC4809A/B/C have different threshold and VREF to accommodate a wide variety of applications.

These devices are available in the MSOP–10 lead free package.

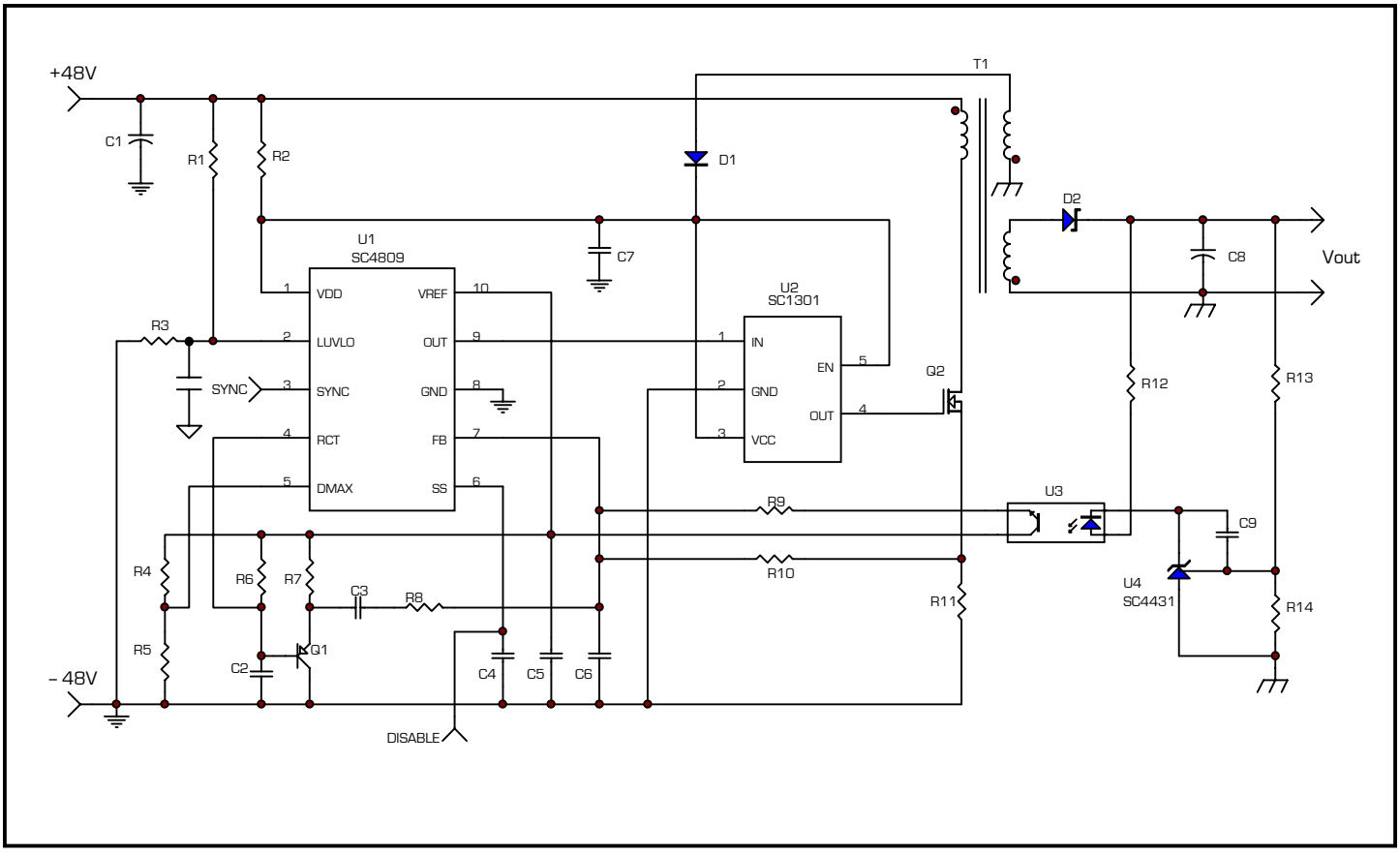
Features

- Operation to 1MHz
- Accurate programmable maximum duty cycle
- Line voltage monitoring
- External frequency synchronization
- **Bi-phase mode of operation for low ripple**
- Under 100µA start-up current
- Accessible reference voltage
- VDD undervoltage lockout
- -40°C to 105°C operating temperature
- 10 lead MSOP package. Lead free package available. Fully WEEE and RoHS compliant

Applications

- Telecom equipment and power supplies
- Networking power supplies
- Power over LAN applications
- Industrial power supplies
- Isolated power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage	V_{DD}	19	V
Supply Current	I_{DD}	25	mA
SS, UVLO, DMAX, RCT		-0.3V to V_{REF} + 0.3V	V
Current VREF	I_{REF}	15	mA
Current LUVLO	I_{LUVLO}	-1	mA
Storage Temperature Range	T_{STG}	-65 to +150	°C
Junction Temperature	T_J	-40 to +150	°C
Thermal Resistance	θ_{JA}	113	°C/W
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	+300	°C
ESD Rating (Human body model)	ESD	2	kV

Electrical Characteristics

Unless specified: V_{DD} = 12V, C_{SS} =1nF, F_{OSC} = 500kHz, R_T = 10K, C_T = 100pF, D_{MAX} = 2V, $T_A = T_J$ = -40°C to +105°C.

Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Section					
VDD Clamp	B version	16	17.5	19	V
I_{DD}			1.5	2.5	mA
I_{DD} Starting				110	µA
UVLO Section (A version)					
Start Threshold		4.35		4.5	V
Hysteresis				0.3	V
UVLO Section (B version)					
Start Threshold		11		12	V
Hysteresis				4	V
UVLO Section (C version)					
Start Threshold		6.55		6.95	V
Hysteresis				0.75	V
VREF Section					
VREF (A version)	0 - 5mA	-3%	4	+3%	V
VREF (B, C version)	0 - 5mA	-3%	5	+3%	V

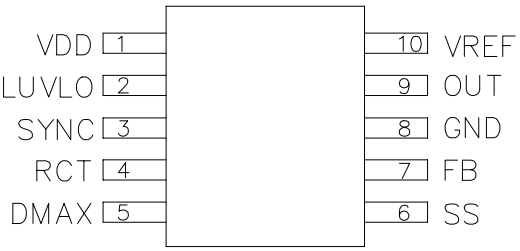
Electrical Characteristics (Cont.)

Unless specified: V_{DD} = 12V, C_{SS} =1nF, F_{OSC} = 500kHz, R_T = 10K, C_T = 100pF, D_{MAX} = 2V, $T_A = T_J$ = -40°C to +105°C.

Parameter	Test Conditions	Min	Typ	Max	Unit
Line Under Voltage Lockout					
Start Threshold	R_A = 61.9k, R_B = 10k	-3%	3	-3%	V
Hysteresis	R_A = 61.9k, R_B = 10k		150		mV
Input Bias Current	LUVLO = 3.2V		-100	-250	nA
Comparator Section					
IFB	Output Off		-100		nA
Comparator Threshold (A, B version)		570	600	630	mV
Comparator Threshold (C version)		950	1000	1050	mV
OUT Propagation Delay (No Load)	V_{FB} = 0.8V to 1.2V at T_R = 10ns		75	100	ns
Soft Start Section					
I_{SS}	V_{SS} = 0V; -40 °C <T_a +105°C	-2		-8.0	µA
Shutdown Threshold (A, B version)		300	340		mV
Shutdown Threshold (C version)		440	500		mV
Oscillator Section					
Frequency range		50		1100	kHz
RCT Peak Voltage			3.00		V
RCT Valley Voltage			0.05		V
Minimum Duty Cycle Pulse Width	V_{FB} = 2V		50		ns
Maximum Duty Cycle			90		%
Sync/CLOCK					
Clock SYNC Threshold	Positive Edge Triggered		2.1		V
Minimum Sync Input Pulse Width	F_{SYNC} > Fosc			50	ns
Output Section					
Output VSAT Low	I_{OUT} = 1mA			500	mV
Output VSAT High	I_{OUT} = 1mA	V_{REF} - 0.5			V
Rise Time	C_{OUT} = 20pF		10	25	ns
Fall Time	C_{OUT} = 20pF		10	25	ns

Pin Configuration

Top View



MSOP-10

Ordering Information

Part Number	Package[1]	Temp. Range (T_J)
SC4809AIMSTR	MSOP-10	-40°C to +150°C
SC4809AIMSTRT[2]		
SC4809BIMSTR		
SC4809BIMSTRT[2]		
SC4809CIMSTR		
SC4809CIMSTRT[2]		

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

FB: This pin is the summing node for current sense feedback, voltage sense feedback (by optocoupler) and slope compensation. Slope compensation is derived from the rising voltage at the time capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250Ω on-resistance NMOS FET during PWM off -time and offers effective leading edge blanking set by the RC time constant of the feedback resistance from the current sense resistor to the FB input and the high frequency filter capacitor capacitance at this node to GND.

GND: Reference ground and power ground for all functions.

OUT: This pin is the logic level drive output to the external MOSFET driver circuit (similar to SC1301).

VREF: The internal 4V (A) / 5V (B & C) reference output. This reference is buffered and is available on the VREF pin. VREF should be bypassed with a 0.47 - 1.0µF ceramic capacitor.

RCT: The oscillator frequency is configured by connecting resistor RT from VREF to RCT and capacitor CT from RCT to ground. Using the equation below values for RT and CT can be selected to provide the desired OUT frequency.

$$F = \frac{1}{-\left[RT \bullet CT \bullet \ln\left(1 - \frac{V_{P-K}}{V_{REF}}\right)\right]}$$

where V_{P-K} = RCT peak voltage

DMAX: Duty cycle up to 98% can be programmed via R4 and R5 (the resistor divider from Vref in the Application Circuit). When DMAX pin is taken above 3V, 100% duty cycle is achieved.

SS: This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 8µA current source. Under normal soft start SS is discharged to less than 1V and then ramps positive to 1V during which time the output driver is held low. As SS charges from 1V to 2V, soft start is implemented by an increasing output duty cycle. If SS is taken below shutdown threshold, the output driver is inhibited and held low. The user accessible voltage reference also goes low and IDD < 100µA.

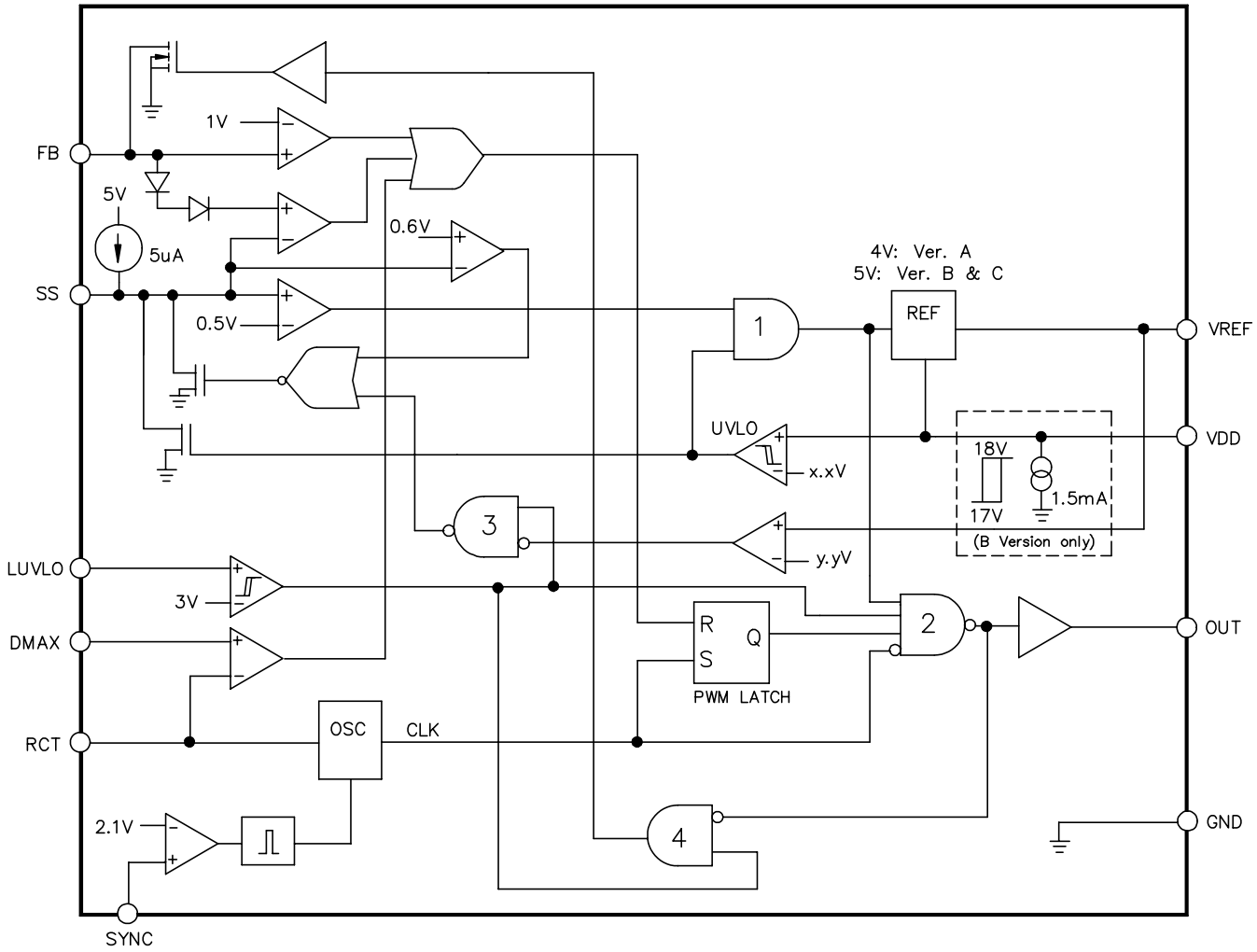
VDD: The power input connection for this device. This pin is shunt regulated at 17.5V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1µF ceramic capacitor.

LUVLO: Line undervoltage lock out pin. An external resistive divider will program the undervoltage lock out level. During the LUVLO, the Driver outputs are disabled and the softstart is reset.

SYNC: SYNC is a positive edge triggered input with a threshold set to 2.1V. In the Bi-Phase operation mode the SYNC pin should be connected to the CT (Timing Capacitor) of the second controller. This will force a out of phase operation. In a single controller operation, SYNC could be grounded or connected to an external synchronization clock with a frequency higher than the on-board oscillator frequency. The external OSC frequency should be 30% greater for guaranteed SYNC operation.

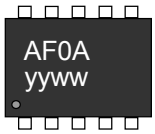
POWER MANAGEMENT

Block Diagram



Marking Information

Top Mark



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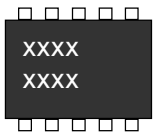

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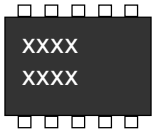

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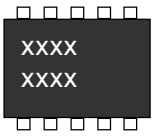
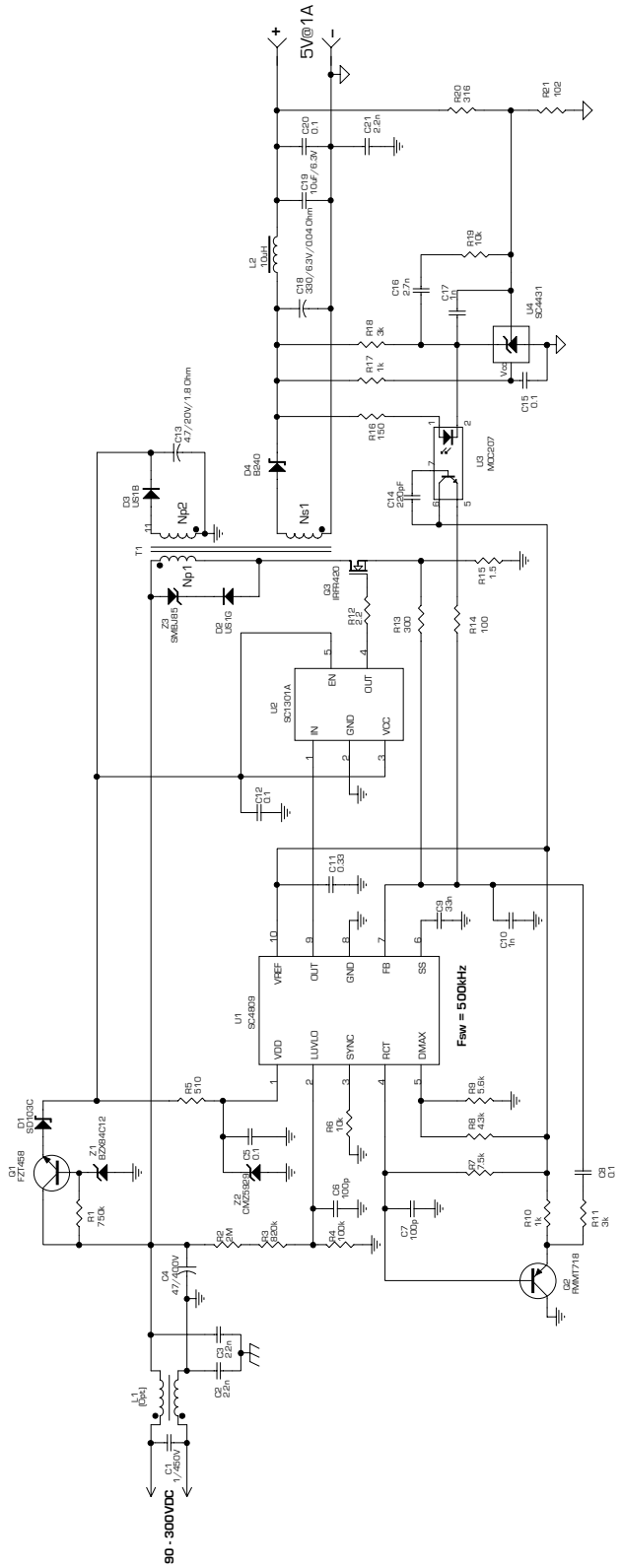


Part Number (Example: 1456)
yyww = Datecode (Example: 0012)
xxxxx = Semtech Lot # (Example: E901
xxxxx = 01-1)

Applications Information

Flyback, 90V - 300V to 5V @ 1A typ.



CRITICAL COMPONENTS:

Q3: IRFR420, Dpak, Inter.Rect.
B240, SMB, Vishay
C17: 6TPB330M, "7343", Sanyo
L2: TOKO, A920CY-100M or similar
U1: SC4809AIMSTR, MSOP-10, SEMTECH
U2: SC1301AISKTR, SOT-23-5, SEMTECH
U4: SC4431CSK, SOT-23-5, SEMTECH

T1

Core: EFD15, 3C85
Magnetizing L = 230uH
Np1 = 24 ts
Np2 = 5 ts
Ns1 = 2 ts
Approximate Gap = 0.038mm
AL value = 397 nH/N²

Application Information

The flyback power stage is very popular in 48V input telecom applications for output power levels up to approximately 50 watts. The exact power rating of the flyback power stage, of course, is dependent on the input voltage/output voltage combination, its operating environment and many other factors. Additional output voltages can be generated easily by simply adding another winding to the coupled inductor along with an output diode and output capacitor. Obtaining multiple output voltages from a single power stage is another advantage of the flyback power stage.

A simplified schematic of the flyback power stage with a drive circuit block included is shown in Figure 1. In the schematic shown, the secondary winding of the coupled inductor is connected to produce output voltage. The power switch, Q1, is an N-channel MOSFET. The secondary inductance, L_{SEC} and capacitor C, make up the output filter, The resistor R, represents the load seen by the power supply output.

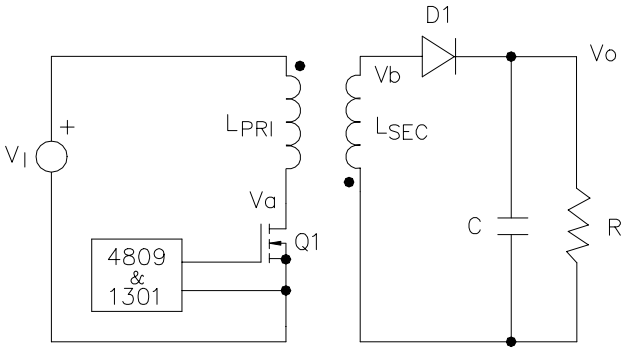


Figure 1: Flyback Power Converter

The important waveforms of the flyback power stage operating in DCM are shown in Figure 2.

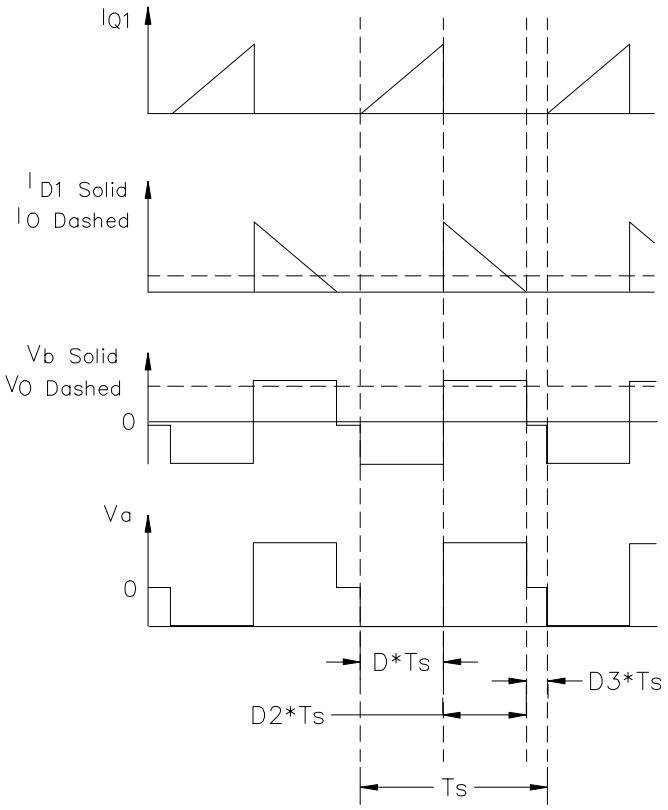


Figure 2: Discontinuous Mode Flyback Waveforms

The simplified voltage conversion relationship for the flyback power stage operating in CCM is given by:

$$V_O = V_I \bullet \frac{N_S}{N_P} \bullet \frac{D}{1-D}$$

The simplified voltage conversion relationship for the flyback power stage operating in DCM is given by:

$$V_O = V_I \bullet \frac{N_S}{N_P} \bullet \frac{D}{\sqrt{K}}$$

Where K is defined as:

$$K = \frac{2 \bullet L_{SEC}}{R \bullet T_S}$$

Application Information (Cont.)

Control-to-Output transfer function for the flyback power stage operating in CCM is given by:

$$\frac{dV_O}{dD} = \frac{V_I}{(1-D)^2} \bullet \frac{N_S}{N_P} \bullet \frac{\left(1+\frac{S}{\omega_{z1}}\right) \bullet \left(1-\frac{S}{\omega_{z2}}\right)}{1+\frac{S}{\omega_O \bullet Q}+\frac{S^2}{\omega_O{}^2}}$$

where:

$$\omega z1 = \frac{1}{R_C \bullet C}$$

$$\omega_{z2} \approx \frac{(1-D)^2 \bullet R}{D \bullet L_{SEC}}$$

$$\omega_O \approx \frac{1-D}{\sqrt{L_{SEC} \bullet C}}$$

$$Q \approx \frac{(1-D) \text{ x } R}{\sqrt{\frac{L_{SEC}}{C}}}$$

Control-to Output transfer function for the flyback power stage operating in DCM is given by:

$$\frac{dV_O}{dD} = V_I \bullet \frac{N_S}{N_P} \bullet \sqrt{\frac{R \bullet T_S}{2 \bullet L_{SEC}}} \bullet \frac{1}{1+\frac{S}{\omega_P}}$$

where:

$$\omega_P = \frac{2}{R \bullet C}$$

Peak current mode control requires simpler compensation, has pulse-by-pulse current limiting, and has better load current regulation. Primary and secondary RMS currents can be up to two times higher for discontinuous mode than for CCM. Discontinuous conduction mode would require using a transistor with a higher current rating. Because the output ripple current is less than it would be continuous mode were used, the output capacitors are smaller. Continuous conduction mode (CCM) was therefore chosen.

The DC transfer function of a CCM flyback converter is:

$$\frac{V_O + V_D}{V_{IN(min)} - V_{Rds(on)}} = \frac{1}{N} \bullet \left(\frac{D_{max}}{1-D_{max}}\right)$$

where V_O = output voltage,

V_D = forward voltage drop across rectifier D1,

N = turns ratio, equal to N_P/N_S,

D = duty cycle.

Transformer Design

The transformer in a flyback converter is actually a coupled inductor with multiple windings. Transformers provide coupling and isolation whereas inductors provide energy storage. The energy stored in the air gap of the inductor is equal to:

$$E = \frac{L_P \bullet (I_{PEAK})^2}{2}$$

where E is in Joules, L_P is the primary inductance in Henries, and I_{PEAK} is the primary peak current in Amperes. When the switch is on, D1 is reverse biased due to the dot configuration of the transformer. No current flows in the secondary windings and the current in the primary winding ramps up at a rate of:

$$\frac{\Delta I_L}{\Delta t} = \frac{V_{IN(min)} - V_{Rds(on)}}{L_P}$$

The output capacitor, C_{OUT}, supplies all of the load current at this time. Because the converter is operating in the continuous conduction mode, ΔI_L is the change in the inductor current which appears as a positive slope ramp on a step. The step is present because there is still current left in the secondary windings when the primary turns on. When the switch turns off, current flows through the secondary winding and D1 as a negative ramp on a step, replenishing C_{OUT} and supplying current directly to the load.

Application Information (Cont.)

The primary inductance can be calculated given an acceptable current ripple, ΔI_L. ΔI_L was set to equal one-half the peak primary current. For a CCM flyback design, the peak primary current is calculated:

$$I_{PEAK} = \left(\frac{I_{OUT(max)}}{N}\right) \bullet \left(\frac{1}{1-D_{max}}\right) + \frac{\Delta I_L}{2}$$

Because the converter is operating in the continuous mode, the maximum peak flux density B_{MAX}, is limited by the saturation flux density, B_{SAT}. Taking all this into consideration, the maximum core size is determined by.

$$AP = \left(\frac{L_P \bullet I_{PEAK} \bullet I_{RMS} \bullet 10^4}{420 \bullet k \bullet B_{MAX}}\right)^{1.31}$$

where AP = the core area product in cm^4,
k = winding factor,
$B_{MAX} \approx B_{SAT}$,

The result is compared to the product of the winding area, Aw (cm^2), and effective core area, Ae (cm^2), listed in the core manufacturer's data sheet.

The minimum number of primary turns is determined by:

$$N_P = \frac{L_P \bullet I_{PEAK} \bullet 10^4}{B_{MAX} \bullet Ae}$$

Based upon this result and the predetermined turns ratio, the number of secondary turns is established.

The energy stored in the flyback transformer is actually stored in an air gap in the core. This is because the high permeability of the ferrite material can't store much energy without saturating first. By adding an air gap, the hysteresis curve of the magnetic material is actually tilted, requiring a much higher field strength to saturate the core. The length of the air gap is calculated by:

$$\ell_g = \frac{\mu_o \bullet \mu_r \bullet (N_P)^2 \bullet Ae \bullet 10^{-2}}{L_P}$$

MOSFET Selection

The switching element in a flyback converter must have a voltage rating high enough to handle the maximum input voltage and the reflected secondary voltage, not to mention any leakage inductance induced spike that is inevitably present. Approximate the required voltage rating of the MOSFET using.

$$V_{ds} = \left[\left(V_{IN(max)} + V_L\right) + \left(\frac{N_P}{N_S}\right) \bullet \left(V_O + V_D\right)\right] \bullet 1.3$$

where V_{ds} = the required drain to source voltage rating of the MOSFET,

V_L = the voltage spike due to the leakage inductance of the transformer, estimated to be thirty percent of $V_{IN(MAX)}$, and the additions 1.3 factor includes an overall thirty percent margin.

This FET will experience both switching and conduction losses. The conduction losses will be equal to the I^2R losses, as shown by:

$$P_{COND} = (I_{RMS})^2 \bullet R_{DS(ON)}$$

Switching losses are the result of overlapping drain current and drain to source voltage at turn on and turn off.

The total switching losses are estimated based on equation:

$$P_{SW} = \frac{C_{OSS} \bullet (V_{DS})^2 \bullet f_{SW}}{2} + V_{DS} \bullet I_{PEAK} \bullet t_{ch} \bullet f_{sw}$$

where t_{ch}:

$$t_{CH} = \frac{Q_{gd} \bullet R_g}{VDD - V_{gs(th)}}$$

Diode Selection

Schottky rectifiers have a lower forward voltage drop than typical PN devices, making it the rectifier of choice when considering reducing converter losses and improving overall efficiency. Selecting the appropriate Schottky for a specific application depends mainly on the working peak reverse voltage rating and peak repetitive forward current.

Application Information (Cont.)

Input and Output Capacitors

The input capacitors are chosen based upon their ripple current rating and their rated voltage. The actual capacitor value is not that critical as long as the minimum capacitance gives an acceptable ripple voltage determined by the following equation:

$$C_{MIN} = \frac{I_{RMS}}{8 \bullet f_{SW} \bullet \Delta V}$$

The output capacitors are also chosen based upon their low equivalent series resistance (ESR), ripple current and voltage ratings. The ripple current that the output capacitor experiences is a result of supplying the load current during the FET conduction time and its charging current during the FET off-time.

Voltage Feedback

The FB pin of the SC4809 sums the voltage feedback signal to the current sense signal and any added slope compensation. The voltage feedback signal is from an optocoupler, which is driven from an error amplifier on the secondary side of the converter. The signal from the optocoupler is designed to trip the FB threshold of the SC4809 internal comparator when the output voltage exceeds its specified limit.

Current Limit

Selection of the current sense resistor is accomplished by dividing the FB threshold value by the peak primary current at the desired current limit point. This ground-referenced R_{SENSE} must be a low inductance type and have a rated power level to meet the $(I_{RMS})^2 \bullet R_{SENSE}$ requirement.

Current spikes caused by the leakage inductance of the flyback transformer and the reverse recovery of the diode could trip the current sense latch and prematurely shut off the output. This unwanted spike can be suppressed by adding a small RC filter for effective leading edge blanking.

Slope Compensation

Sensing peak inductor current instead of average inductor current results in a loop response that is Less than ideal. Adding slope compensation to the current signal cancels this error by maintaining a constant average current independent of duty cycle. Slope compensation is required for open loop stability in a current mode system with 50% or greater duty cycles, but will benefit any current mode application at the cost of a few small parts.

Loop Compensation

The continuous current mode flyback will contain a right-half-plane (RHP) zero in its transfer function. Any increase in load current will require the primary peak inductor current to increase. The duty cycle must increase to accomplish this. In a flyback converter, the inductor current flows to the output only when the FET is off and the diode is conducting. Increasing the duty cycle increases the FET condition time but decreases the diode conduction time. The result of this is the average diode current, the current that supplies the load, actually decreases. This is a temporary situation; as the inductor current rises, the diode current eventually reaches its proper value. The condition where the average diode current must actually decrease before it can increase is referred to as a right-half-plane zero. To complicate matters, this zero contributes a phase lag, not a phase lead as a normal zero would. This zero moves in frequency as a function of load and input voltage, making it impossible to cancel out by the insertion of a pole.

$$f_{RHPZERO} = \frac{N \bullet V_{IN}^{\ 2}}{2 \bullet \pi \bullet R_{OUT} \bullet L_P \bullet (V_{IN} + N \bullet V_{OUT})}$$

The easiest way to deal with a right-half-plane zero is to roll off the loop gain at a relatively low frequency using simple dominant pole compensation. Unfortunately, the result of this is poor dynamic response.

The primary goal of the compensation network is to provide good line and load regulation and dynamic response. These objectives are best met by providing high gain at low frequencies for good DC regulation and high bandwidth for good transient response. Optimum closed loop performance can only be achieved by first

Application Information (Cont.)

knowing what the transfer characteristic of the PWM and switching circuit looks like. Constructing a Bode plot of the known poles and zeros in the power stage does this. Bode plots give a visual interpretation of the gain versus frequency and phase versus frequency characteristics of a system. In the gain plot, the gain shown at each frequency represents the amount by which the feedback loop will reduce a disturbance at that frequency.

Besides the RHP zero, the output capacitor and the load contribute a pole and the output capacitor alone will contribute a zero based upon its ESR.

$$f_{pole} = \frac{1+D}{2 \bullet \pi \bullet R_{OUT} \bullet C_{OUT}}$$

$$f_{zero} = \frac{1}{2\pi \bullet ESR \bullet C_{OUT}}$$

The control to output gain is calculated by:

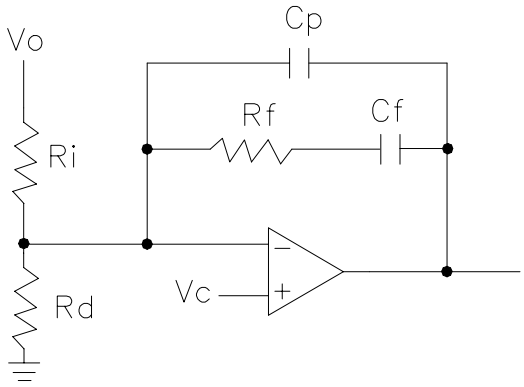
$$GAIN = 20 \bullet \log \bullet \left[\frac{I_{SC} \bullet R_{OUT} \bullet V_{IN}}{V_C \bullet (1-D) \bullet (2 \bullet N \bullet V_O + V_{IN})} \right]$$

Once the frequency response of the uncompensated system is determined, the next step is to determine what compensation is needed around the error amplifier for optimum performance. As stated earlier, optimum performance requires a high gain at low frequencies for good DC regulation and high bandwidth for good transient response. The crossover frequency, f_c, is the frequency at which the gain magnitude equals 0dB. High bandwidth is achieved by having the highest possible f_c. Because of the RHP zero, the highest possible crossover frequency is limited to $f_{RHPZERO}/\pi$. The phase margin, or the amount the phase lag measures at f_c less 180°, should be at least 45° for good transient response with little overshoot. The magnitude of the gain at the frequency where the phase plot measures - 180° is referred to as the gain margin. If the slope of the gain plot is -2, or -40dB/decade, at low frequencies, it much transition to a -20dB/decade slope, also known as a -1 slope, one decade before crossing the 0dB point. If the slope remains at the -2 slope the resultant gain margin would be too small causing sever underdamped oscillations at fc.

The scheme shown below will handle most compensation requirements. There is a pole at the origin which contributes a -1 slope in the gain plot, a low frequency zero, f_{EAZERO} flattens out the slope so the mid-range gain is equal to Rf/Ri. A high frequency pole, f_{EAPOLE} helps suppress any high frequency noise from propagating through the system. Rd forms a voltage divider with Ri and provides a DC offset.

$$f_{EAZERO} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_f}$$

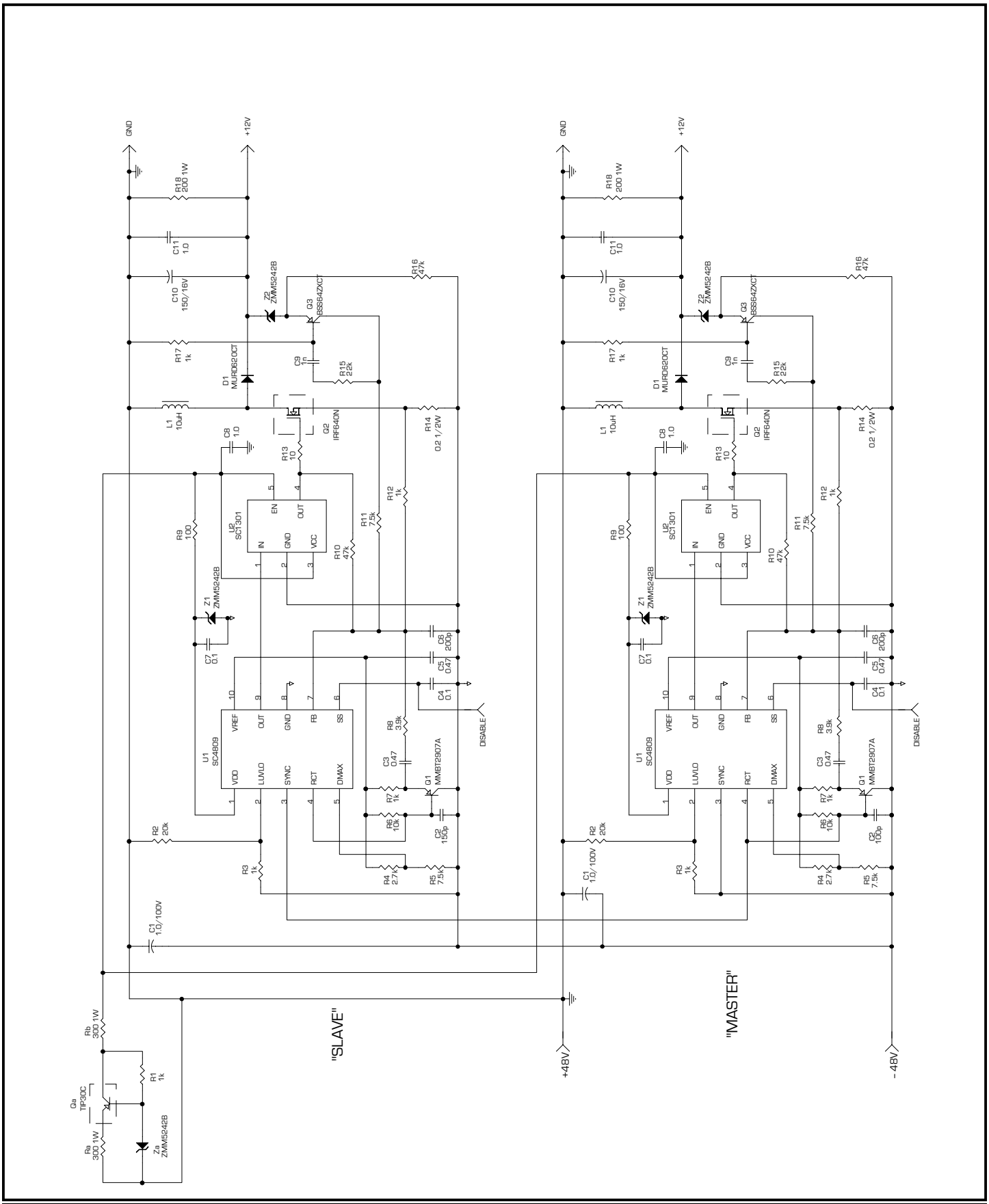
$$f_{EAPOLE} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_p}$$



By combining the Bode plots of the PWM and power stage with the error amplifier compensation, a plot of the entire system is realized.

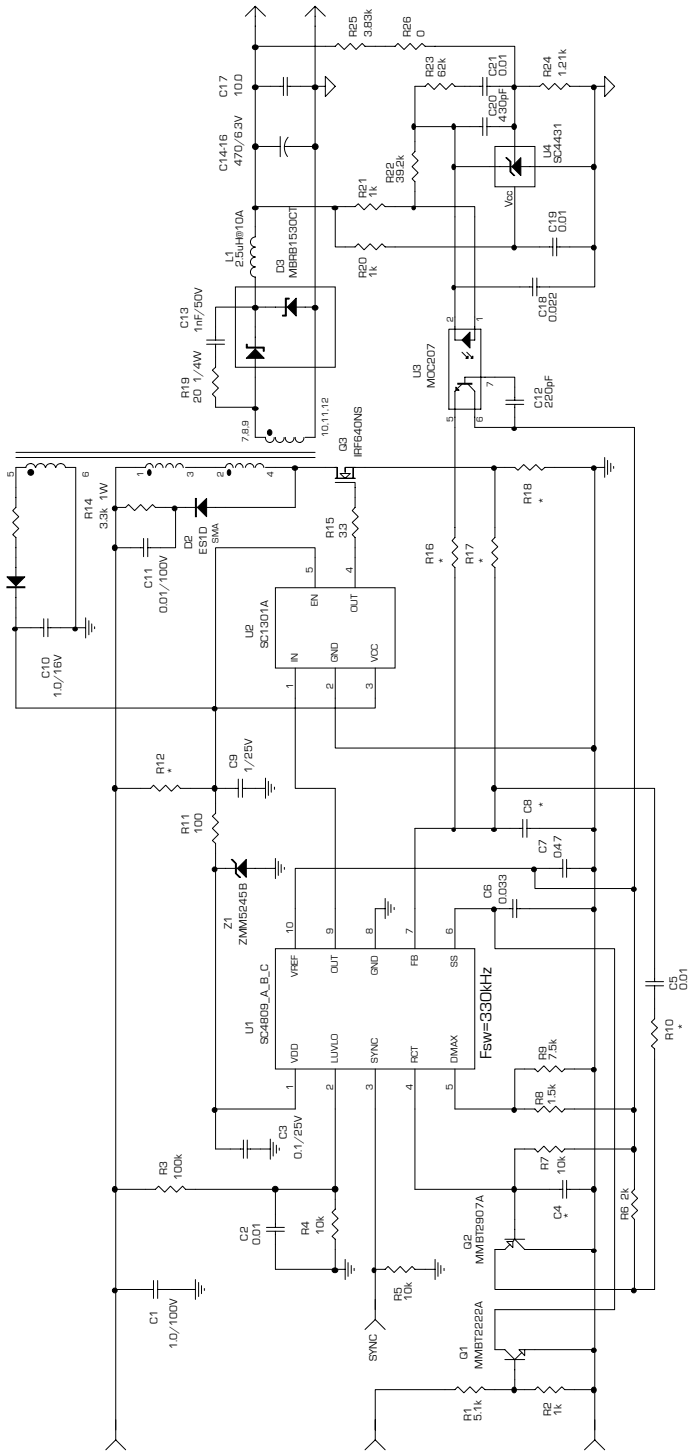
Applications Information (Cont.)

Out of Phase, Synchronized, Dual Converter



Evaluation Board Schematic

50W Forward Converter

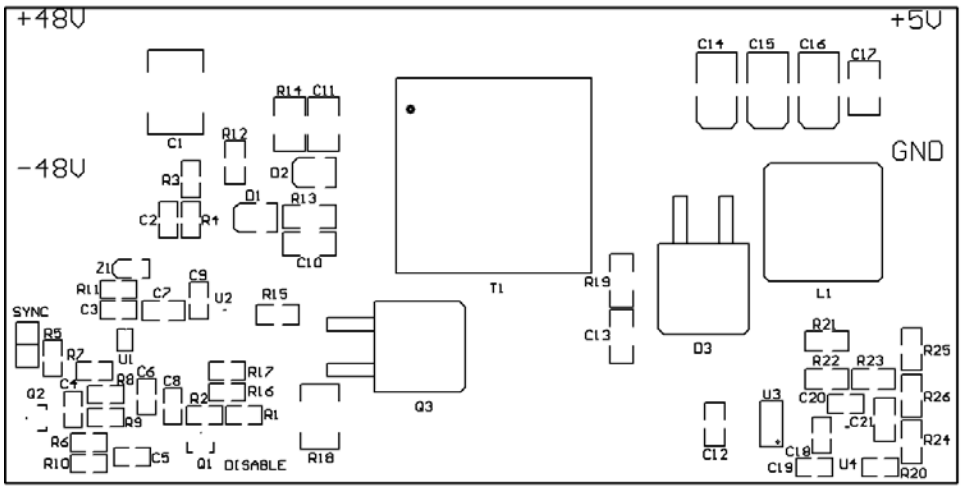


T1: PA0273, Pulse Eng.

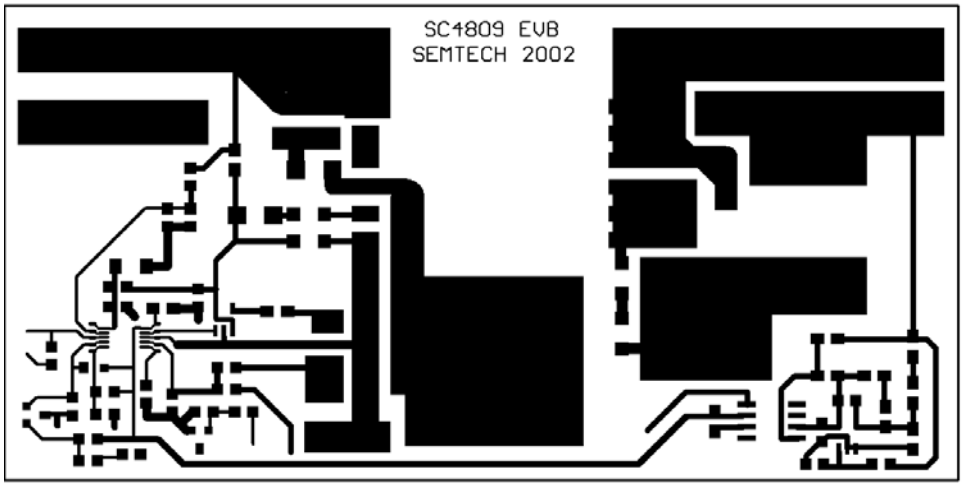
L1: ETQP6F2R5SFA, Panasonic

C14-16: 6TPB470M, PosCap, Sanyo

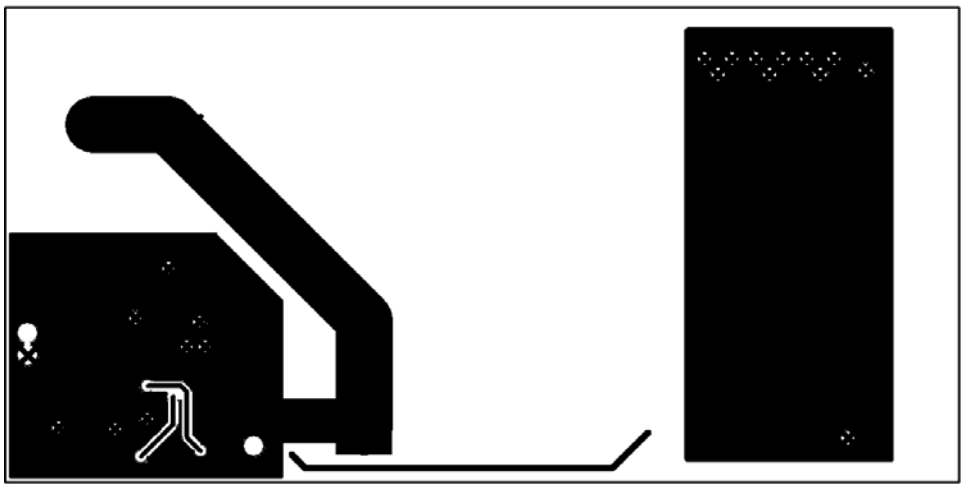
	R10	R16	R17	R18	R12	C4	C8
A	10k	62	604	0.15	2x12k||	200p	680p
B	10k	62	604	0.15	3x12k||	300p	680p
C	8.2k	100	1k	0.22	2x10k||	300p	390p



Layout

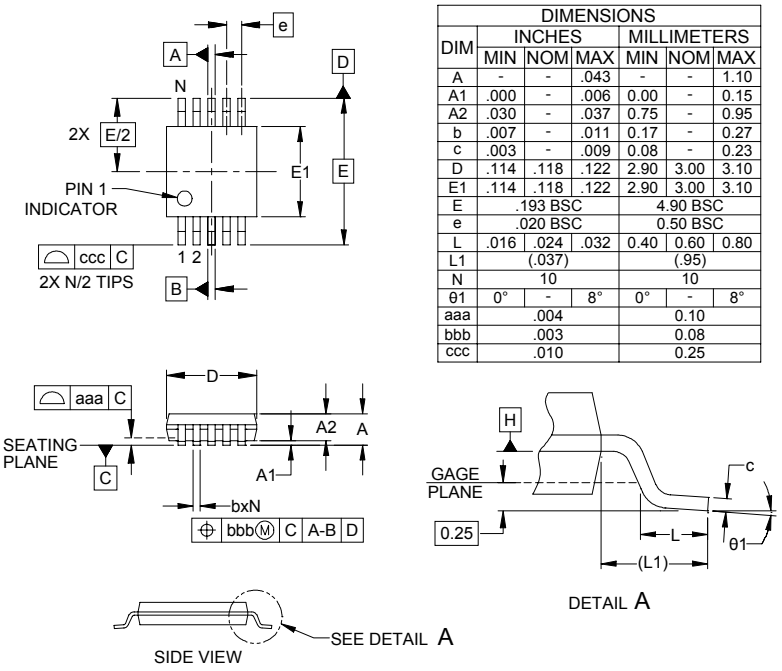


Top



Bottom

Outline Drawing - MSOP-10

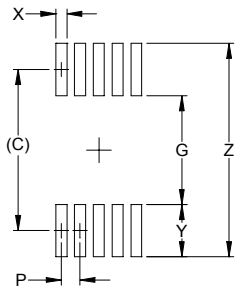


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP-10



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804

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