Applications

- Smart Meters
- In-home appliances
- Smart thermostats

Features

- Integrated PA with 30 dBm output power
- Integrated LNA with programmable bypass
- Integrated antenna switching with Tx and Rx diversity function
- Low FEM noise figure of 2 dB typical
- Single ended 50 Ω Tx/Rx RF interface
- Fast turn-ON / turn-OFF time <1 µsec
- 2.0 V – 4.8 V supply operation
- Sleep mode current <1 µA
- 4 x 4 x 0.9 mm 24 pin QFN
- Pb-free, RoHS compliant and Halogen free

Product Description

The SE2435L is a high performance, highly integrated RF Front End Module designed for high power ISM band applications operating in the 860 – 930 MHz frequency band.

The SE2435L is designed for ease of use and maximum flexibility, with fully matched 50 Ω input and output, and digital controls compatible with 1.6 – 3.6 V CMOS levels.

The RF blocks operate over a wide supply voltage range from 2.0 to 4.8 V allowing the SE2435L to be used in battery powered applications over a wide spectrum of the battery discharge curve.

Ordering Information

Part No.	Package	Remark
SE2435L-S	24 pin QFN	Samples
SE2435L-R	24 pin QFN	Tape & Reel
SE2435L-EK1	N/A	Evaluation kit

Functional Block Diagram

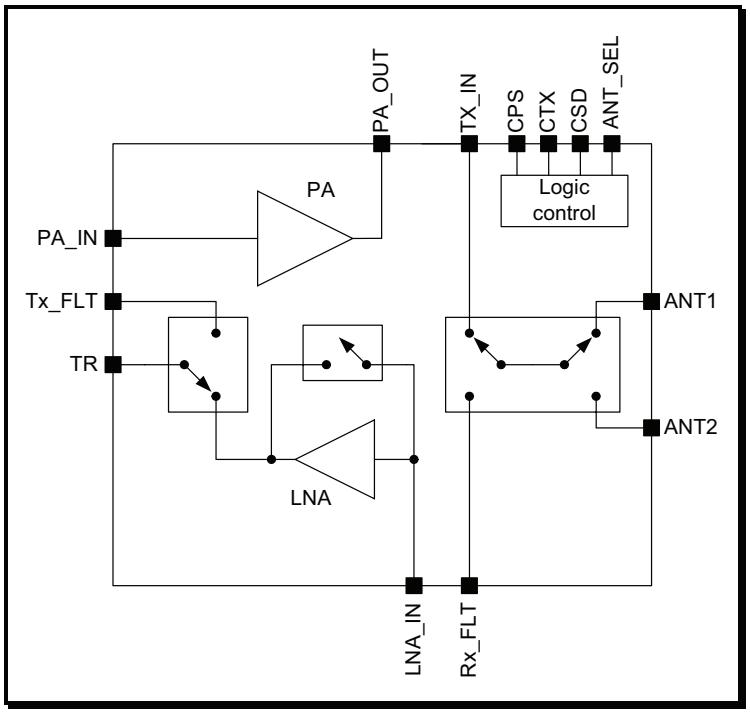

Figure 1: Functional Block Diagram

Pin Out Diagram

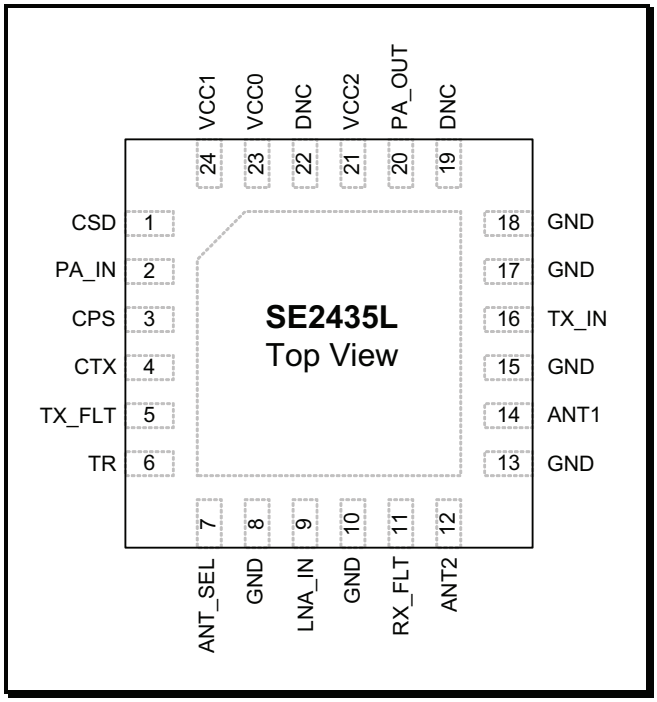

Figure 2: SE2435L Pinout

Pin Out Description

Pin No.	Name	Description
1	CSD	Shutdown control input
2	PA_IN	PA input (from Tx filter)
3	CPS	Power select control input
4	CTX	Transmit enable control input
5	TX_FLT	Transmit signal (to Tx filter)
6	TR	Bi-directional RF signal to/from transceiver
7	ANT_SEL	Antenna select control input
8	GND	Ground
9	LNA_IN	LNA input (from Rx filter)
10	GND	Ground
11	RX_FLT	Rx signal from antennas (to Rx filter)
12	ANT2	Antenna port 2
13	GND	Ground
14	ANT1	Antenna port 1
15	GND	Ground
16	TX_IN	Tx signal to antennas (from OMN)

Pin No.	Name	Description
17	GND	Ground
18	GND	Ground
19	DNC	Do not connect
20	PA_OUT	PA output (to OMN)
21	VCC2	Positive power supply
22	DNC	Do not connect
23	VCC0	Positive power supply
24	VCC1	Positive power supply
Paddle	GND	Exposed die paddle; electrical and thermal ground; Connect to PCB ground

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below.

Symbol	Definition	Note	Min.	Max.	Unit
VCC	Supply Voltage – No RF	1	-0.3	5.5	V
	Control pin voltages		-0.3	3.6	V
T_{OP}	Operating temperature		-40	85	°C
$T_{STORAGE}$	Storage temperature		-40	125	°C
	ESD Voltage all pins (HBM)	1	-	1000	V
Pin_Tx_max	Tx input power at TR port		-	+10	dBm
Pin_Rx_max	Rx input power at ANT1 or ANT2 ports		-	+10	dBm

Note: (1) No damage assuming only one parameter is set at limit at a time with all other parameters set at or below the recommended operating conditions.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Ambient temperature	-40	25	85	°C
VCC	Supply voltage on VCC	2.0	4.0	4.8	V

DC Electrical Characteristics

Conditions: VCC = 4.0 V, T_A = 25 °C, as measured on SiGe Semiconductor's SE2435L-EK1 evaluation board (de-embedded to device), unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC-Tx30}$	Total Supply Current	Tx mode P_{OUT} = 30 dBm CPS = CSD = CTX = HIGH	-	500	-	mA
$I_{CC-Tx27}$	Total Supply Current	Tx mode P_{OUT} = 27 dBm CPS = CSD = CTX = HIGH	-	350	-	mA
$I_{CC-Tx24}$	Total Supply Current	Tx mode P_{OUT} = 24 dBm CPS = CSD = CTX = HIGH	-	250	-	mA
I_{CQ-Tx}	Quiescent Current	No RF CPS = CSD = CTX = HIGH	-	45	-	mA
I_{CC-Rx}	Total Supply Current	Rx mode CPS = CSD = HIGH, CTX = 0 V	-	5	-	mA
$I_{CC-RxBypass}$	Total Supply Current	Rx bypass mode CSD = HIGH, CPS = CTX = 0 V	-	-	280	uA
I_{CC_OFF}	Sleep Supply Current	No RF, CSD = 0 V	-	-	1	µA

Logic Characteristics

Conditions: T_A = 25 °C, as measured on SiGe Semiconductor's SE2435L-EK1 evaluation board (de-embedded to device), unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Logic input high		1.6	-	VCC	V
V_{IL}	Logic input low		0	-	0.3	V
I_{IH}	Logic input high		-	-	1	µA
I_{IL}	Logic input low		-	-	1	µA

Logic Controls

Conditions: T_A = 25 °C

Mode	Mode description	Note	CPS	CSD	CTX
0	All off (sleep mode)	1	X	0	X
1	Rx bypass mode	1, 2	0	1	0
2	Rx LNA mode	1, 2	1	1	0
3	Tx mode	1, 2	1	1	1

Note: (1) Logic '0' level compliant to V_{IL} as specified in the "Logic Characteristics" table
(2) Logic '1' level compliant to V_{IH} as specified in the "Logic Characteristics" table

Conditions: T_A = 25 °C

Mode description	Note	CPS	CSD	CTX	ANT_SEL
ANT1 port enabled	1	X	X	X	0
ANT2 port enabled	2	X	X	X	1

Note: (1) Logic '0' level compliant to V_{IL} as specified in the "Logic Characteristics" table
(2) Logic '1' level compliant to V_{IH} as specified in the "Logic Characteristics" table

AC Electrical Characteristics, Transmit

Conditions: VCC = 4.0 V, T_A = 25 °C, as measured on SiGe Semiconductor's SE2435L-EK1 evaluation board (de-embedded to device), all unused ports terminated with 50 Ω, unless otherwise noted. Input port TR, output ports ANT1 and ANT2. Lumped elements filter connected between the Tx_FLT and PA_IN pins.

Symbol	Parameter	Condition	Note	Min.	Typ.	Max.	Unit
F_{IN}	Frequency Range			860	-	930	MHz
Pout_900	Output power at ANT1 or ANT2 ports in the 900 – 930 MHz frequency range	VCC = 4.0 V VCC = 3.6 V VCC = 3.0 V VCC = 2.0 V	1, 5	-	30 27 24 19	-	dBm
Pout_860	Output power at ANT1 or ANT2 ports in the 860 – 870 MHz frequency range	VCC = 4.0 V VCC = 3.6 V VCC = 3.0 V VCC = 2.0 V	2, 5	-	27 24 21 18	-	dBm
PAE	PA Power added efficiency	Pout = 28 dBm at PA_OUT port, 915 MHz			64		%
S_{21_900}	Small Signal Gain	900 – 930 MHz	1	26	-	-	dB
S_{21_860}	Small Signal Gain	860 – 870 MHz	2	26	-	-	dB
ΔS_{21}	Small Signal Gain Variation	Gain variation across frequency range	1, 2	-	-	2	dBp-p
$S22_{ANT1,2}$	Output Return Loss	Into 50 Ω, ANT1 and ANT2 ports	1, 2	-	-10	-6	dB
HD2	Harmonics	P_{OUT} = 30 dBm	1, 3	-	-	-32	dBm
HD3 – HD10	Harmonics	P_{OUT} = 30 dBm	1, 3	-	-	-43	dBm
HD2 – HD10	Harmonics	P_{OUT} = 27 dBm	2, 3	-	-	-35	dBm
T_{ON}	Turn on time		4	-	-	1	us
T_{OFF}	Turn off time		5	-	-	1	us
STAB	Stability	CW, P_{IN} = 0 dBm 0.1 GHz – 20 GHz Load VSWR = 6:1		All non-harmonically related outputs less than -43 dBm			
RU	Ruggedness	CW, Pout = 30 dBm into 50 Ω, Load VSWR = 10:1		No permanent damage			

Note:
(1) 900 – 930 MHz with specified matching network on the SE2435L-EK1 evaluation board
(2) 860 – 870 MHz with specified matching network on the SE2435L-EK1 evaluation board
(3) Measured with Continuous Wave signal
(4) From 50% of CTX edge to 90% of final RF output power
(5) From 50% of CTX edge to 10% of final RF output power

AC Electrical Characteristics, Receive

Conditions: VCC = 4.0 V, T_A = 25 °C, as measured on SiGe Semiconductor's SE2435L-EK1 evaluation board (de-embedded to device), all unused ports terminated with 50 Ω, unless otherwise noted. Input port ANT1 or ANT2, output port TR. 0 Ω connected between the Rx_FLT and LNA_IN pins, in lieu of external filters.

Symbol	Parameter	Condition	Note	Min.	Typ.	Max.	Unit
F_{IN}	Frequency Range			860	-	930	MHz
Rx_gain	Receive gain	CPS = CSD = logic '1', CTX = logic '0'	1, 2	16	18	20	dB
NF	Receive noise figure	CPS = CSD = logic '1', CTX = logic '0'	1, 2	-	2	2.5	dB
IIP3	Input 3rd order intercept	CPS = CSD = logic '1', CTX = logic '0'	1, 2	-5	-2	-	dBm
IP1dB	Input 1-dB compression point	CPS = CSD = logic '1', CTX = logic '0'	1, 2	-15	-12	-	dBm
$S11_{ANT1,2}$	Antenna port return loss	Into 50 Ω, ANT1 and ANT2 ports	1, 2	-	-12	-10	dB
T_{ON}	Turn on time		3	-	-	1	us
T_{OFF}	Turn off time		4	-	-	1	us
G_bp	Gain in bypass mode	CPS = CTX = logic '0', CSD = logic '1'		-3	-2	-	dB
IP1dB	Input 1-dB compression point in bypass mode	CPS = CTX = logic '0', CSD = logic '1'		10	-	-	dBm

Note: (1) 900 – 930 MHz
(2) 860 – 870 MHz
(3) From 50% of CTX edge to 90% of final RF output power
(4) From 50% of CTX edge to 10% of final RF output power

AC Electrical Characteristics, Diversity Antenna Function

Conditions: VCC = 4.0 V, T_A = 25 °C, as measured on SiGe Semiconductor's SE2435L-EK1 evaluation board (de-embedded to device), all unused ports terminated with 50 Ω, unless otherwise noted.

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
$ISOL_{ANTSW}$	Isolation Between ANT1 and ANT2 Ports	1, 2	-	-20	-	dB
Tx_ANT1	Insertion loss from TX_IN to ANT1	1, 2	-	0.8	-	dB
Tx_ANT2	Insertion loss from TX_IN to ANT2	1, 2	-	0.8	-	dB
Rx_ANT1	Insertion loss from ANT1 to Rx_FILT	1, 2	-	0.6	-	dB
Rx_ANT2	Insertion loss from ANT2 to Rx_FILT	1, 2	-	0.6	-	dB
TxRx_Tx	Insertion loss from TR to Tx_FILT	1, 2	-	0.5	-	dB
$T_{ANT1-ANT2}$	Antenna 1 to Antenna 2 switching time	1, 2	-	400	-	nsec

Note: (1) 900 – 930 MHz
(2) 860 – 870 MHz

Package Drawing

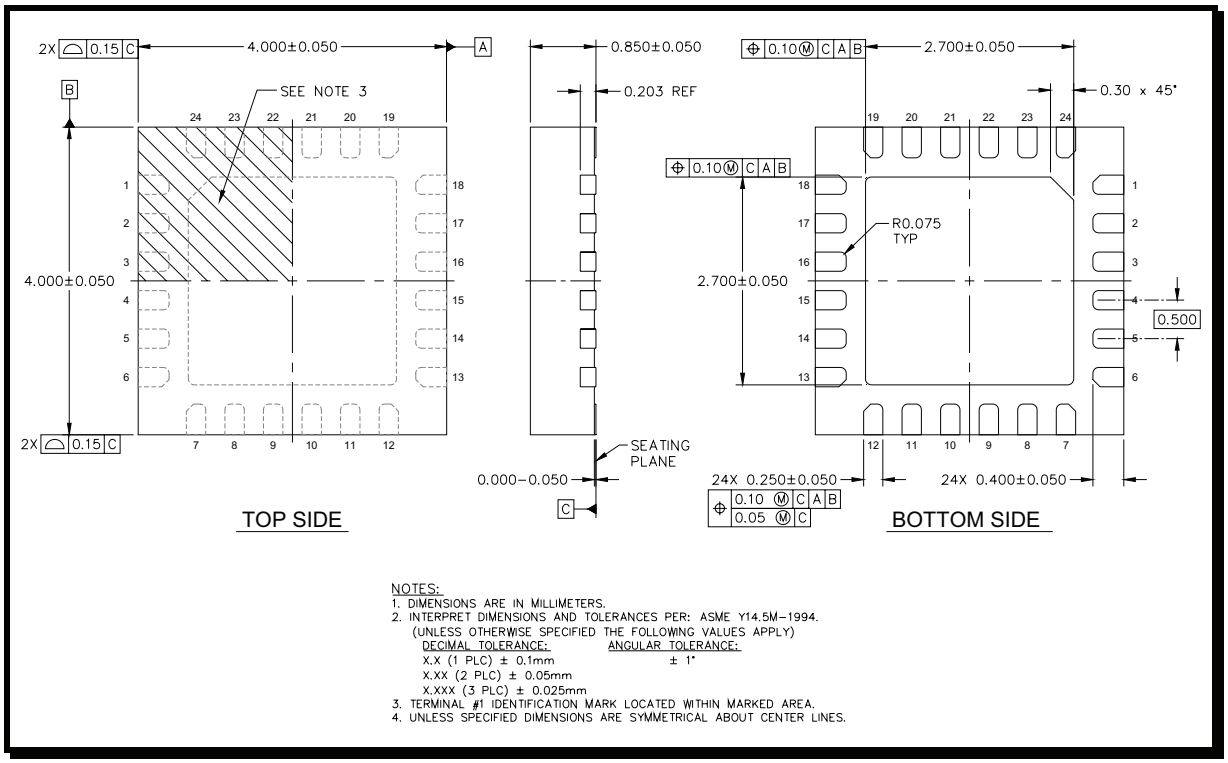

Figure 3: Package Drawing: Topside

Tape and Reel Information

Parameter	Value
Devices Per Reel	3000
Reel Diameter	13 inches
Tape Width	12 millimeters

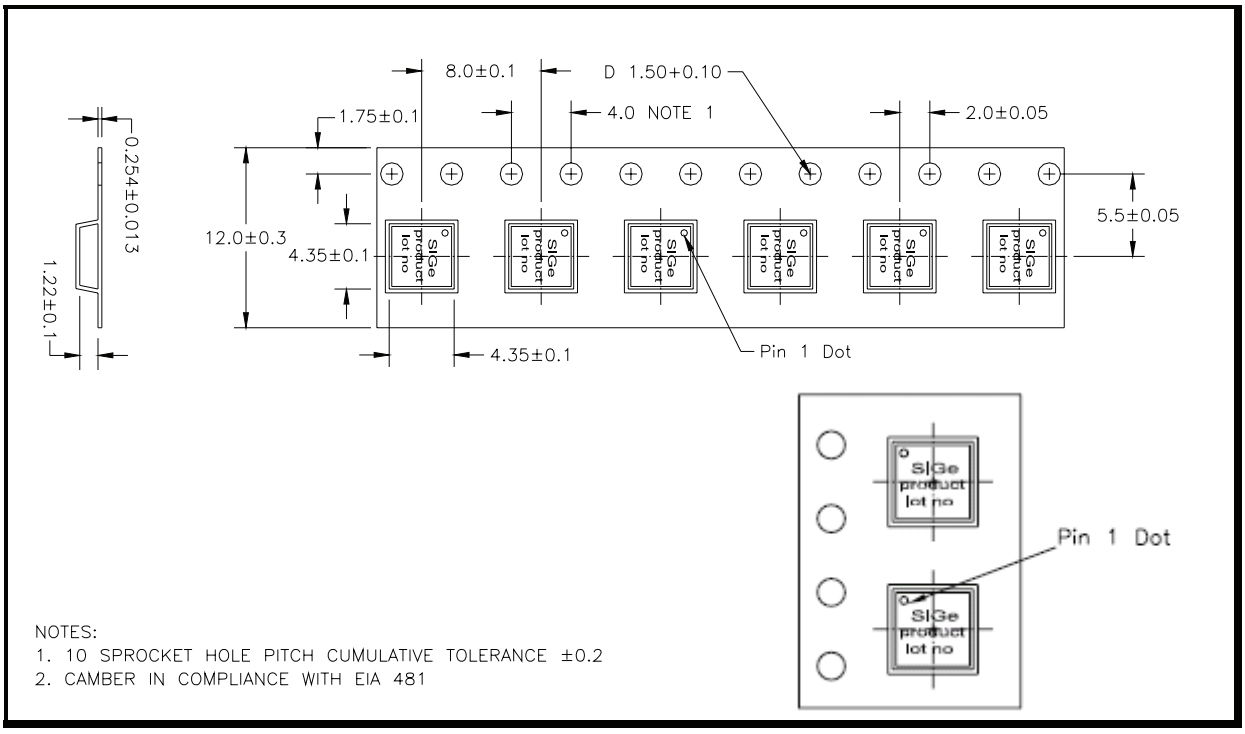

Figure 4: Detailed Tape and Reel Information (All diminensions in Millimeters)

Recommended Reflow Temperature Profile

Profile Feature	SnPb Eutectic Assembly	Lead (Pb) Free Assembly
Average Ramp-up Rate (T_L to T_P)	3°C/s (max)	3°C/s (max)
Preheat		
Temperature Min. (T_{smin})	100°C	150°C
Temperature Max. (T_{smax})	150°C	200°C
Time (Min. to Max) (t_s)	60 - 120s	60 - 80s
Ramp Up		
Tsmax to t_L	-	3°C/s (max)
Time 25°C to Peak Temperature	6 mins. (max)	8 mins. (max)
Reflow		
Temperature (t_L)	183°C	217°C
Time maintained above t_L	60 - 150s	60 - 150s
Peak Temperature (t_p)	240 ±5°C	260 +0/-5°C
Time Within 5°C of Actual Peak Temperature (t_p)	10 - 30s	20 - 40s
Ramp-Down		
Ramp-Down Rate	6°C/s (max)	6°C/s (max)

Reflow Profile (Reference JEDEC J-STD-020)

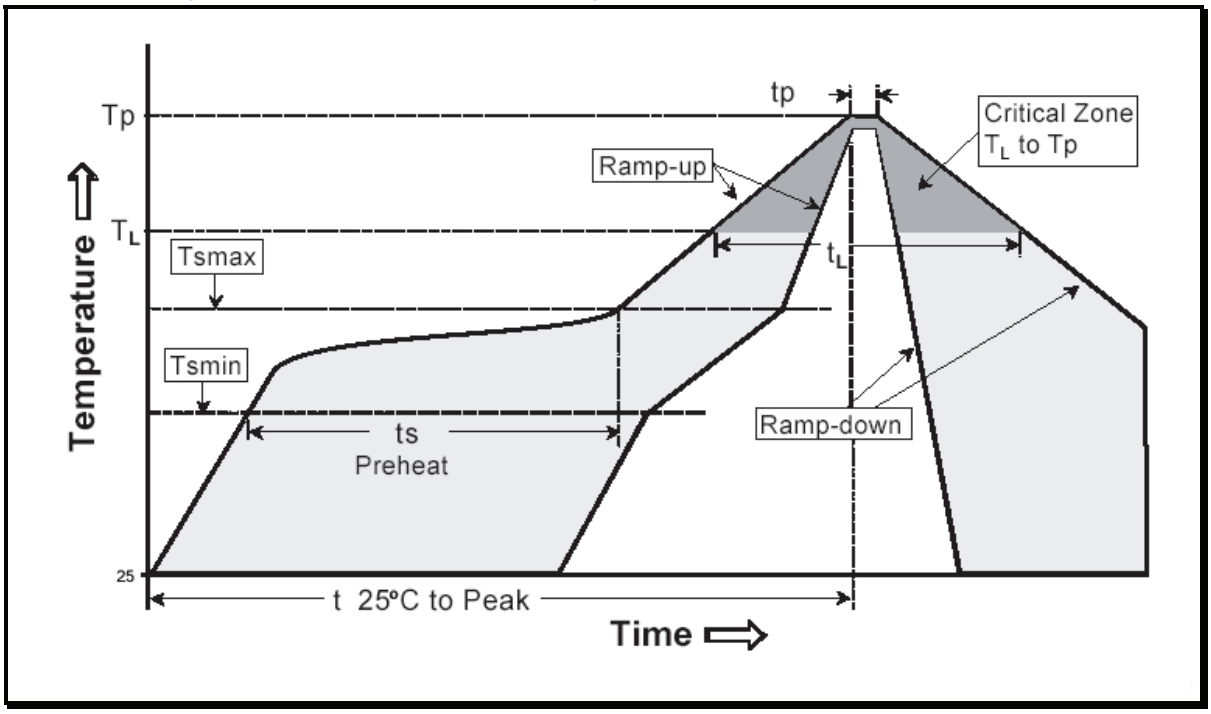

Figure 5: Reflow temperature profile

Branding Information

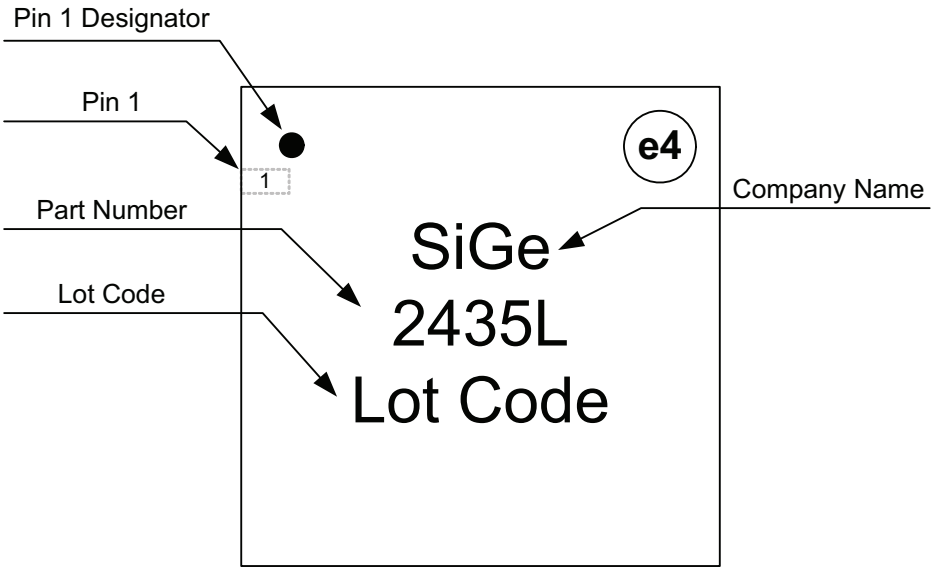

Figure 6: SE2435L Branding

Document Change History

Revision	Date	Notes
1.0	June 11, 2010	Initial release
1.1	July 14, 2010	Updated pinout description
1.2	October 7, 2010	General updates and corrections
1.3	November 5, 2010	Update harmonics limits to reflect compliance with FCC and ETSI
1.4	December 2, 2010	Added specs for PA PAE. Updated package branding

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Product Preview
The datasheet contains information from the product concept specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Preliminary Information
The datasheet contains information from the design target specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Production testing may not include testing of all parameters.

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