FAIRCHILD SEMICONDUCTOR®

August 2010

SG1577A
Dual Synchronous DC/DC Controller

Features

- Integrated Two Sets of MOSFET Drivers
- Two Independent PWM Controllers
- Constant Frequency Operation: Free-Running Fixed Frequency Oscillator Programmable: 61kHz to 340kHz
- Maximum Input Supply Voltage: 15V
- Programmable Output as Low as 0.7V
- Internal Error Amplifier Reference Voltage: 0.7V±1.5%
- Two Soft-Start / EN Functions
- Programmable Over-Current Protection (OCP)
- 30V HIGH Voltage Pin for Bootstrap Voltage
- Output Over-Voltage Protection (OVP)
- 20-Pin SOP

Applications

- CPU and GPU Vcore Power Supply
- Power Supply Requiring Two Independent Outputs

Description

The SG1577A is a high-efficiency, voltage-mode, dual-channel, synchronous DC/DC PWM controller for two independent outputs. The two channels are operated out of phase. The internal reference voltage is trimmed to 0.7V±1.5%. It is connected to the error amplifier's positive terminal for voltage feedback regulation.

The soft-start circuit ensures the output voltage can be gradually and smoothly increased from zero to its final regulated value. The soft-start pin can also be used for chip-enable function. When two soft-start pins are grounded, the chip is disabled and the total operation current can be reduced to under 0.7mA.

The fixed-frequency is programmable from 60kHz to 340kHz. The Over-Current Protection (OCP) level can be programmed by an external current-sense resistor. It has two integrated sets of internal MOSFET drivers.

SG1577A is available in a 20-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
SG1577ASY	-40°C to +105°C	20-Lead, Small Outline Package (SOP-20)	Tape & Reel

Application Diagram

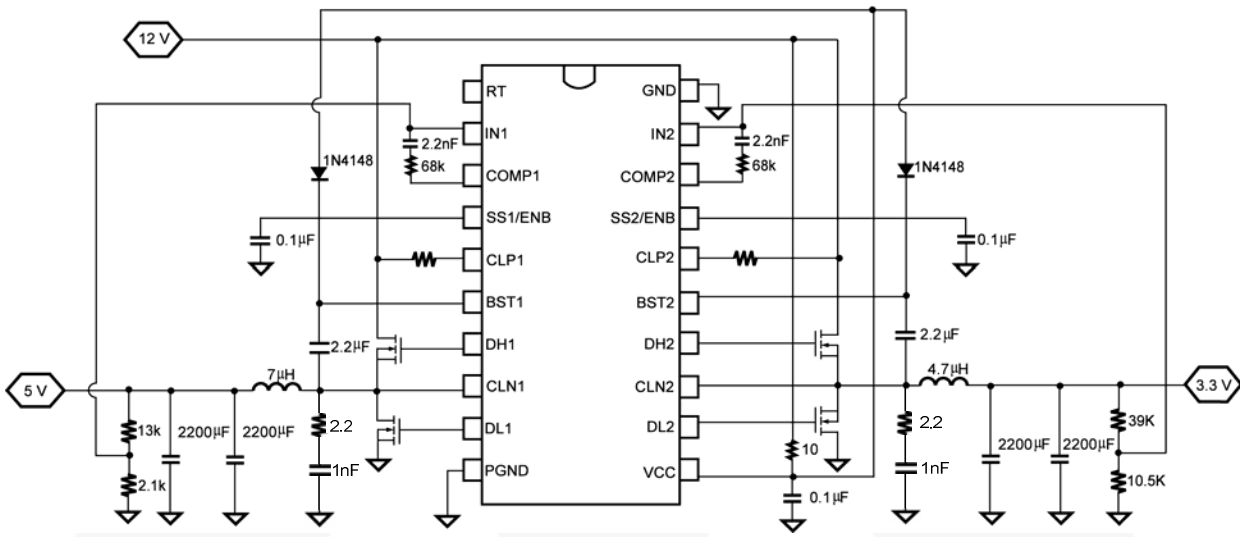


Figure 1. Typical Application

Internal Block Diagram

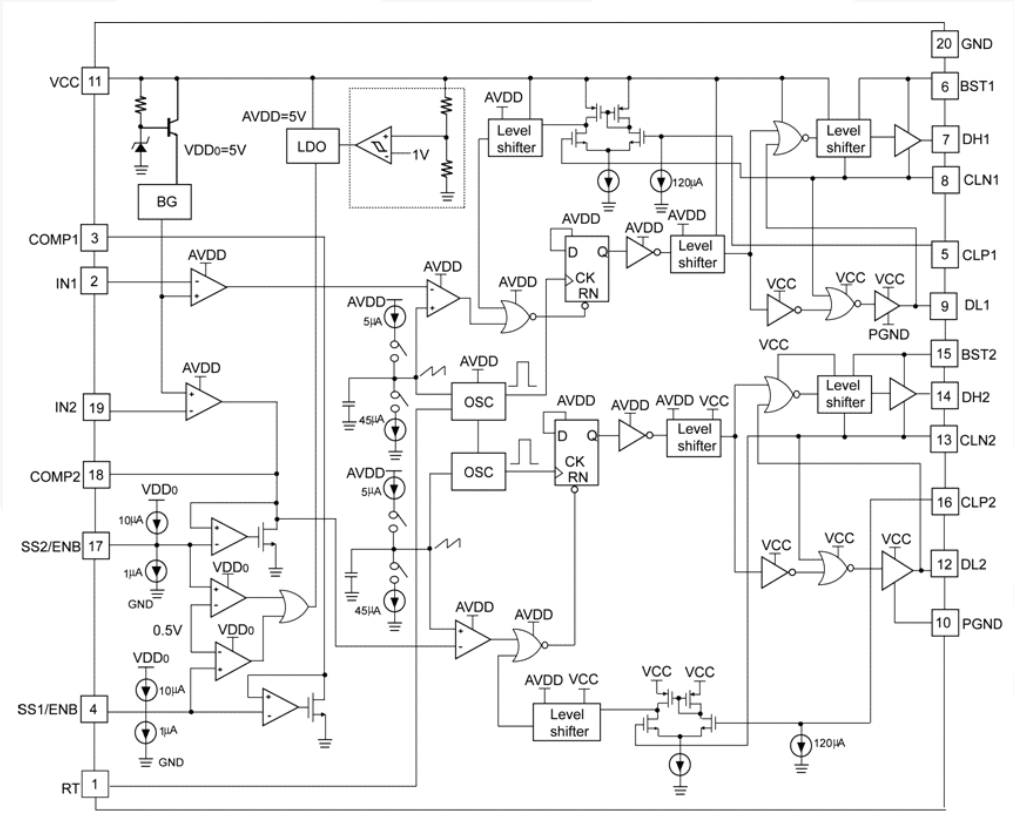
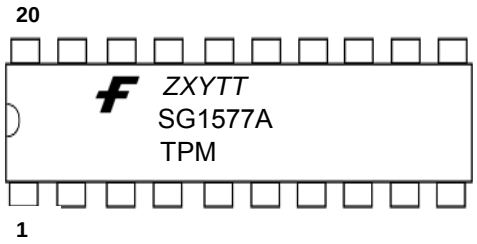


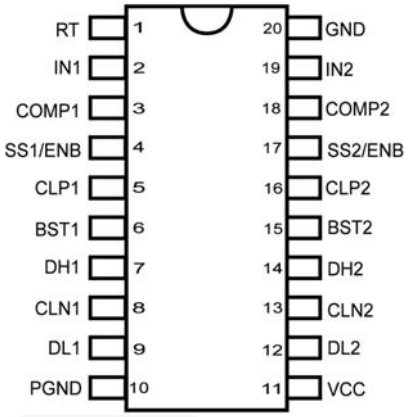
Figure 2. Functional Block Diagram

Marking Diagram



F: Fairchild Logo
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: S = SOP
P: Y=Green Package
M: Mask Version

SOP-20



Pin Configuration

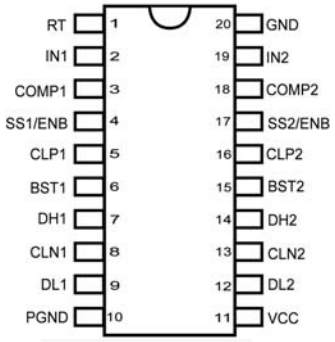


Figure 3. SOP-20 Pin Configuration (Top View)

Pin Definitions

Name	Pin #	Type	Description
RT	1	Frequency Select	Switching frequency programming pin. An external resistor connecting this pin to GND can program the switching frequency. The switching frequency is 61kHz when RT is open and becomes 340kHz when RT is shorted to ground.
IN1	2	Feedback	Inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider.
COMP1	3	Compensation	Output of the error amplifier and input to the PWM comparator. It is used for feedback loop compensation.
SS1/ENB	4	Soft Start/Enable	A 35/15μA internal current source charging an external capacitor for soft-start. Pull down this pin and pin 17 to disable the chip.
CLP1	5	Over Current Protection	Over-current protection for high-side MOSFET. Connect a resistor from this pin to the high-side supply voltage to program the OCP level.
BST1	6	Boost Supply	Supply for high-side driver. Connect to the internal bootstrap circuit.
DH1	7	High-Side Drive	Channel 1, high-side MOSFET gate driver pin.
CLN1	8	Switch Node	Switch-node connection to inductor. For channel 1 high-side driver's reference ground.
DL1	9	Low-Side Drive	Low-side MOSFET gate driver pin.
PGND	10	Driver Ground	Driver circuit reference. Connect to low-side MOSFET GND.
VCC	11	Power Supply	Supply voltage input.
DL2	12	Low-Side Drive	Low-side MOSFET gate driver pin.
CLN2	13	Switch Node	Switch-node connection to inductor. For channel 2, high-side driver's reference ground.
DH2	14	High-Side Drive	Channel 2 high-side MOSFET gate driver pin.
BST2	15	Boost Supply	Supply for high-side driver. Connect to the internal bootstrap circuit.
CLP2	16	Over-Current Protection	Over-current protection for the high-side MOSFET. Connect a resistor from this pin to the high-side supply voltage to program the OCP level.
SS2/ENB	17	Soft-Start/Enable	A 35/15μA internal current source charging an external capacitor for soft-start. Pull down this pin and pin 4 to disable the chip.
COMP2	18	Compensation	Output of the error amplifier and input to the PWM comparator. It is used for feedback-loop compensation.
IN2	19	Feedback	Inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider.
GND	20	Analog Ground	The reference of internal control circuits.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to the network ground terminal. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage, VCC to GND			16	V
BST1(or 2) - CLN1(or 2)	BST1(2) to CLN1(2)			16	V
CLN1(or 2) - GND	CLN1(2) to GND for 100ns Transient		-4	18	V
BST1(or 2) - GND	BST1(2) to GND for 100ns Transient			30	V
DH1(or 2) - CLN1(or 2)				16	V
CLN1(or 2), DL1(or 2)			-0.3	V_{CC}+0.3	V
PGND	PGND to GND			± 1	V
Θ_{JA}	Thermal Resistance, Junction-Air			90	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-65	+150	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model (HBM)		2	kV
		Charged Device Model (CDM)		1	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage		+15	V
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{CC}=12V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC} UVLO						
V_{CC_ON}	Turn-On Threshold	V_{CC} Ramp-Up	9.5	10.0	10.5	V
V_{CC_HYS}	UVLO Hysteresis	V_{CC} Ramp-Down	1.5	2.0	2.5	V
Oscillator						
f_{osc}	Oscillator Frequency	R_{RT}=OPEN	55	61	67	KHz
		R_{RT}=GND	308	340	372	
$f_{osc,rt}$	Total Accuracy	20kΩ < R_{RT}	-10		10	%
D_{ON_MAX}	Maximum Duty Cycle		85	90	95	%
Error Amplifier						
V_{REF}	Internal Reference Voltage	V_{CC}=8V, V_{CC}=15V	0.6895	0.7000	0.7105	V
$\triangle V_{REF}$ (1)	V_{REF} Temperature Coefficient	T_A=0~85°C		0.03		mV/°C
A_{VOL}	Open-loop Voltage Gain			77		dB
BW	Unity Gain Bandwidth			3.5		MHz
I_{SOURCE}	Output Source Current	IN1=IN2=0.6V	60	80	100	µA
I_{SINK}	Output Sink Current	IN1=IN2=0.8V	250	400	550	µA
V_{RAMP_Peak}	The Peak of V_{RAMP}	Gate Output=D_{ON_MAX}	2.45	2.8	3.15	V
V_{RAMP_Valley}	The Valley of V_{RAMP}	No Gate Output	1.05	1.2	1.35	V
Two-Stage Soft-Start						
$I_{SOURCE\_1}{}^{st}$	1st Soft-start Charge Current	V_{CLP} < V_{CLN} , $V_{SS\_Transition}$ > V_{SS}	28	35	42	µA
$I_{SOURCE\_2}{}^{nd}$	2nd Soft-start Charge Current	V_{CLP} < V_{CLN} , $V_{SS\_Transition}$ < V_{SS}	13	16	19	µA
$V_{SS\_Transition}$	Soft-start Transition Point	$I_{SOURCE\_1}{}^{st}$ Transit to $I_{SOURCE\_2}{}^{nd}$ *See Figure 4*	1.40	1.42	1.44	V
I_{SINK}	Soft-start Discharge Current	V_{CLP} > V_{CLN}		50		µA
Protections						
I_{OCSET}	OC Sink Current	V_{CC}=12V	90	120	150	µA
T_{OT}	Over-Temperature			150		°C
T_{OT_hys}	Over-Temperature Hysteresis			20		°C
V_{OVP}	Over-Voltage Protection of IN	V_{OVP}/V_{IN}	118	122	126	%
Output						
I_{DH}	High-Side Current Source	V_{BST} - V_{CLN}=12V, V_{DH} - V_{CLN}=6V	1.0	1.8		A
R_{DH}	High-Side Sink Resistor	V_{BST} - V_{CLN}=12V		2.8	3.8	Ω
I_{DL}	Low-Side Current Source	V_{CC}=12V, V_{DL} =6V	1.0	1.8		A
R_{DL}	Low-Side Sink Resistor	V_{CC}=12V		2.8	3.8	Ω
T_{DT} (2)	Dead Time	V_{CC}=12V, D_H & D_L=1000pF	50	70	90	ns
Total Operating Current						
I_{CC_OP}	Operating Supply Current	V_{CC}=12V, No load	3.3	4.3	5.3	mA
I_{CC_SBY}	Standby Current (Disabled)	SS1/ENB=SS2/ENB=0V		0.7	1.0	mA

Notes:
1. Not tested in production, 30pcs sample.
2. When V_{DL} falls less than 2V relative to V_{DH} rising to 2V.

Timing Diagrams

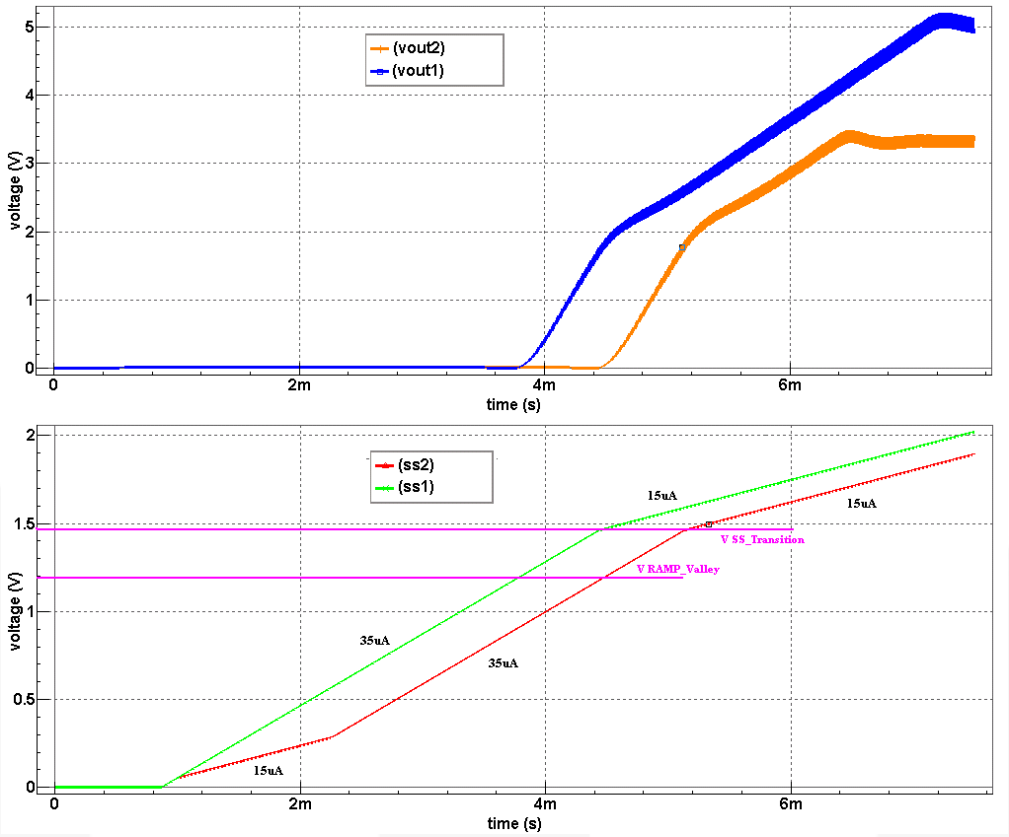


Figure 4. Timing Chart of Two-Stage Soft-Start

Typical Performance Characteristics

Unless otherwise noted, values are for V_{CC}=12V, T_A=+25°C, $C_{SS1/ENB}$=150nF and $C_{SS2/ENB}$=168nF.

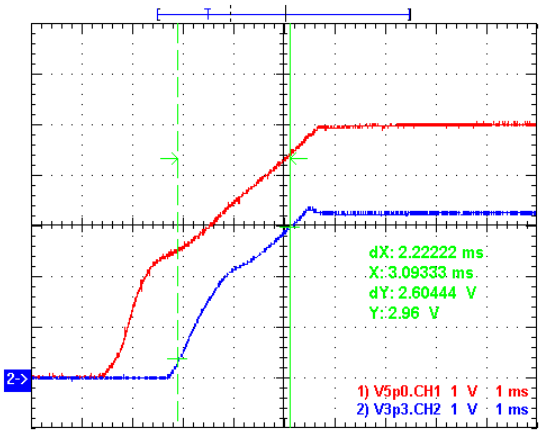


Figure 5. Power On at 0.3A Load

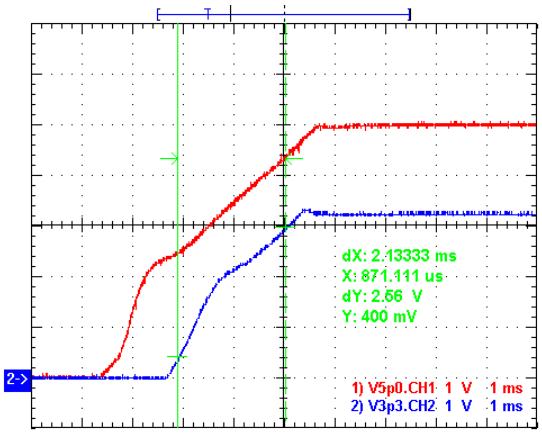


Figure 6. Power On at 3.6A Load

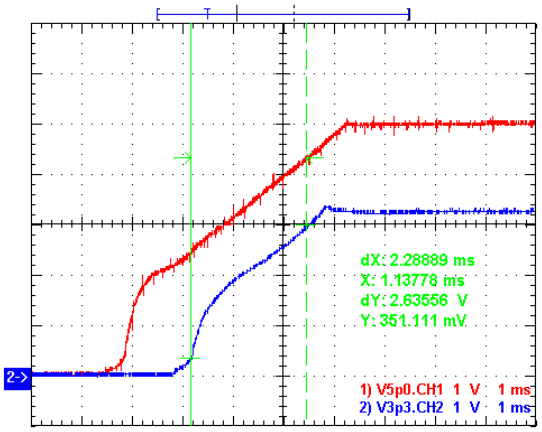


Figure 7. Power On at 9A Load

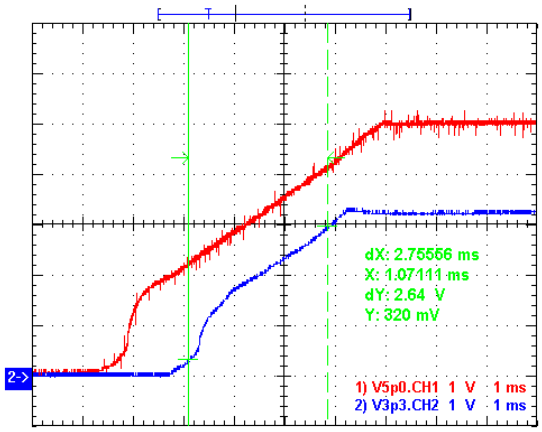


Figure 8. Power On at 18A Load

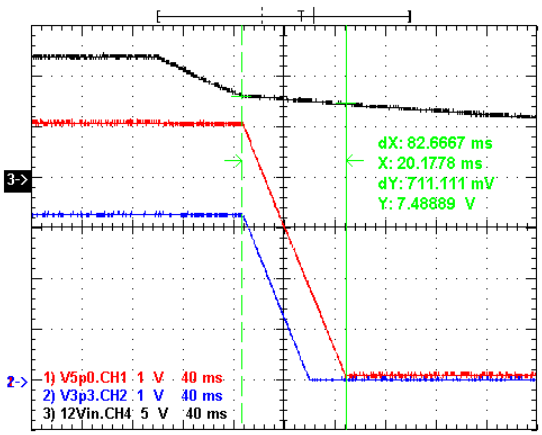


Figure 9. Power Off with 0.3A Load

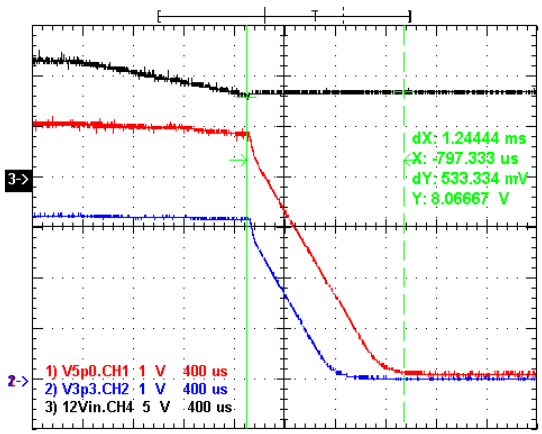


Figure 10. Power Off with 18A Load

Typical Performance Characteristics (Continued)

Unless otherwise noted, values are for V_{CC}=12V, T_A=+25°C, $C_{SS1/ENB}$=150nF and $C_{SS2/ENB}$=168nF.

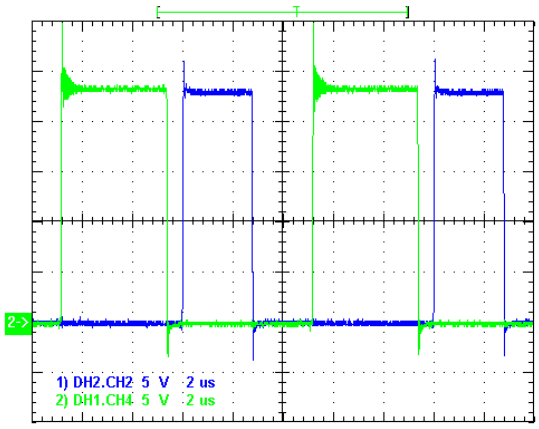


Figure 11. Phase Shift at 0.3A Load

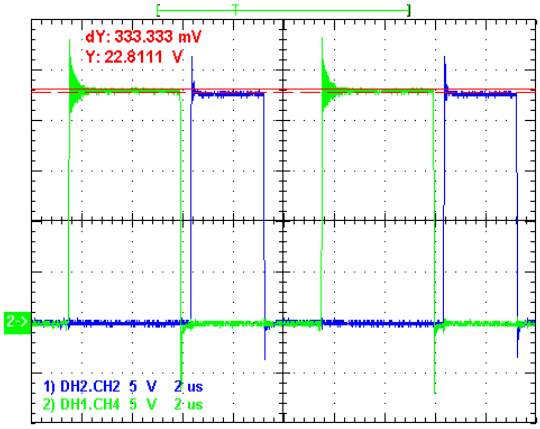


Figure 12. Phase Shift at 18A Load

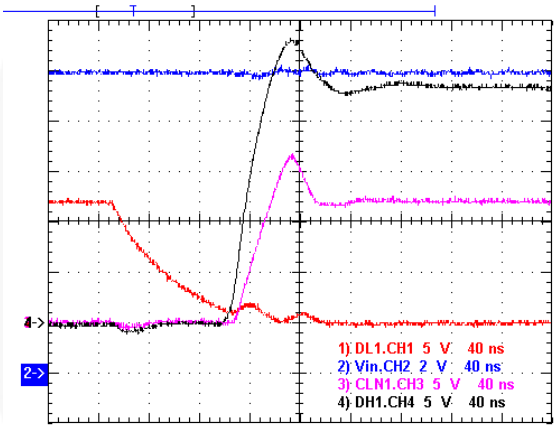


Figure 13. Dead Time at 0.3A Load (Rising Edge)

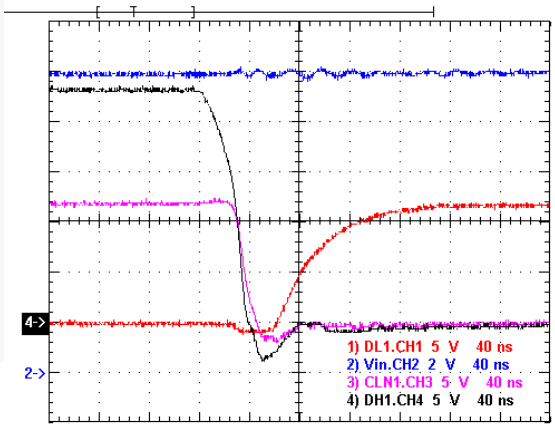


Figure 14. Dead Time at 0.3A Load (Falling Edge)

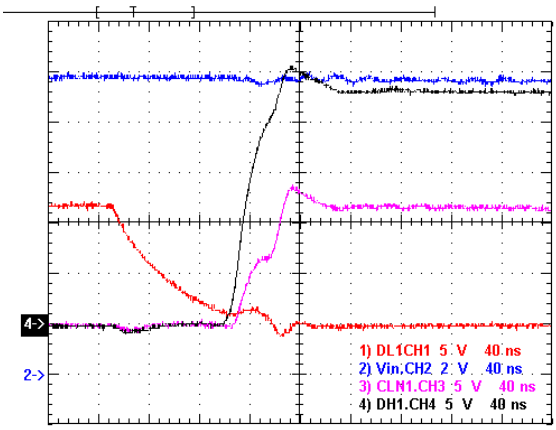


Figure 15. Dead Time at 18A Load (Rising Edge)

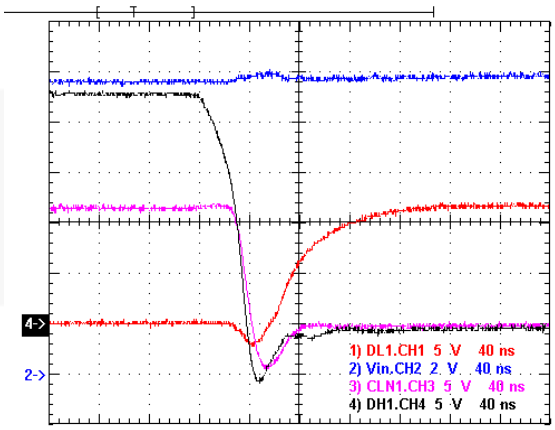


Figure 16. Dead Time at 18A Load (Falling Edge)

Typical Performance Characteristics (Continued)

Unless otherwise noted, values are for V_{CC}=12V, T_A=+25°C, $C_{SS1/ENB}$=150nF and $C_{SS2/ENB}$=168nF.

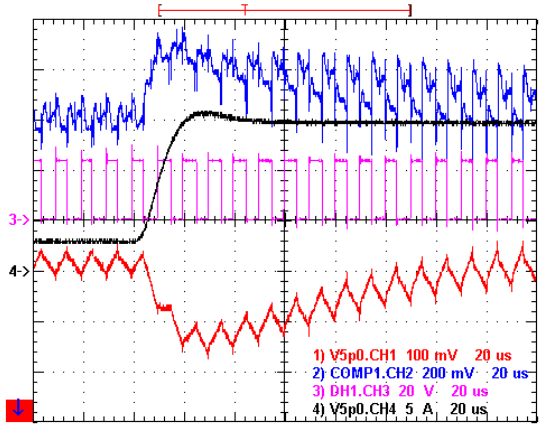


Figure 17. Load Transient Response (Step-Up) 20kΩ/22nF in Compensation Loop

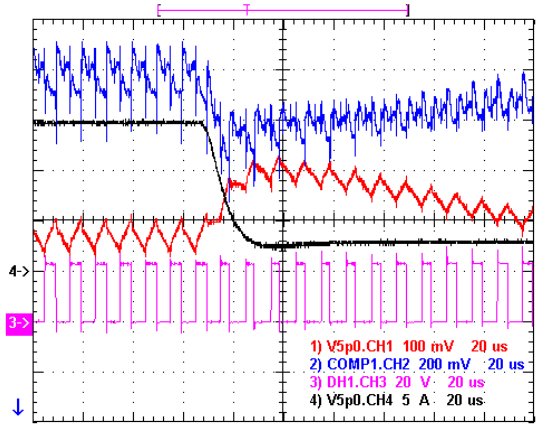


Figure 18. Load Transient Response (Step-Down) 20kΩ/22nF in Compensation Loop

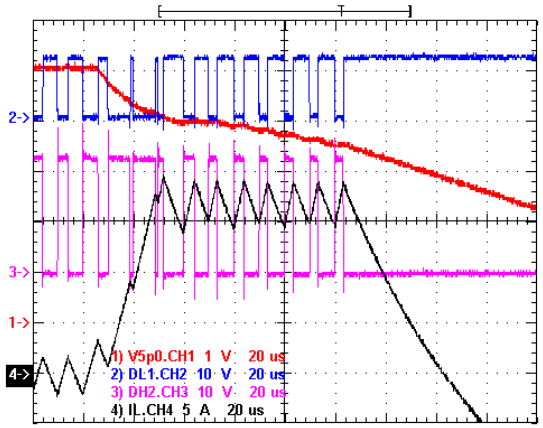


Figure 19. Over-Current Protection (OCP)

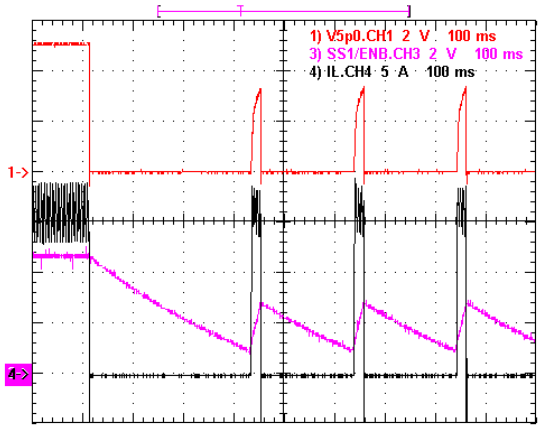


Figure 20. Over-Current Protection ("Hiccup" Mode)

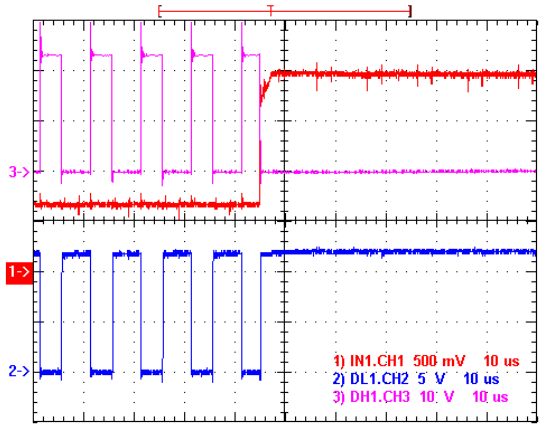


Figure 21. Over-Voltage Protection (OVP)

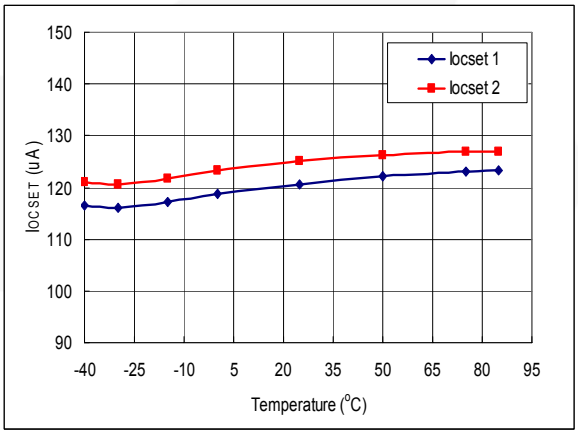


Figure 22. I_{OCSET} vs. Temperature

Functional Description

The SG1577A is a dual-channel voltage-mode PWM controller. It has two sets of synchronous MOSFET driving circuits. The two channels are running 180-degrees out of phase. The following descriptions highlight the advantages of the SG1577A design.

Soft Start

An internal start-up current (35/15μA) flows out of SS/EN pin to charge an external capacitor. During the startup sequence, SG1577A isn't enabled until the SS/ENB pin is higher than 1.2V. From 1.2V to (1.2 + 1.6 x D_{ON} / D_{ON_MAX}) V, the PWM duty cycle gradually increases following the SS/ENB pin voltage to bring output rising. After (1.2 + 1.6 x D_{ON} / D_{ON_MAX}) V, the soft-start period ends and SS/ENB pin continually rises to 4.8V. When input power is abnormal, the external capacitor on the SS pin is shorted to ground and the chip is disabled.

$$C_{SS1} \times (1.4V - 1.2V) = 35\mu A \times t_1;\ C_{SS1} \times \left(1.2V + 1.6 \times \frac{\frac{5}{12}}{0.9} - 1.4V\right) = 15\mu A \times t_2$$
$$; t_1 + t_2 = t_{SS1}$$

$$C_{SS2} \times (1.4V - 1.2V) = 35\mu A \times t_1;\ C_{SS2} \times \left(1.2V + 1.6 \times \frac{\frac{3.3}{12}}{0.9} - 1.4V\right) = 15\mu A \times t_2 \quad (1)$$
$$; t_1 + t_2 = t_{SS2}$$

$$C_{SS1} \times 1.2V = 35\mu A \times t_3;\ \frac{C_{SS2} \times 0.3V}{15\mu A} + \frac{C_{SS2} \times (1.2V - 0.3V)}{35\mu A} = t_4$$
$$; t_4 - t_3 = t_{time\text{-}shift}$$

Over-Current Protection (OCP)

Over-current protection is implemented by sensing the voltage drop across the drain and the source of external high-side MOSFET. Over-current protection is triggered when the voltage drop on external high-side MOSFET's $R_{DS(ON)}$ is greater than the programmable current limit voltage threshold. 120μA flowing through an external resistor between input voltage and the CLP pin sets the threshold of current limit voltage. When over-current condition is true, the system is protected against the cycle-by-cycle current limit. A counter counts a series of over-current peak values to eight cycles; the soft-start capacitor is discharged by a 50μA current until the voltage on SS pin reaches 1.2V. During the discharge period, the high-side driver is turned off and the low-side driver is turned on. Once the voltage on SS/ENB pin is under 1.2V, the normal soft-start sequence is initiated and the 35/15μA current charges the soft-start capacitor again.

$$I_{L(OCP)} = [(R_{SENSE} \times I_{OCSET} + V_{OFFSET}) / R_{DS(ON)} - (V_{IN} - V_{OUT}) \times V_{OUT} / (f_{OSC} \times L_{OUT} \times V_{IN} \times 2)] \quad (2)$$

where V_{OFFSET} (≒ 10mV) is the offset voltage contributed by the internal OCP comparator.

Error Amplifier

The IN1 and IN2 pins are connected to the corresponding internal error amplifier's inverting input and the outputs of the error amplifiers are connected to the corresponding COMP1 and COMP2 pins. The COMP1 and COMP2 pins are available for control-loop compensation externally. Non-inverting inputs are internally tied to a fixed 0.7V ± 1.5% reference voltage.

Oscillator Operation

The SG1577A has a frequency-programmable oscillator. The oscillator is running at 61kHz when the RT pin is floating. The oscillator frequency can be adjusted from 61kHz up to 340kHz by an external resistor R_{RT} between RT pin and the ground. The oscillator generates a sawtooth wave that has 90% rising duty. Sawtooth wave voltage threshold is from 1.2V to 2.8V. The frequency of oscillator can be programmed according to the following equation:

$$f_{OSC}, RT(kHz) = 61kHz + 8522 / R_{RT}(k\Omega) \quad (3)$$

Output Driver

The high-side gate drivers need an external bootstrapping circuit to provide the required boost voltage. The highest gate driver's output (15V is the allowed) on high-side and low-side MOSFETs forces external MOSFETs to have the lowest $R_{DS(ON)}$, which results in higher efficiency.

Over-Temperature Protection (OTP)

The device is over-temperature protected. When chip temperature is over 150°C, the chip enters tri-state (high-side driver is turned off). The hysteresis is 20°C.

Type II Compensation Design (for Output Capacitors with High ESR)

SG1577A is a voltage-mode controller; the control loop is a single voltage feedback path, including an error amplifier and PWM comparator, as shown in Figure 23. To achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. A stable control loop has a 0dB gain crossing with -20dB/decade slope and a phase margin greater than 45°.

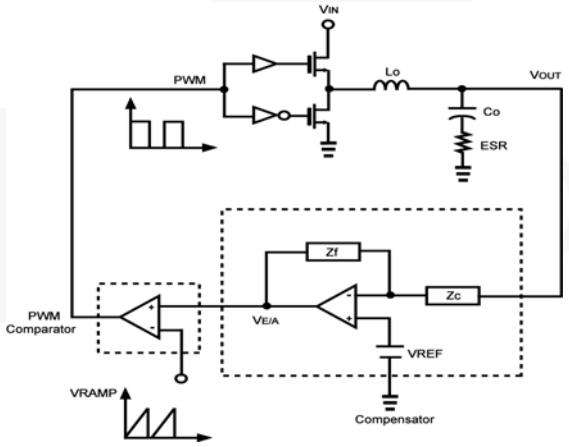


Figure 23. Closed Loop

1. Modulator Frequency Equations

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This transfer function is dominated by a DC gain and the output filter (L_O and C_O) with a double-pole frequency at f_{LC} and a zero at f_{ESR}. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{RAMP}(=1.6V). The first step is to calculate the complex conjugate poles contributed by the LC output filter. The output LC filter introduces a double pole, -40dB / decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter expressed as:

$$f_{P(LC)} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad (4)$$

The next step of compensation design is to calculate the ESR zero. The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as:

$$f_{Z(ESR)} = \frac{1}{2\pi \times C_O \times ESR} \quad (5)$$

2. Compensation Frequency Equations

The compensation network consists of the error amplifier and the impedance networks Z_C and Z_f, as Figure 24 shows.

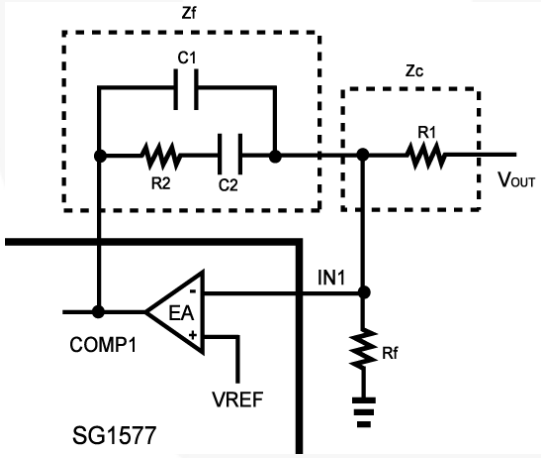


Figure 24. Compensation Loop

$$f_{P1} = 0$$
$$f_{Z1} = \frac{1}{2\pi \times R_2 \times C_2} \quad (6)$$
$$f_{P2} = \frac{1}{2\pi \times R_2 \times (C_1 // C_2)}$$

Figure 25 shows the DC-DC converter gain vs. frequency. The compensation gain uses external impedance networks Z_C and Z_f to provide a stable, high-bandwidth loop.

High crossover frequency is desirable for fast transient response, but often jeopardizes system stability. To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency. Place the zero at 75% of the LC filter resonant frequency. Crossover frequency should be higher than the ESR zero, but less than 1/5 of the switching frequency. The second pole should be placed at half the switching frequency.

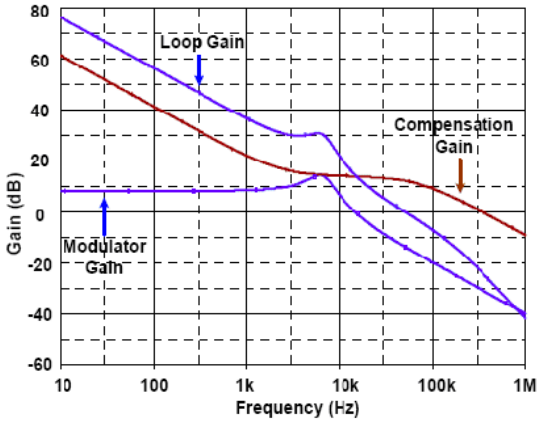


Figure 25. Bode Plot

Layout Considerations

Layout is important in high-frequency switching converter design. If designed improperly, PCB can radiate excessive noise and contribute to converter instability.

Place the PWM power stage components first. Mount all the power components and connections in the top layer with wide copper areas. The MOSFETs of buck, inductor, and output capacitor should be as close to each other as possible to reduce the radiation of EMI due to the high-frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered. Place the input capacitor near the drain of high-side MOSFET. In multi-layer PCB, use one layer as power ground and have a separate control signal ground as the reference for all signals. To avoid the signal ground being affected by noise and to achieve the best load regulation, it should be connected to the ground terminal of output.

Follow the below guidelines for best performance:

- A two-layer printed circuit board is recommended.
- Use the bottom layer of the PCB as a ground plane and make all critical component ground connections through vias to this layer.
- Keep the metal running from the CLNx terminal to the output inductor short.
- Use copper-filled polygons on the top (and bottom, if two-layer PCB) circuit layers for the CLN node.
- The small-signal wiring traces from the DLx and DHx pins to the MOSFET gates should be kept short and wide enough to easily handle the several amps of drive current.
- The critical, small-signal components include any bypass capacitors (SMD-type of capacitors applied at VCC and SSx/ENB pins), feedback components (resistor divider), and compensation components (between INx and COMPx pins). Position those components close to their pins with a local, clear, GND connection or directly to the ground plane.
- Place the bootstrap capacitor near the BSTx and CLNx pins.
- The resistor on the RT pin should be near this pin and the GND return should be short and kept away from the noisy MOSFET's GND (which is shorted together with IC's PGND pin to GND plane on back side of PCB).
- Place the compensation components close to the INx and COMPx pins.
- The feedback resistors for both regulators should be located as close as possible to the relevant INx pin with vias tied straight to the ground plane as required.
- Minimize the length of the connections between the input capacitors, CIN, and the power switchers (MOSFETs) by placing them nearby.
- Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible and make the GND returns short (from the source of lower MOSFET to V_{IN} capacitor GND).
- Position the output inductor and output capacitors between the upper MOSFET and lower MOSFET and the load.
- Keep AGND on the clearer plane and away from the noisy MOSFET GND.
- PGND should be short, together with MOSFET GND, then through vias to GND plane on the bottom of PCB.
- Prevent a spike on the CLN pin with a proper snubber circuit for CLN and GND.

Physical Dimensions

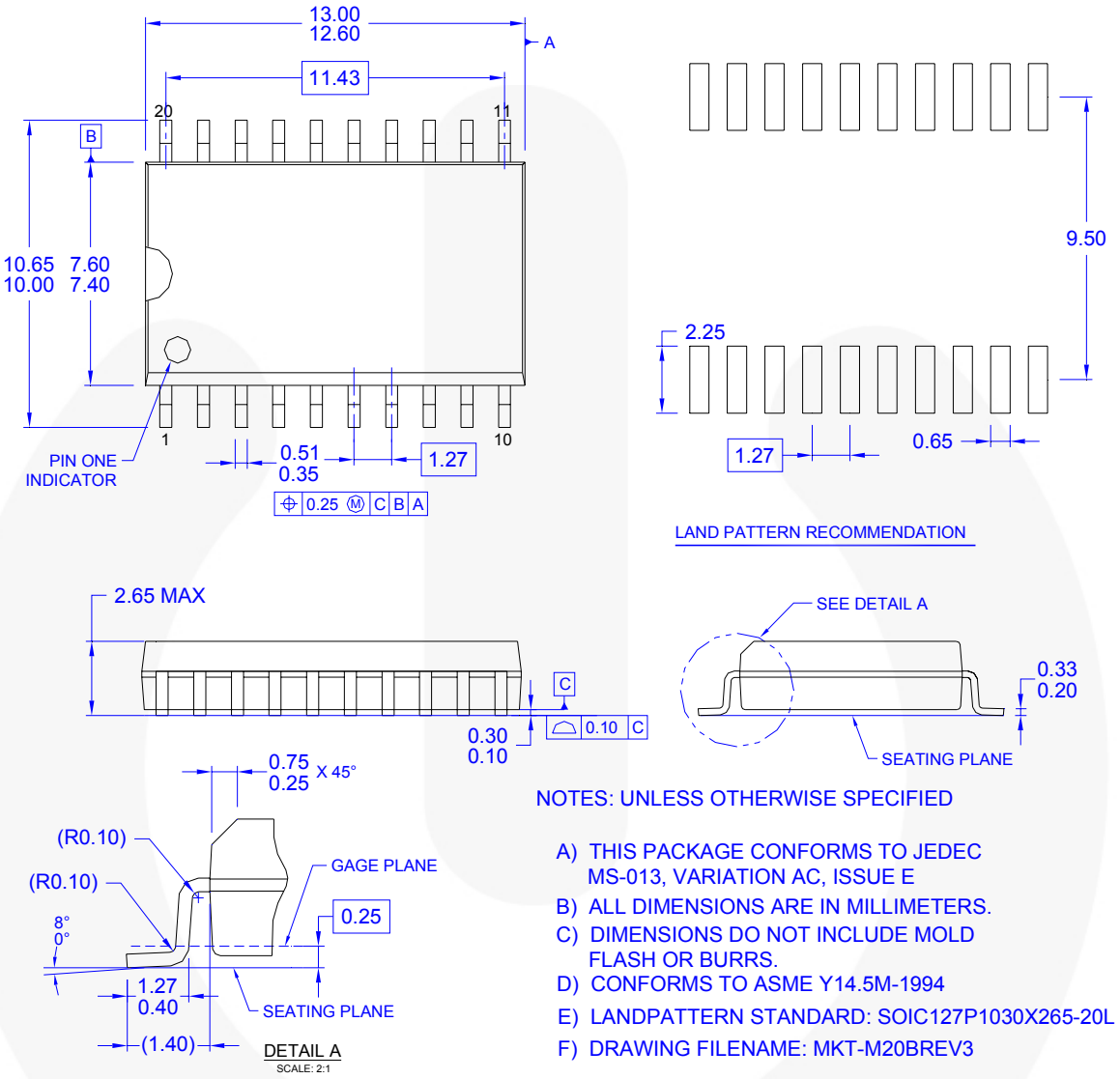


Figure 26. 20-Lead Small Outline Package (SOP)

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