CRYSTAL OSCILLATOR
PROGRAMMABLE

SG-8002LB series

- Frequency range : 1 MHz to 125 MHz
- Supply voltage : 3.3 V / 5.0 V
- Function : Output enable(OE) or Standby($\overline{ST}$)
- External dimensions : 5.0 × 3.2 × 1.2 t (mm)
- Short mass production lead time by PLL technology.
- SG-Writer available to purchase.
  Please contact Epson Toyocom or local sales representative.

Pb Free RoHS Compliant

Product Number (please contact us)
Q3323LBxxxxxx00

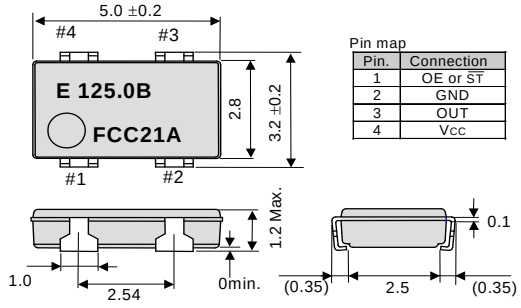
Actual size

Specifications (characteristics)

Item		Symbol	Specifications *2 PH / SH	Specifications *2 PC / SC	Remarks
Output frequency range		f_0	1 MHz to 80 MHz	—	V_{CC}=4.5 V to 5.5 V
			—	1 MHz to 125 MHz	V_{CC}=3.0 V to 3.6 V
			—	1 MHz to 66.7 MHz	V_{CC}=2.7 V to 3.6 V
Supply voltage		V_{CC}	4.5 V to 5.5 V	2.7 V to 3.6 V	
Temperature range	Storage temperature	T_stg	-40 °C to +125 °C		Store as bare product after unpacking
	Operating temperature	T_use	-20 °C to +70 °C (-40 °C to +85 °C)		Refer to "Outline specifications" (Frequency range)
Frequency tolerance		f_tol	B: ±50 × 10^{-6} ,C: ±100 × 10^{-6}		-20 °C to +70 °C
			M: ±100 × 10^{-6} *3		-40 °C to +85 °C
			L: ± 50 × 10^{-6}		-40 °C to +85 °C, V_{CC} ±5 % *3
Current consumption		I_{CC}	30 mA Max.	—	No load condition, f_0=80 MHz
			—	28 mA Max.	No load condition, f_0=125 MHz
Disable current		I_dis	25 mA Max.	—	P Type only, f_0=80 MHz
			—	16 mA Max.	P Type only, f_0=125 MHz
Stand-by current		I_std	50 µA Max.		S Type only, $\overline{ST}$ =GND
Symmetry *1		SYM	40 % to 60 %	—	50 % V_{CC}, L_CMOS=15 pF, ≤80 MHz
			45 % to 55 %	—	50 % V_{CC}, L_CMOS=25 pF, ≤50 MHz
			—	40 % to 60 %	50 % V_{CC}, L_CMOS=15 pF, V_{CC}=3.0 V to 3.6 V, ≤125 MHz
			—	40 % to 60 %	50 % V_{CC}, L_CMOS=15 pF, V_{CC}=2.7 V to 3.6 V, ≤66.7 MHz
			—	45 % to 55 %	50 % V_{CC}, L_CMOS=15 pF, V_{CC}=3.0 V to 3.6 V, ≤40 MHz
High output voltage		V_{OH}	V_{CC}-0.4 V Min.		I_{OH}=-16 mA(PH,SH),-8 mA(PC,SC)
Low output voltage		V_{OL}	0.4 V Max.		I_{OL}= 16 mA(PH,SH), 8 mA(PC,SC)
Output load condition(CMOS) *1		L_CMOS	15 pF Max.		Max. frequency and Max. supply voltage
Output enable / disable input voltage		V_{IH}	2.0 V Min.	70 % V_{CC} Min.	$\overline{ST}$ terminal or OE terminal
		V_{IL}	0.8 V Max.	20 % V_{CC} Max.	
Rise time / Fall time *1		t_r / t_f	3 ns Max.		20 % V_{CC} to 80 % V_{CC} level, L_CMOS=Max.
Start-up time		t_str	10 ms Max.		Time at minimum supply voltage to be 0 s
Frequency aging		f_aging	±5 × 10^{-6} / year Max.		+25 °C, Vcc=5.0 V/ 3.3 V (PC / SC) First year

*1 Operating temperature (-40 °C to +85 °C), the available frequency, symmetry and output load conditions, please refer to "Outline specifications" page.
*2 PLL-PLL connection & Jitter specification, please refer to "Jitter specifications and characteristics chart" page.
*3 PH,SH for "M" tolerance and "L" tolerance will be available up to 27 MHz. Checking possible by the Frequency checking program.

External dimensions (Unit:mm)



Pin map

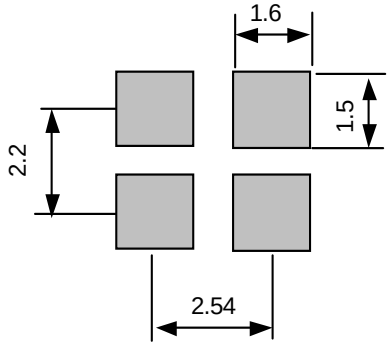
Pin.	Connection
1	OE or $\overline{ST}$
2	GND
3	OUT
4	Vcc

Note.
OE pin (PH, PC)
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.

$\overline{ST}$ pin (SH, SC)
$\overline{ST}$ pin = "H" or "open" : Specified frequency output.
$\overline{ST}$ pin = "L" : Output is low level (weak pull - down),oscillation stops.

Metal may be exposed on the top or bottom of this product.
This will not affect any quality, reliability or electrical spec.

Footprint (Recommended) (Unit:mm)



To maintain stable operation, provide by-pass capacitor with more than 0.1 µF at a location as near as possible to the power source terminal of the crystal products (between Vcc - GND).