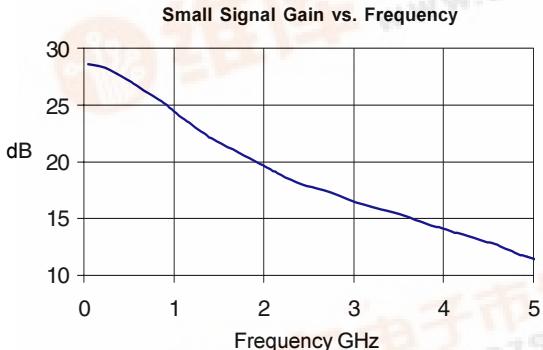


## Product Description

Stanford Microdevices' SGA-6589 is a high performance cascadeable 50-ohm amplifier. This RFIC uses the latest Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) process featuring 1 micron emitters with  $F_T$  up to 50 GHz.

This circuit uses a darlington pair topology with resistive feedback for broadband performance as well as stability over its entire temperature range. Internally matched to 50 ohm impedance, the SGA-6589 requires only DC blocking and bypass capacitors for external components.



## SGA-6589

### DC-4000 MHz Silicon Germanium HBT Cascadeable Gain Block



#### Product Features

- DC-4000 MHz Operation
- Single Voltage Supply
- High Output Intercept: +32.5 dBm typ. at 850 MHz
- High Output Power : 21.5 dBm typ. at 850 MHz
- High Gain : 25.6 dB typ. at 850 MHz

#### Applications

- Oscillator Amplifiers
- Final PA for Low Power Applications
- IF/ RF Buffer Amplifier
- Drivers for CATV Amplifiers

Symbol	Parameters: Test Conditions: $Z_0 = 50$ Ohms, $I_D = 80$ mA, $T = 25^\circ\text{C}$		Units	Min.	Typ.	Max.
$P_{1\text{dB}}$	Output Power at 1dB Compression	$f = 850$ MHz $f = 1950$ MHz $f = 2400$ MHz	dBm		21.5 19.0 17.8	
$IP_3$	Third Order Intercept Point Power out per tone = 0 dBm	$f = 850$ MHz $f = 1950$ MHz $f = 2400$ MHz	dBm		32.5 31.6 30.3	
$S_{21}$	Small Signal Gain	$f = 850$ MHz $f = 1950$ MHz $f = 2400$ MHz	dB		25.6 20.5 18.8	
Bandwidth	(Determined by $S_{11}$ , $S_{22}$ Values)		MHz		4000	
$S_{11}$	Input VSWR	$f = DC-4000$ MHz	-		1.60:1	
$S_{22}$	Output VSWR	$f = DC-4000$ MHz	-		1.80:1	
$S_{12}$	Reverse Isolation	$f = 850$ MHz $f = 1950$ MHz $f = 2400$ MHz	dB		28.7 24.3 22.9	
NF	Noise Figure, $Z_s = 50$ Ohms	$f = 1950$ MHz	dB		2.9	
$V_D$	Device Voltage		V		4.8	
$R_{thJ}$	Thermal Resistance (junction - lead)		°C/W		97	

The information provided herein is believed to be reliable at press time. Stanford MicroDevices assumes no responsibility for inaccuracies or omissions.

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### Absolute Maximum Ratings

Operation of this device above any one of these parameters may cause permanent damage.

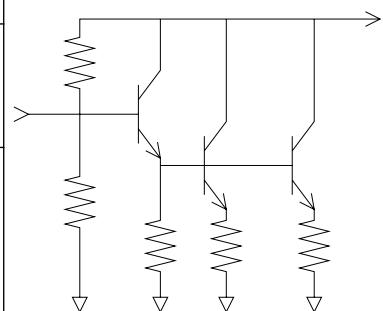
Bias Conditions should also satisfy the following expression:

$$I_D V_D (\text{max}) < (T_J - T_{OP}) / R_{th, j-l}$$

Parameter	Value	Unit
Supply Current	160	mA
Operating Temperature	-40 to +85	C
Maximum Input Power	+10	dBm
Storage Temperature Range	-40 to +150	C
Operating Junction Temperature	+150	C

### Key parameters, at typical operating frequencies:

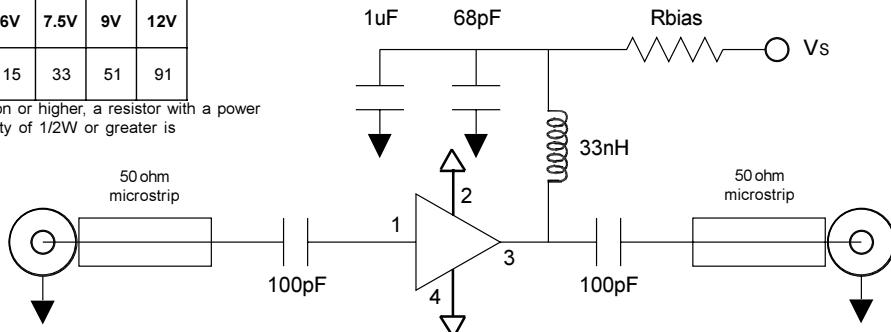
Parameter	Typical		Test Condition ( $I_D = 80$ mA, unless otherwise noted)
	25°C	Unit	
<b>500 MHz</b>			
Gain	27.4	dB	
Noise Figure	2.5	dB	$Z_s = 50$ Ohms
Output IP3	32.1	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	21.6	dBm	
Input Return Loss	13.8	dB	
Isolation	29.9	dB	
<b>850 MHz</b>			
Gain	25.6	dB	
Noise Figure	2.5	dB	$Z_s = 50$ Ohms
Output IP3	32.5	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	21.5	dBm	
Input Return Loss	15.7	dB	
Isolation	28.7	dB	
<b>1950 MHz</b>			
Gain	20.5	dB	
Noise Figure	2.9	dB	$Z_s = 50$ Ohms
Output IP3	31.6	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	19.0	dBm	
Input Return Loss	14.0	dB	
Isolation	24.3	dB	
<b>2400 MHz</b>			
Gain	18.8	dB	
Noise Figure	3.3	dB	$Z_s = 50$ Ohms
Output IP3	30.3	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	17.8	dBm	
Input Return Loss	12.5	dB	
Isolation	22.9	dB	

Pin #	Function	Description	Device Schematic
1	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.	
2	GND	Connection to ground. Use via holes for best performance to reduce lead inductance. Place vias as close to ground leads as possible.	
3	RF OUT/Vcc	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.	
4	GND	Same as Pin 2.	

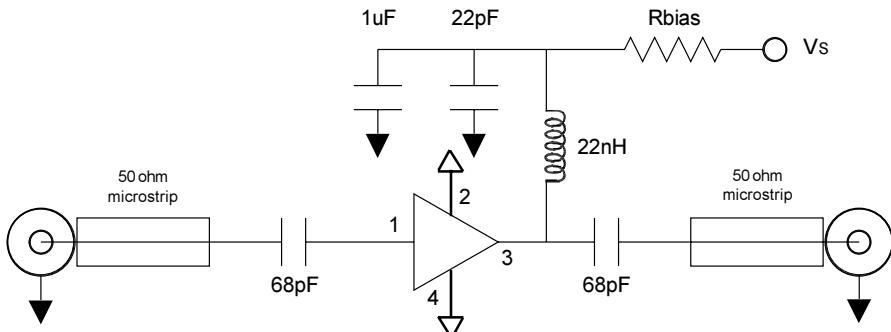
### Application Schematic for Operation at 850 MHz

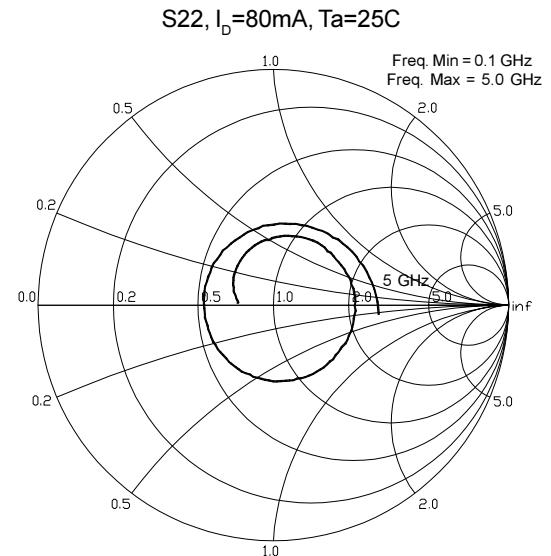
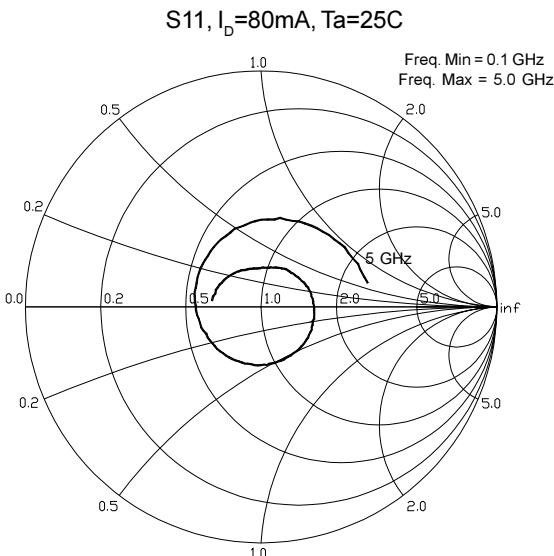
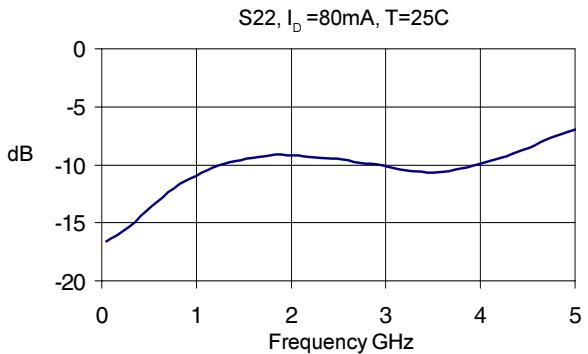
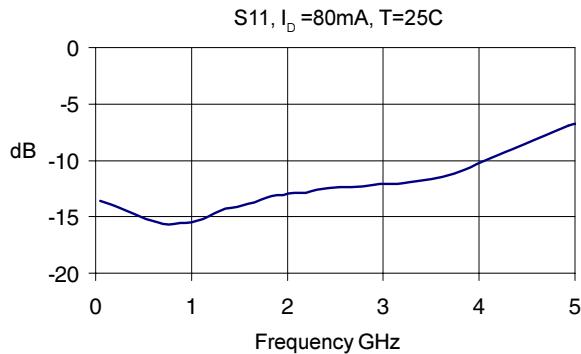
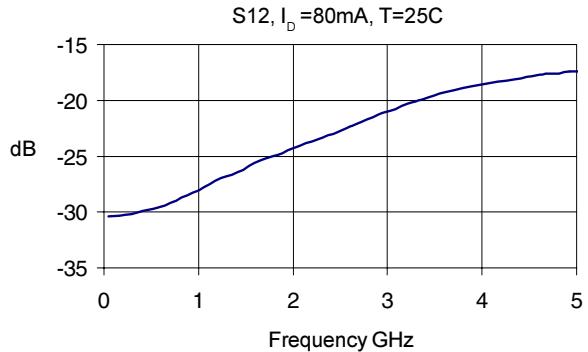
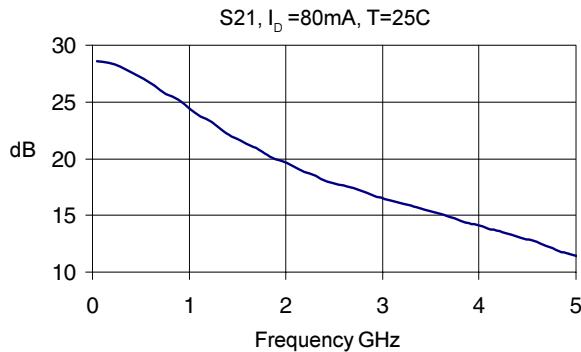
Recommended Bias Resistor Values				
Supply Voltage(Vs)	6V	7.5V	9V	12V
Rbias (Ohms)	15	33	51	91

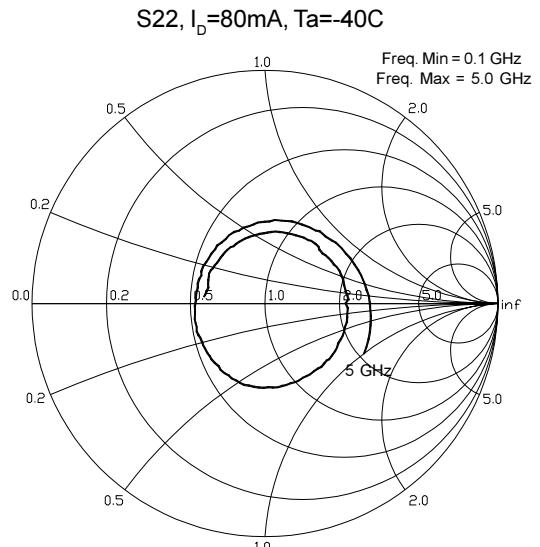
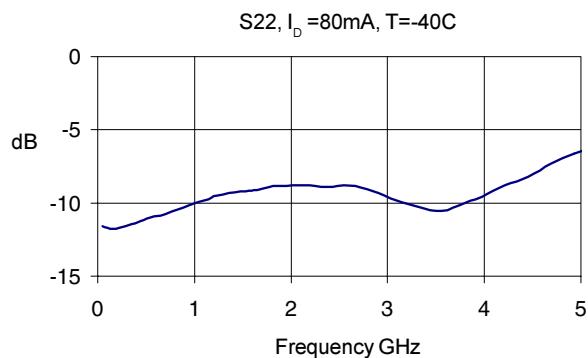
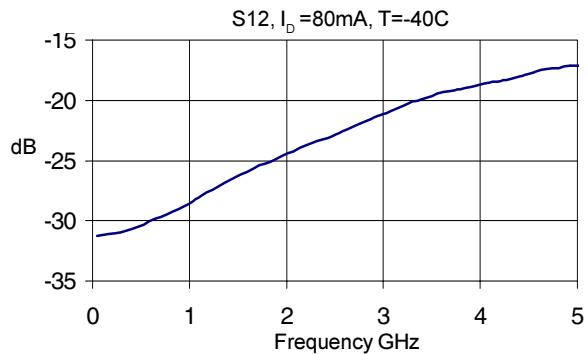
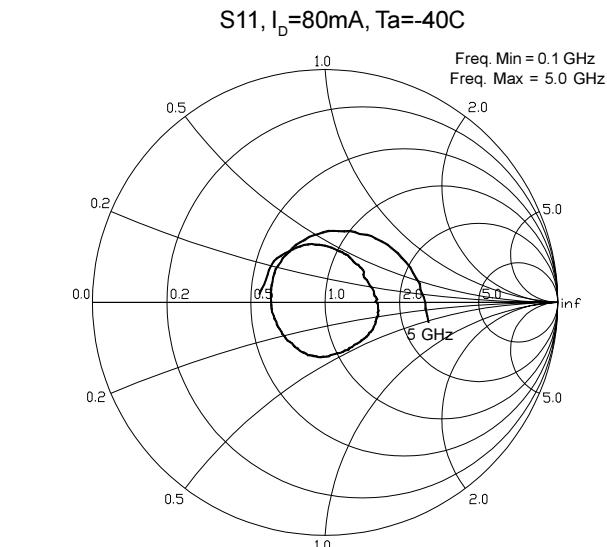
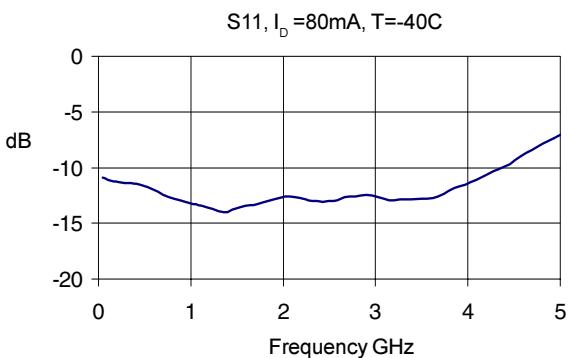
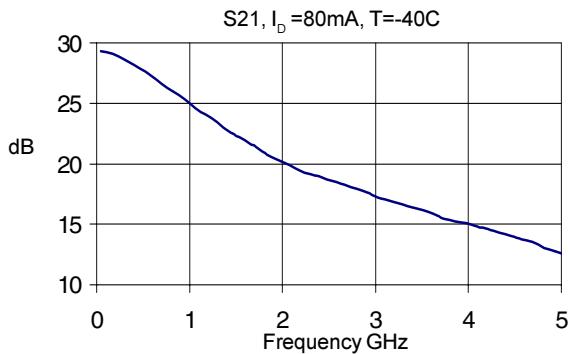
For 7.5V operation or higher, a resistor with a power handling capability of 1/2W or greater is recommended.

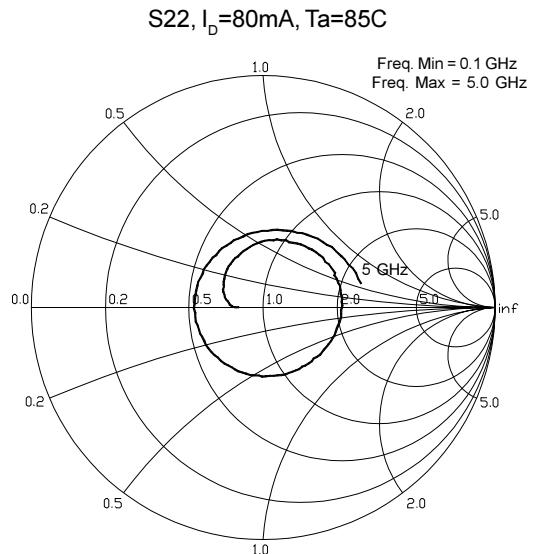
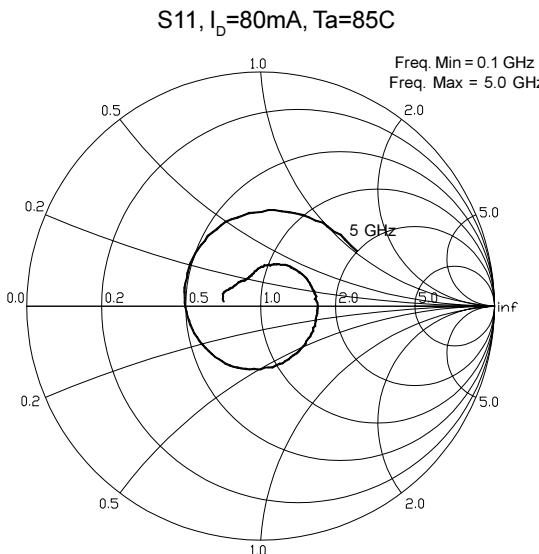
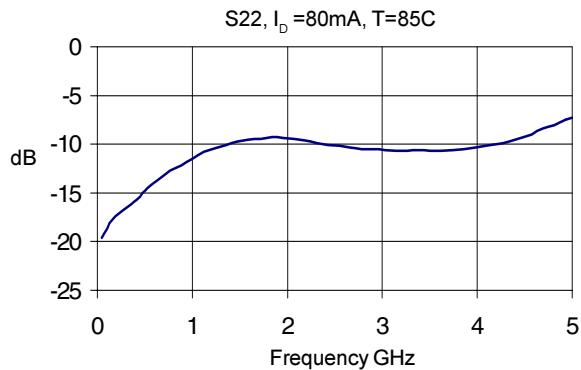
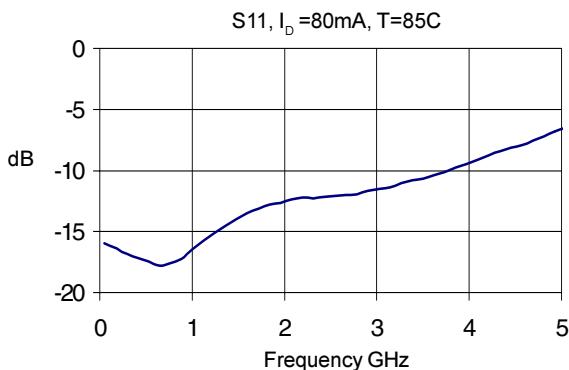
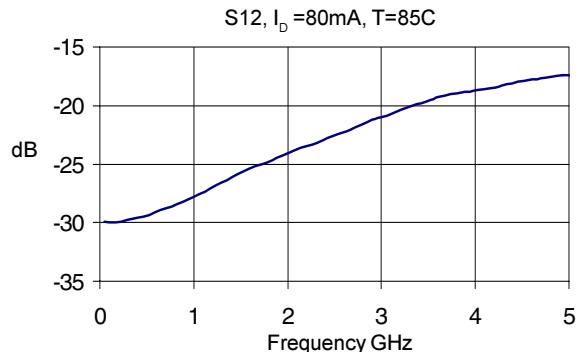
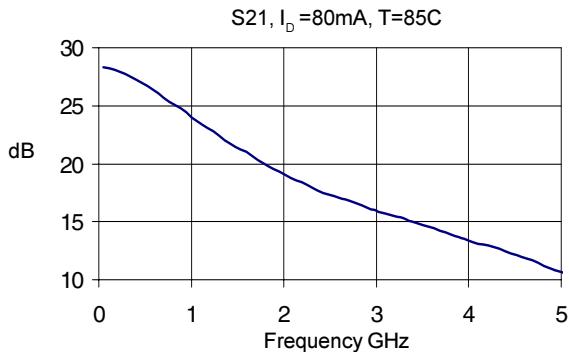


### Application Schematic for Operation at 1950 MHz



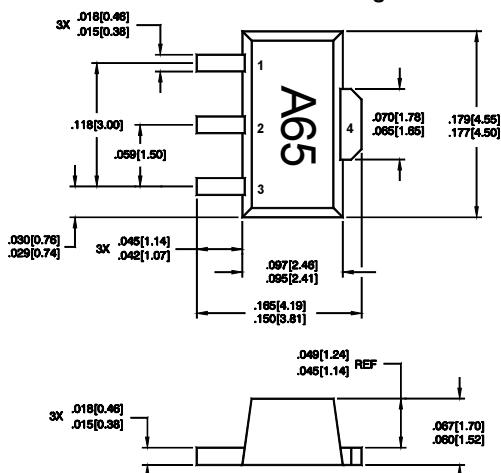




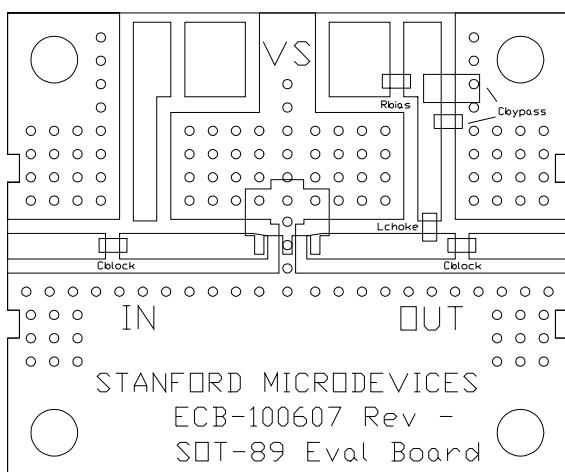



**Caution: ESD Sensitive**

Appropriate precautions in handling, packaging and testing devices must be observed.

**Package Dimensions**
**Outline Drawing**

**DIMENSIONS ARE IN INCHES [MM]**

Pin assignments shown for reference only, not marked on part


**Part Number Ordering Information**

Part Number	Reel Size	Devices/Reel
SGA-6589	13"	3000

**Part Symbolization**

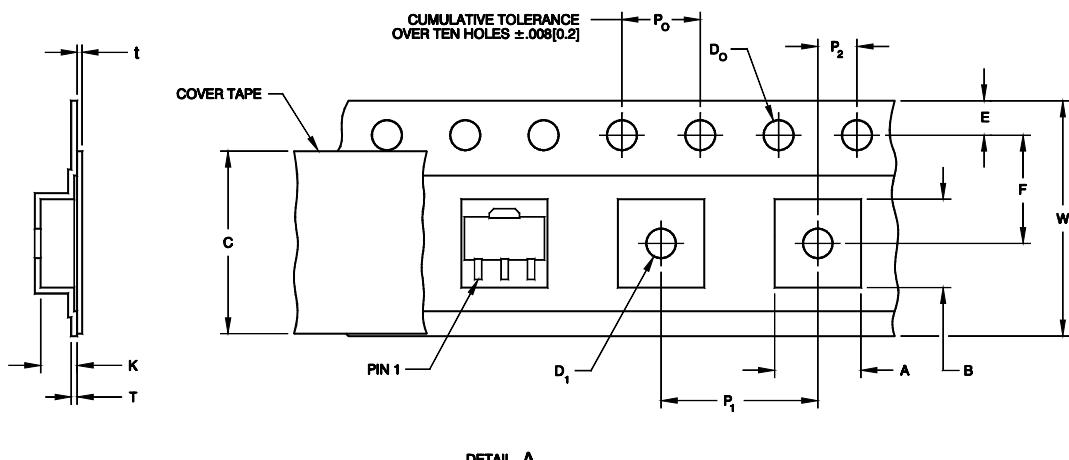
The part will be symbolized with an "A65" designator on the top surface of the package.

**PCB Pad Layout**

## Component Tape and Reel Packaging

## Tape Dimensions

For 89 Outline



DETAIL A

Description		Symbol	Size (mm)
Cavity	Length	A	4.91 +/- 0.01
	Width	B	4.52 +/- 0.01
	Depth	K	1.90 +/- 0.01
	Pitch	P <sub>1</sub>	8.00 +/- 0.01
	Bottom Hole Diameter	D <sub>1</sub>	1.60 +/- 0.10
Perforation	Diameter	D <sub>0</sub>	1.55 +/- 0.05
	Pitch	P <sub>0</sub>	4.00 +/- 0.01
	Position	E	1.75 +/- 0.01
Cover Tape	Width	C	9.10 +/- 0.25
	Tape Thickness	t	0.05 +/- 0.01
Carrier Tape	Width	W	12.0 +/- 0.03
	Thickness	T	0.30 +/- 0.05
Distance	Cavity to Perforation (Width Direction)	F	5.50 +/- 0.10
	Cavity to Perforation (Length Direction)	P <sub>2</sub>	2.00 +/- 0.10