

N-Channel 200-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
200	0.240 at V _{GS} = 10 V	2.2		
	0.260 at V _{GS} = 6.0 V	2.1		

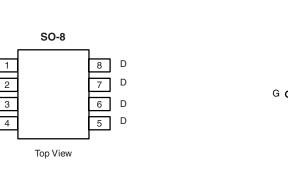
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- PWM Optimized for Low $\mathbf{Q}_{\mathbf{g}}$ and Low $\mathbf{R}_{\mathbf{g}}$
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

Primary Side Switch



Ordering Information: Si4464DY-T1-E3 (Lead (Pb)-free)

S

Si4464DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T	_A = 25 °C, unle	ss otherwise r	noted		
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	200		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current /T 150 °C\a	T _A = 25 °C	- I _D	2.2	1.7	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		1.7	1.3	^
Pulsed Drain Current		I _{DM}	8		Α
Single Avalanch Current	L = 0.1 mH	I _{AS}	;	3	
Single Avalanch Energy	L = 0.111111	E _{AS}	0.	45	mJ
Continuous Source Current (Diode Conduction) ^a	I _S	2.1	1.2	Α	
Mariana Baran Biraha Kad	T _A = 25 °C	P _D	2.5	1.5	W
Maximum Power Dissipation ^a	T _A = 70 °C] ' ⁻ D	1.6	0.9	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 t	o 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manipular landing to Austriant	t ≤ 10 s	R _{thJA}	37	50	
Maximum Junction-to-Ambient ^a	Steady State	' ¹thJA	68	85	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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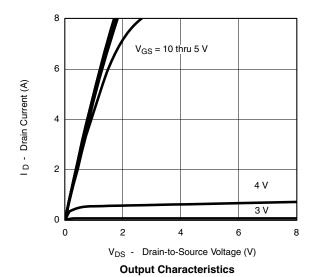
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Drain Current		V _{DS} = 200 V, V _{GS} = 0 V		1			
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 200 V, V_{GS} = 0 V, T_{J} = 55 °C			5	μΑ	
On-State Drain Current ^a	State Drain Current ^a $I_{D(on)}$ $V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$		8			Α	
	В	$V_{GS} = 10 \text{ V}, I_D = 2.2 \text{ A}$		0.195	0.240	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 6.0 \text{ V}, I_D = 2.1 \text{ A}$		0.210	0.260	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 2.2 \text{ A}$		8.0		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 2.1 A, V _{GS} = 0 V		0.8	1.2	V	
Dynamic ^b			"	•			
Total Gate Charge	Q_g			12	18		
Gate-Source Charge	Q_{gs}	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2.2 \text{ A}$		2.5		nC	
Gate-Drain Charge	Q_{gd}			3.8			
Gate Resistance	R_g			2.5		Ω	
Turn-On Delay Time	t _{d(on)}			10	15		
Rise Time	t _r	V_{DD} = 100 V, R_L = 100 Ω		12	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		15	25	ns	
Fall Time	t _f			15	25		
Source-Drain Reverse Recovery Time t _{rr}		I _F = 2.1 A, dI/dt = 100 A/μs		60	90		

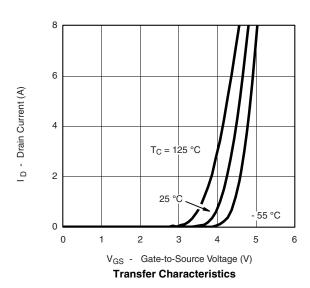
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



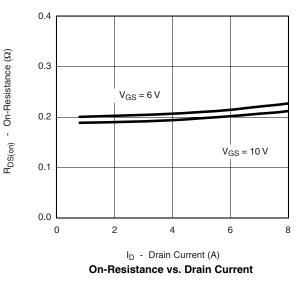


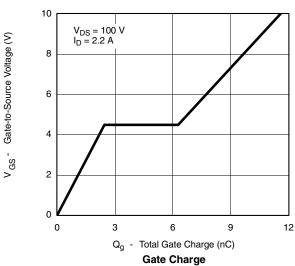


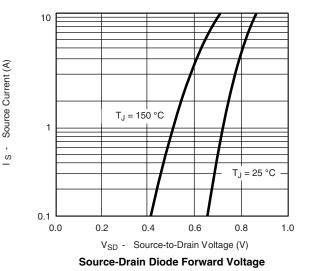


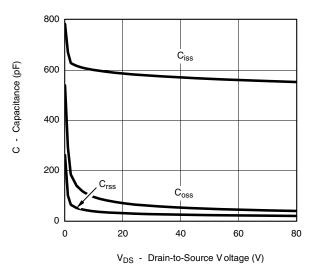


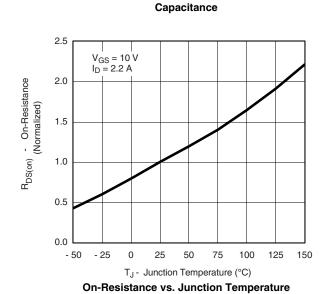
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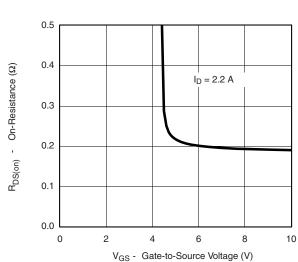










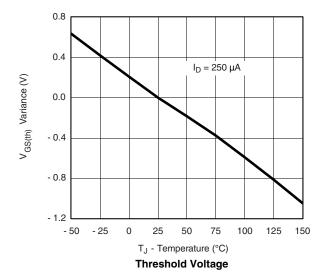


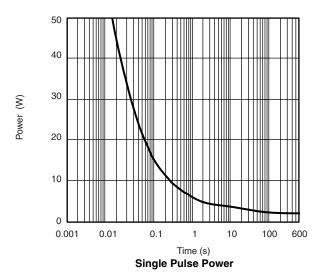
On-Resistance vs. Gate-to-Source Voltage

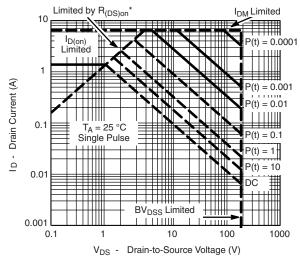
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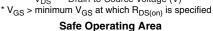
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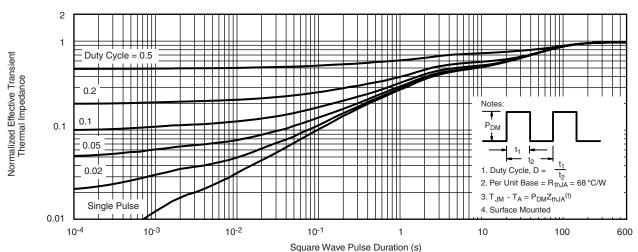
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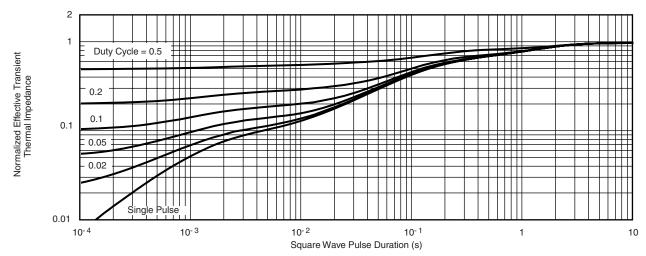








TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg272051.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

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