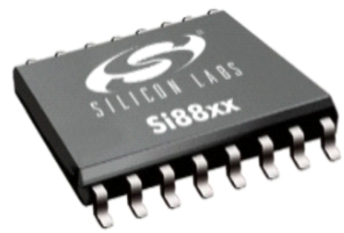
Si88x4x

QUAD DIGITAL ISOLATORS WITH DC-DC CONVERTER

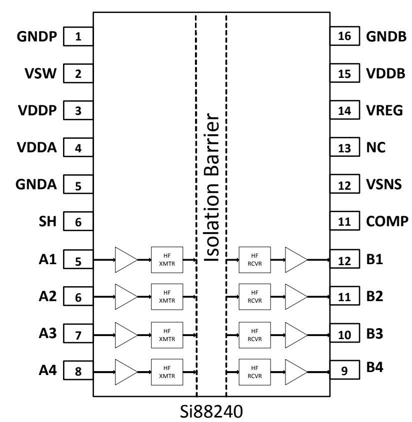
Features

- High-speed isolators with integrated dc-dc converter
- Fully-integrated secondary sensing feedback-controlled converter with dithering for low EMI
- dc-dc converter efficiency of 78%
- Up to 2 W isolated power with integrated power switches
- Options include dc-dc shutdown, frequency control, and soft start
- Conversion
  - 3/5 V to isolated 3/5 V
  - 24 V to isolated 3/5 V supported
- Precise timing on digital isolators
  - 0–100 Mbps
  - 18 ns typical prop delay
- Highly-reliable: 100 year lifetime
- High electro-magnetic immunity and ultra-low emissions
- RoHS compliant packages
  - SOIC-20 wide body
- Isolation of up to 5000 Vrms
- High transient immunity of 100 kV/µs (typical)
- AEC-Q100 qualified
- Wide temp range
  - –40 to +125 °C



Ordering Information:
See page 36.

Pin Assignments
See page 31



Patents pending

Applications

- Industrial automation systems
- Hybrid electric and electric vehicles
- Isolated power supplies
- Inverters
- Data acquisition
- Motor control
- PLCs, distributed control systems

Safety Approval (Pending)

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE 0884-10)
- EN 60950-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1

Description

The Si88xx integrates Silicon Labs' proven digital isolator technology with an on-chip isolated dc-dc converter that provides regulated output voltages of 3.3 or 5.0 V (or >5 V with external components) at peak output power levels of up-to 2 W. These devices provide up-to four digital channels. The dc-dc converter has user-adjustable frequency for minimizing emissions, a soft-start function for safety, a shut-down option and loop compensation. The device requires only minimal passive components and a miniature transformer.

The ultra-low-power digital isolation channels offer substantial data-rate, propagation delay, size and reliability advantages over legacy isolation technologies. Data rates up to 100 Mbps are supported, and all devices achieve propagation delays of only 23 ns. Ordering options include a choice of dc-dc converter features, isolation channel configurations and a fail-safe mode. All products are certified by UL, CSA, VDE, and CQC.

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

Table of Contents

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	–40	25	125	°C
Power Input Voltage	VDDP	3.0	—	5.5	V
Supply Voltage	VDDA	3.0	—	5.5	V
	VDDB	3.0	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Electrical Characteristics[1]

VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC/DC Converter						
Switching Frequency Si882xx, Si884xx	FSW			250		kHz
Switching Frequency Si883xx, Si886xx only	FSW	R_{fsw} = 23.3 kΩ FSW = 1025.5/(R_{FSW} x C_{SS}) C_{SS} = 220 nF (see Figure 3) (1% tolerance on BOM)	180	200	220	kHz
		R_{fsw} = 5.18 kΩ, C_{SS} = 220 nF (see Figure 3)	810	900	990	kHz
VSNS voltage	VSNS(V)	ILOAD = 0	1.002	1.05	1.097	V
VSNS current offset	I_{offset}		–500	—	500	nA
Output Voltage Accuracy[2]		See Figure 2 ILOAD = 0 mA	–5	—	+5	%
Line Regulation	ΔVOUT(line)/ΔVDDP	See Figure 2 ILOAD = 50 mA VDDP varies from 4.5 to 5.5 V		1		mV/V

Notes:
1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Load Regulation	ΔVOUT(load)/VOUT	See Figure 2 ILOAD = 50 to 400 mA		0.1		%
Output Voltage Ripple		See Figure 2 COUT = 0.1 µF in parallel with 10 µF, ILOAD = 100 mA		100		mV p-p
Turn-on overshoot	ΔVOUT(start)	See Figure 2 CIN = COUT = 0.1 µF in parallel with 10 µF, ILOAD = 0 A CSS = 220 nF, for Si883xx/Si886xx		2		%
Continuous Output Current 5.0 V to 5.0 V 3.3 V to 3.3 V 3.3 V to 5.0 V 5.0 V to 3.3 V	ILOAD(max)	See Figure 2		 400 400 250 550		mA
Cycle-by-cycle average current limit	ILIM	See Figure 2 Output short circuited		3		A
No Load Supply Current IDDP Si882xx, Si883xx	IDDPQ_DCDC[3]	See Figure 2 VDDP = VDDA = 5 V		30		mA
No Load Supply Current IDDA Si882xx, Si883xx	IDDAQ_DCDC[4]	See Figure 2 VDDP = VDDA = 5 V		5.7		mA
No Load Supply Current IDDP Si884xx, Si886xx	IDDPQ_DCDC[4]	See Figure 2 VIN = 24 V		0.8		mA
No Load Supply Current IDDA Si884xx, Si886xx	IDDAQ_DCDC[4]	See Figure 2 VIN = 24 V		5.8		mA
Peak Efficiency	η	See Figure 2		78		%

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)
VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage Regulator Voltage Si884xx, Si886xx	VREGA, VREGB	IDD = 600 µA See Figure 26 for typical I–V curve		4.8		V
VREG tempco	K_{TVREG}			–0.43		mV/°C
VREG input current	I_{REG}		350	—	950	µA
Start-up Time from power-up: internal FET only	tSU			40		ms
Restart Time from fault event	tOTP			21		s
Digital Isolator						
VDD Undervoltage Threshold	VDDUV+	VDDA, VDDB rising		2.7		V
VDD Undervoltage Threshold	VDDUV–	VDDA, VDDB falling		2.6		V
VDD Undervoltage Hysteresis	VDD_{HYS}			100		mV
Positive-Going Input Threshold	VT+	All inputs rising		1.67		V
Negative-Going Input Threshold	VT–	All inputs falling		1.23		V
Input Hysteresis	V_{HYS}			0.44		V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DDA}, V_{DDB} – 0.4	—	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	—	0.4	V
Input Leakage Current	I_L		—	—	±10	µA

Notes:
1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Impedance	Z_O		—	50	—	Ω
Supply Current, CL = 15 pF						
DC, VDDx = 3.3 V ± 10%						
Si88x40 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 12.9 5.4 5.1 5.3		 mA
Si88x41 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 10.9 6.8 5.6 5.1		 mA
Si88x42 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 9.7 7.8 5.9 4.3		 mA
Si88x43 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 8.5 9.3 6.5 3.9		 mA
Si88x44 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 6.6 10.6 6.5 3.6		mA
1 Mbps, VDDx = 3.3 V ± 10% (All Inputs = 500 kHz Square Wave, CL = 15 pF)						
Si88x40 V_{DDA} V_{DDB}			 — —	 8.9 5.4		mA

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si88x41 V_{DDA} V_{DDB}			 — —	 8.3 6.0		mA
Si88x42 V_{DDA} V_{DDB}			 — —	 7.9 6.1		mA
Si88x43 V_{DDA} V_{DDB}			 — —	 7.6 6.7		mA
Si88x44 V_{DDA} V_{DDB}			 — —	 6.7 7.1		mA
100 Mbps, VDDx = 3.3 V ± 10% (All Inputs = 50 MHz Square Wave, CL = 15 pF)						
Si88x40 V_{DDA} V_{DDB}			 — —	 8.7 19.2		mA
Si88x41 V_{DDA} V_{DDB}			 — —	 12.7 16.6		mA
Si88x42 V_{DDA} V_{DDB}			 — —	 15.6 13.6		mA
Si88x43 V_{DDA} V_{DDB}			 — —	 18.7 11.0		mA
Si88x44 V_{DDA} V_{DDB}			 — —	 21.6 6.9		mA

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)
VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC, VDDx = 5 V ± 10%						
Si88x40 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 13.1 5.6 5.2 5.4		 mA
Si88x41 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 11.1 6.9 5.7 5.2		 mA
Si88x42 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 10.1 7.9 6.2 4.4		 mA
Si88x43 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 8.6 9.2 6.6 3.9		 mA
Si88x44 V_{DDA} V_{DDB} V_{DDA} V_{DDB}		 V_I = 0 V_I = 0 V_I = 1 V_I = 1	 — — — —	 6.8 11.0 6.7 3.8		 mA
1 Mbps, VDDx = 5 V ± 10% (All Inputs = 500 kHz Square Wave, CL = 15 pF)						
Si88x40 V_{DDA} V_{DDB}			 — —	 9.1 5.8		mA

Notes:
1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si88x41 V_{DDA} V_{DDB}			 — —	 8.4 6.3		mA
Si88x42 V_{DDA} V_{DDB}			 — —	 8.2 6.2		mA
Si88x43 V_{DDA} V_{DDB}			 — —	 7.8 6.7		mA
Si88x44 V_{DDA} V_{DDB}			 — —	 6.9 7.4		mA
100 Mbps, VDDx = 5 V ± 10% (All Inputs = 50 MHz Square Wave, CL = 15 pF)						
Si88x40 V_{DDA} V_{DDB}			 — —	 8.2 26.2		mA
Si88x41 V_{DDA} V_{DDB}			 — —	 14.7 22.0		mA
Si88x42 V_{DDA} V_{DDB}			 — —	 18.9 16.5		mA
Si88x43 V_{DDA} V_{DDB}			 — —	 24.0 11.7		mA
Si88x44 V_{DDA} V_{DDB}				 28.1 6.6		mA
Timing Characteristics						
Data Rate			0	—	100	Mbps
Minimum Pulse Width			10	—	—	ns

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)
VDDA = VDDP = 3.0 V – 5.5 V, T_A = –40 to 125 °C, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t_{PHL}	See Figure 1 VDDx = 3.3 V		17.8		ns
Propagation Delay	t_{PLH}	See Figure 1 VDDx = 3.3 V		14.5		ns
Propagation Delay	t_{PHL}	See Figure 1 VDDx = 5.0 V		17.5		ns
Propagation Delay	t_{PLH}	See Figure 1 VDDx = 5.0 V		12.6		ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1 VDDx = 3.3 V		3.4		ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1 VDDx = 5.0 V		4.8		ns
Propagation Delay Skew[6]	$t_{PSK(P-P)}$			2.0		ns
Channel-Channel Skew	t_{PSK}		—	1.0		ns
Output Rise Time	t_r	C_L = 15 pF		2.5		ns
Output Fall Time	t_f	C_L = 15 pF		2.5		ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V V_{CM} = 1500 V	40	100		kV/µs
Startup Time[7]	t_{SU}			55		µs

Notes:
1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS(V) x (1 + R5/R6) + R5 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
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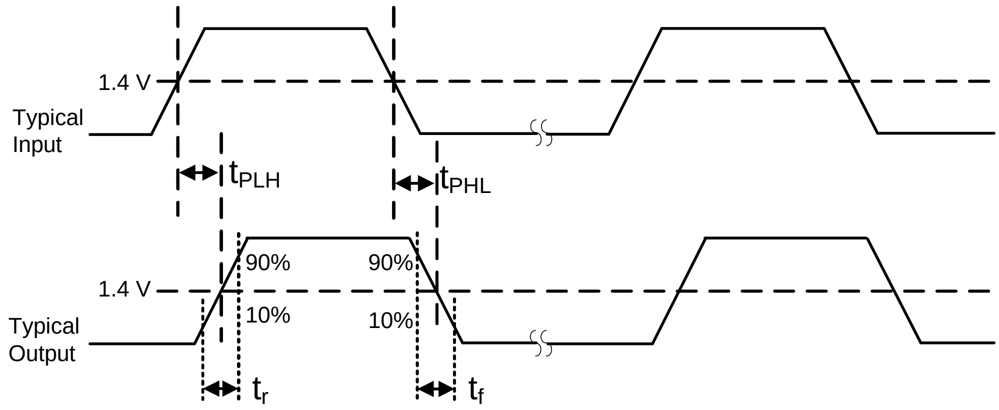

Figure 1. Propagation Delay Timing for Digital Channels

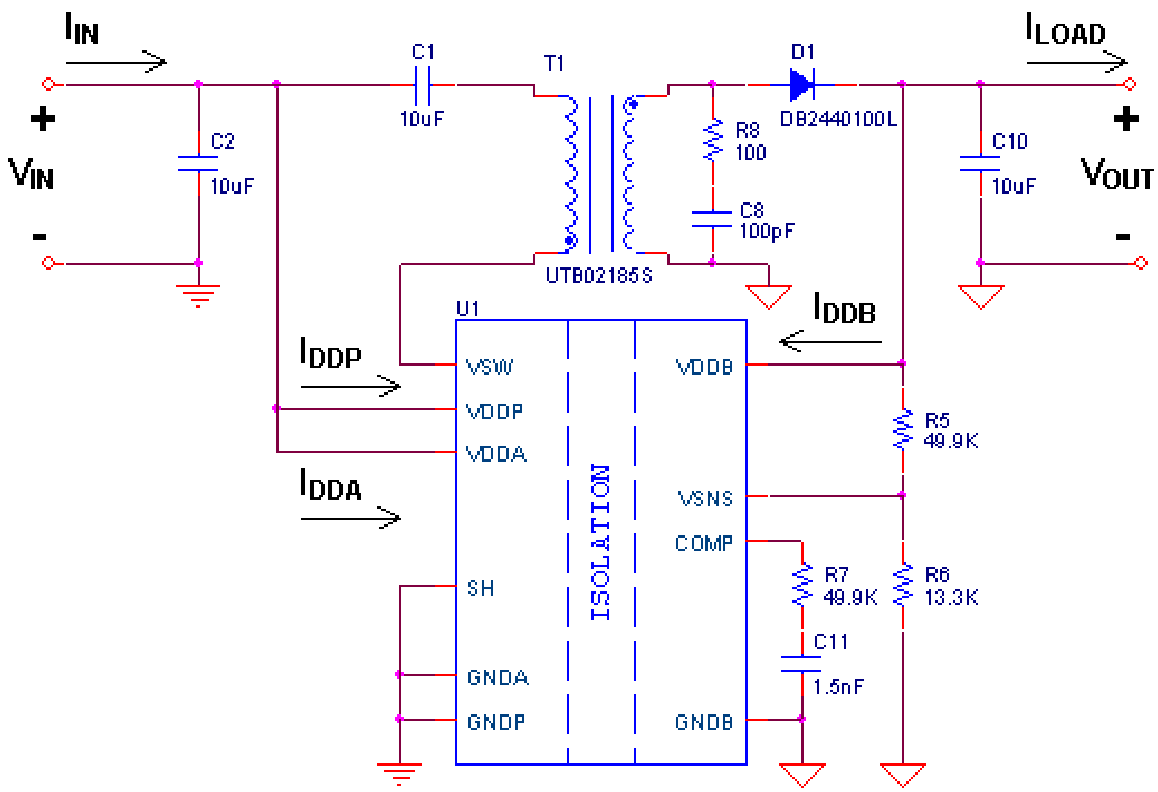

Figure 2. Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx

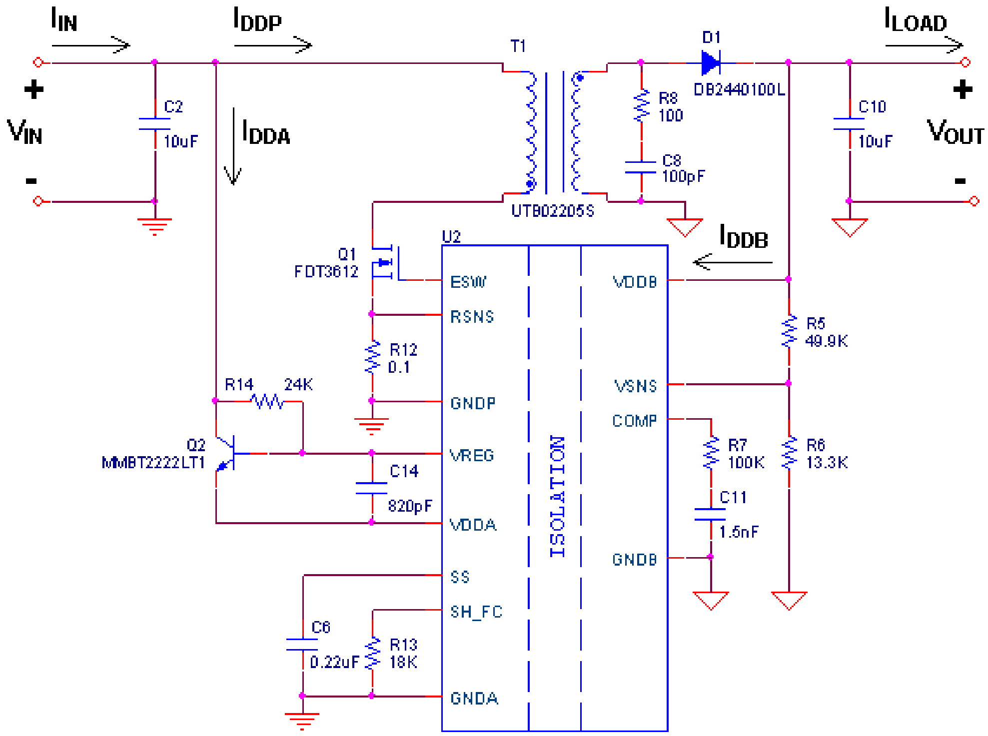

Figure 3. Measurement Circuit for Converter Efficiency and Regulation for Si884xx, Si886xx

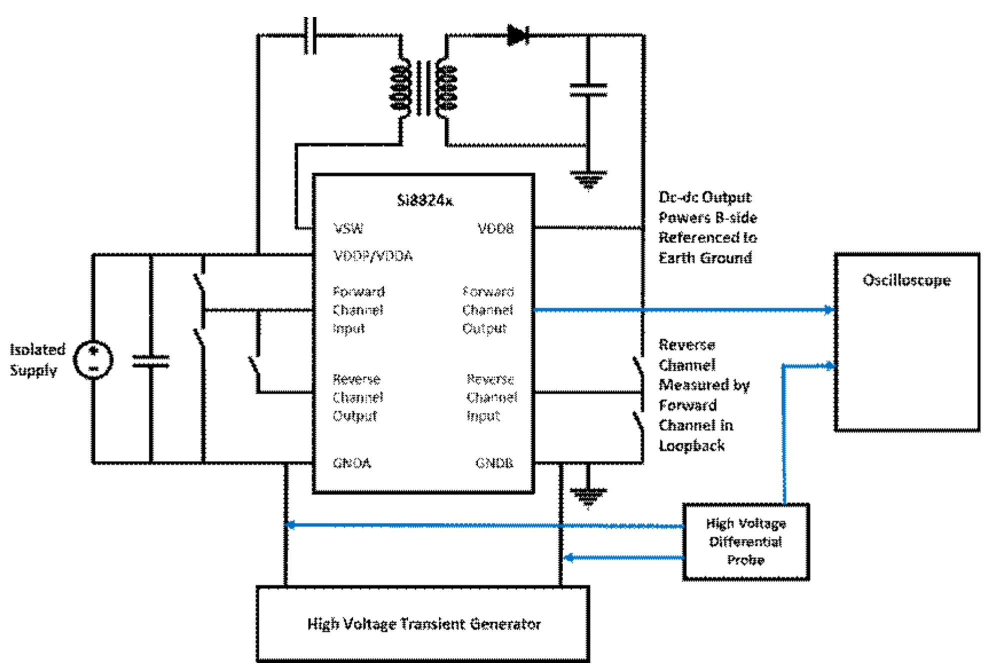

Figure 4. Common-Mode Transient Immunity Test Circuit

Table 3. Regulatory Information[1,2]

CSA
The Si88xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si88xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 891 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si88xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si88xx is certified under GB4943.1-2011. For more details, see File V2012CQC001041.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Notes: 1. Regulatory Certifications apply to 5 kVRMS rated devices which are production tested to 6.0 kVRMS for 1 sec. 2. All certifications are pending.

Table 4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			WB SOIC	
Nominal Air Gap (Clearance)	L(1O1)		7.6	mm
Nominal External Tracking (Creepage)	L(1O2)		7.6	mm
Minimum Internal Gap (Internal Clearance)			0.014	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	1.4	pF
Input Capacitance[2]	C_I		4.0	pF

Notes:

1. To determine resistance and capacitance, the Si88xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input to ground.

Table 5. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Condition	Specification
		WB SOIC
Basic Isolation Group	Material Group	I
Installation Classification	Rate Mains Voltages ≤150 V_{RMS}	I–IV
	Rate Mains Voltages ≤300 V_{RMS}	I–IV
	Rate Mains Voltages ≤400 V_{RMS}	I–III
	Rate Mains Voltages ≤600 V_{RMS}	I–III

Table 6. IEC 60747-5-2 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic	Unit
			WB SOIC	
Maximum Working Insulation Voltage	V_{IORM}		891	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si88xx provides a climate classification of 40/125/21.

Table 7. IEC Safety Limiting Values*

Parameter	Symbol	Test Condition	WB SOIC-20	Unit
Case Temperature	T_S		150	°C
Safety Input Current	I_S	θ_{JA} = 55 °C/W (WB SOIC-20), V_{DDI} = 5.5 V, T_J = 150 °C, T_A = 25 °C	413	mA
Device Power Dissipation	P_D		2.27	W

***Note:** Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 3.

Table 8. Thermal Characteristics

Parameter	Symbol	WB SOIC-20	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	55	°C/W

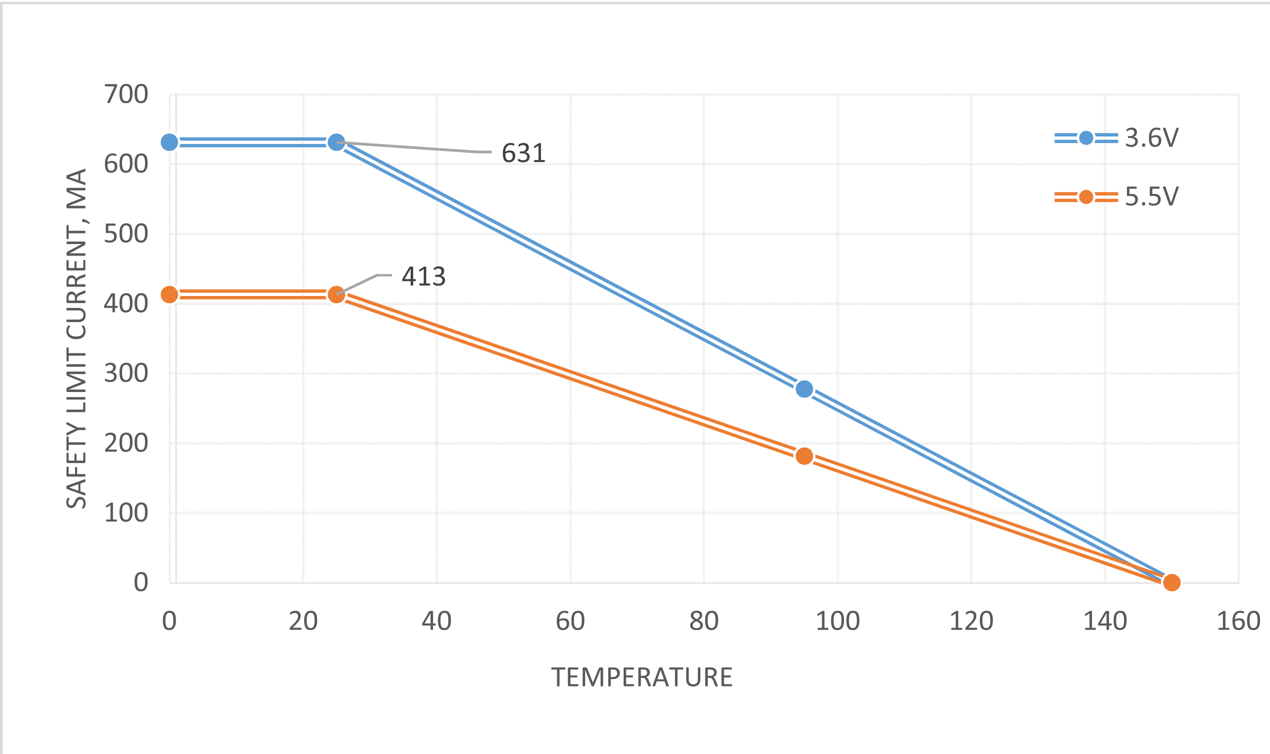

Figure 5. WB SOIC-20 Thermal Derating Curve*

***Note:** Values are not final and are subject to change. Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 9. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Ambient Temperature under Bias	T_A	–40	+125	°C
Junction Temperature	T_J	—	+150	°C
Input-side Supply Voltage	VDDA VDDP	–0.6	6.0	V
Output supply	VDDB	–0.6	6.0	V
Voltage on any Pin with respect to Ground	VIN	–0.5	VDD + 0.5	V
Output Drive Current per Channel	I_O		10	mA
Input Current for VREGA, VREGB	I_{REG}	—	1	mA
Lead Solder Temperature (10 s)		—	260	°C
ESD per AEC-Q100	HBM	—	4	kV
	CDM	—	2	kV
Maximum Isolation (Input to Output) (1 sec) WB SOIC-20, WB SOIC-24		—	6500	V_{RMS}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from –40 to 150 °C.

2. Functional Description

2.1. Theory of Operation

The Si88xx family of products is capable of transmitting and receiving digital data signals from an isolated power domain to a local system power domain with up to 5 kV of isolation. Each part has four unidirectional digital isolation channels. In addition, Si88xx products include an integrated controller and switches for a dc-dc converter which regulates output voltage by sensing it on the isolated side.

2.2. Digital Isolation

The operation of an Si88xx digital channel is analogous to that of a digital buffer, except an RF carrier transmits data across the isolation barrier. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si88xx channel is shown in Figure 6.

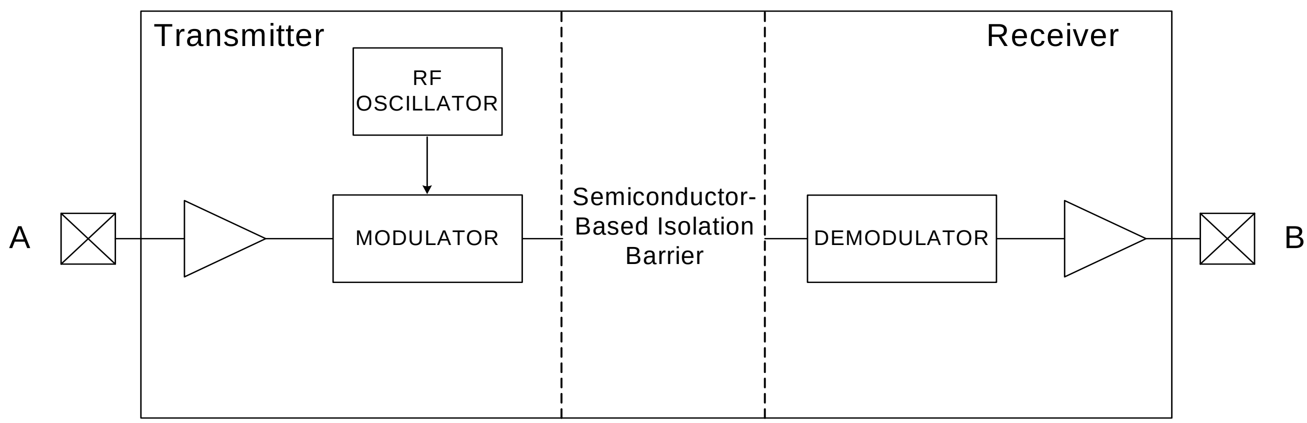

Figure 6. Simplified Si88xx Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a silicon dioxide capacitive isolation barrier. In the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

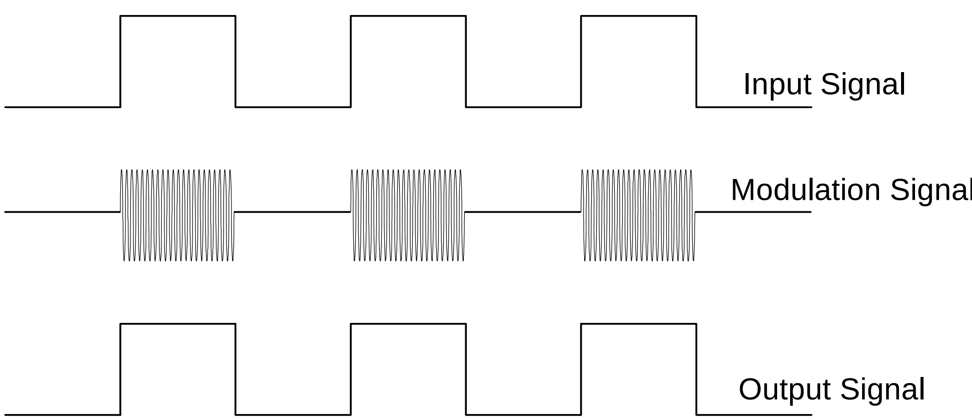

Figure 7. Modulation Scheme

2.3. DC-DC Converter Application Information

The Si88xx isolated dc-dc converter is based on a modified fly-back topology and uses an external transformer and Schottky rectifier for low cost and high operating efficiency. The PWM controller operates in closed-loop, peak current mode control and generates isolated output voltages with 2 W average output power at 5.0 V. Options are available for up-to 24 Vdc input or output operation and externally configured switching frequency.

The dc-dc controller modulates a pair of internal primary-side power switches (see Figure 8) to generate an isolated voltage at external diode D1 cathode. Closed-loop feedback is provided by a compensated error amplifier, which compares the voltage at the VSNS pin to an internal voltage reference. The resulting error voltage is fed back through the isolation barrier via an internal feedback path to the controller, thus completing the control loop.

For higher input supply voltages than 5V, an external FET Q2 is modulated by a driver pin ESW as shown in (see Figure 9). A shunt resistor based voltage sense pin RSN provides current sensing capability to the controller.

Additional features include an externally-triggered shutdown of the converter functionality using the SH pin and a programmable soft start configured by a capacitor connected to the SS pin. The Si88xx can be used in low- or high-voltage configurations. These features and configurations are explained in more detail below.

2.3.1. Shutdown

This feature allows the operation of the dc-dc converter to be shut down when asserted high.

2.3.2. Soft-Start

The dc-dc controller has an internal timer that controls the power conversion start-up to avoid inrush current. There is also the Soft Start option where users can program the soft start up by an external capacitor connected to the SS pin.

2.3.3. Programmable Frequency

The frequency of the PWM modulator is set to a default of 250 kHz. Users can program their desired frequency within a given band of 200 kHz to 800 kHz by controlling the time constant of an external RC connected to the SH_FC and SS pins.

2.3.4. External Transformer Driver

The dc-dc controller has internal switches (VSW) for driving the transformer with up-to a 5.5 V voltage supply. For higher voltages on the primary side, a driver output (ESW) is provided that can drive an external NMOS power transistor for driving the transformer. When this configuration is used, a shunt resistor based voltage sense pin (RSN) provides current sensing capability to the controller.

2.3.5. VREGA, VREGB

For supporting voltages greater than 5V, an internal voltage regulator (VREGA, VREGB) needs to be used in conjunction with an external NPN transistor, a resistor and a capacitor to provide regulated voltage to the IC.

2.3.6. Output Voltage Control

The isolated output voltage (VOUT) is sensed by a resistor divider that provides feedback to the controller through the VSNS pin. The voltage error is integrated and coupled back to the primary side controller across the isolation barrier, which in turn changes the duty cycle of the transformer driver.

2.3.7. Compensation

The dc-dc converter uses peak current mode control. The loop is compensated by connecting an external resistor in series with an external capacitor from the COMP pin to GNDB.

2.3.8. Thermal Protection

A thermal shutdown circuit is included to protect the system from over-temperature events. The thermal shutdown is activated at a junction temperature that prevents permanent damage from occurring.

2.3.9. Cycle Skipping

Cycle skipping is included to reduce switching power losses at light loads. This feature is transparent to the user and is activated automatically at light loads. The product options with integrated power switches (Si882xx/3xx) may never experience cycle skipping during operation even at light loads while the external power switch options (Si884xx/6xx) are likely to have cycle skipping kick in at light loads.

2.3.10. Low-Voltage Configuration

The low-voltage configuration is used for converting 3.0 V to 5.5 V. All product options of the Si88x2x and Si88x3x are intended for this configuration.

An advantage of Si882xx and Si884xx devices over other converters that use this same topology is that the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the Si882xx and Si884xx dc-dc to operate with superior line and load regulation while reducing external components and increasing lifetime reliability.

In a typical digital signal isolation application, the dc-dc powers the Si8824x and Si8834x's VDDB as shown in Figure 8. In addition to powering the isolated side of Si882xx and Si883xx, the dc-dc can deliver up to 2 W of power to other loads. The dc-dc requires an input capacitor, C2, blocking capacitor, C1, transformer, T1, rectifying diode, D1, and an output capacitor, C10. Resistors R5 and R6 divide the output voltage to match the internal reference of the error amplifier. Type 1 loop compensation made by R7 and C11 are required at the COMP pin. Though it is not necessary for normal operation, we recommend that a snubber be used to minimize radiated emissions. More details can be found in "AN892: Design Guide for Isolated DC-DC Using the Si882xx/883xx".

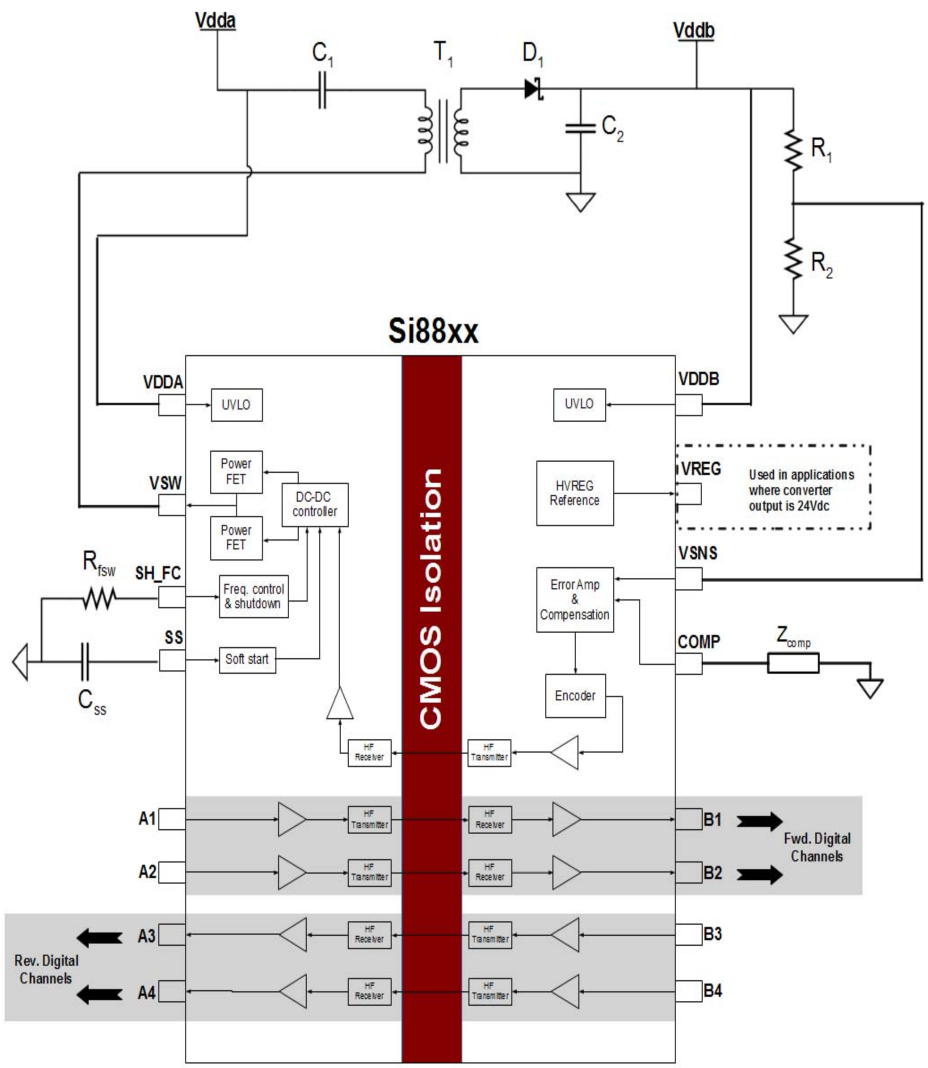

Figure 8. Si88xx Block Diagram: 3 V/3 V or 5 V/5 V Operation

2.3.11. High-Voltage Configuration

The high-voltage configuration is used for converting up to 24 V to 3.3V or 5.0 V. All product options of the Si88x4x and Si88x6x are intended for this configuration.

Si8844x and Si8864x can be used for dc-dc applications that have primary side voltage greater than 5.5 V. Si8844x and Si8864x dc-dc converter uses the isolated flyback topology. With this topology, the switch and sense resistor are external, allowing higher switching voltages. Digital isolator supply VDDA of the Si8844x and Si8864x require a supply less than or equal to 5.5 V. If a suitable supply is not available on the primary side, the VREGA voltage reference with external NPN transistor can supply VDDA. This eliminates the need to design an additional linear regulator circuit. Like the Si8824x and Si8834x, the output voltage is sensed on the secondary side without requiring additional opto-couplers and support circuitry to bias those opto-couplers. This allows the Si8844x and Si8864x dc-dc to operate with superior line and load regulation.

Figure 9 shows the block diagram of an Si8864x with external components. Si8864x is different from the Si8824x/8834x as it has externally-controlled switching frequency and soft start. The dc-dc requires input capacitor C2, transformer T1, switch Q1, sense resistor R12, rectifying diode D1and an output capacitor C10. To supply VDDA, Q2 transistor is biased and filtered by R14 and C14. External frequency and soft start behavior is set by C6 and R13. Resistors R5 and R6 divide the output voltage to match the internal reference of the error amplifier. Type 1 loop compensation made by R7 and C11 are required at the COMP pin. Though it is not necessary for normal operation, we recommend to use a snubber, to minimize high frequency emissions.

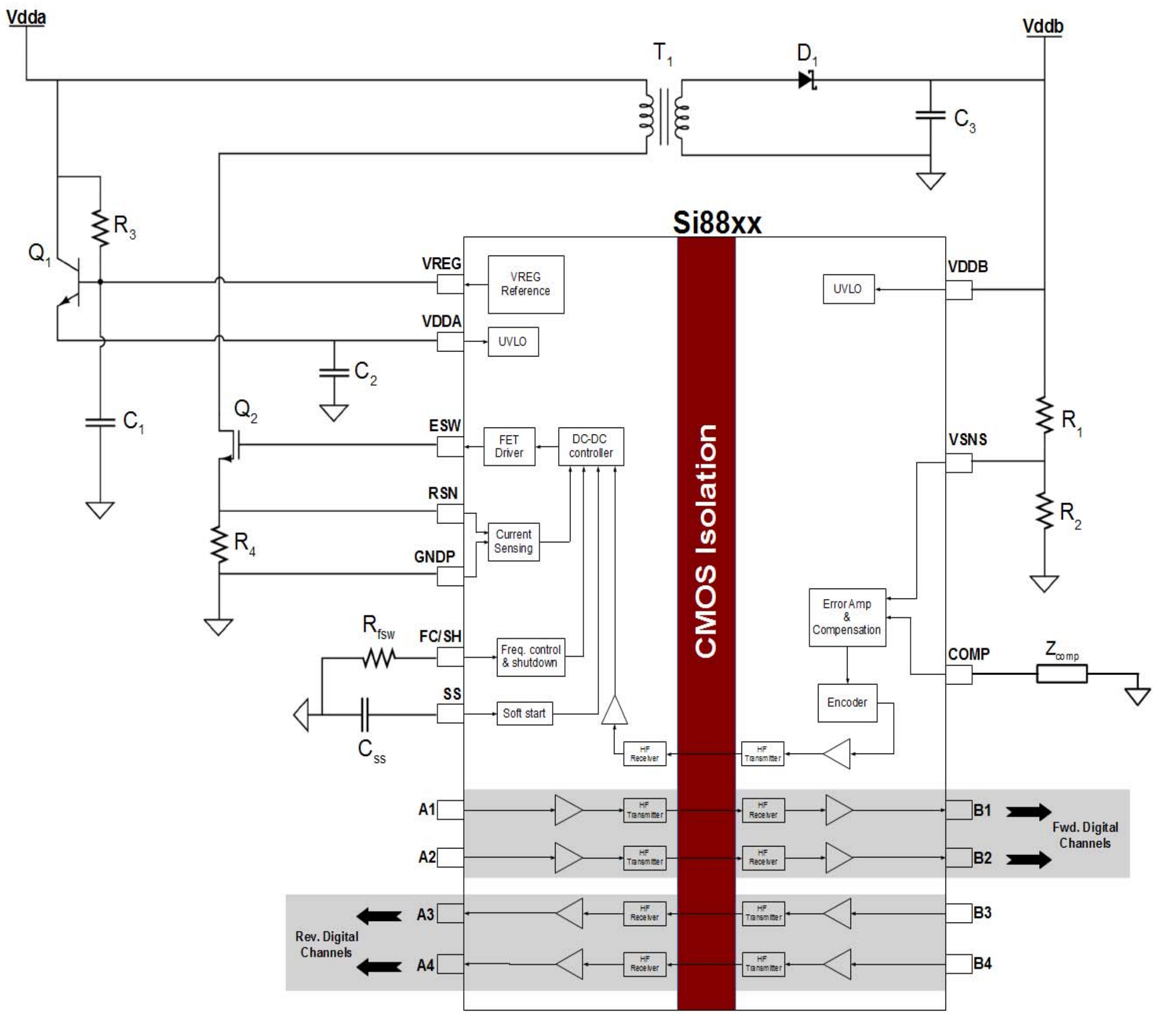

Figure 9. Si88xx Block Diagram: 24 V Input to 5 V Output

2.4. Transformer Design

Table 10 below provides the information on the appropriate transformer that has been validated for use for the different configurations as described in “2.3.10. Low-Voltage Configuration” . We highly recommend that users order the transformers from the vendors per the part numbers given below. Table 10 also provides detailed specifications for manufacturing your own transformers.

Table 10. Transformer Specifications

Transformer Part #	Input Voltage Range	Turns Ratio	Leakage Inductance	Primary Inductance	Primary Resistance	Isolation Rating
UMEC – UTB02185s	3.0– 5.5 V	4.0	100 nH ±5%	2 µH ±5%	0.05 Ω, max	2.5 kVrms

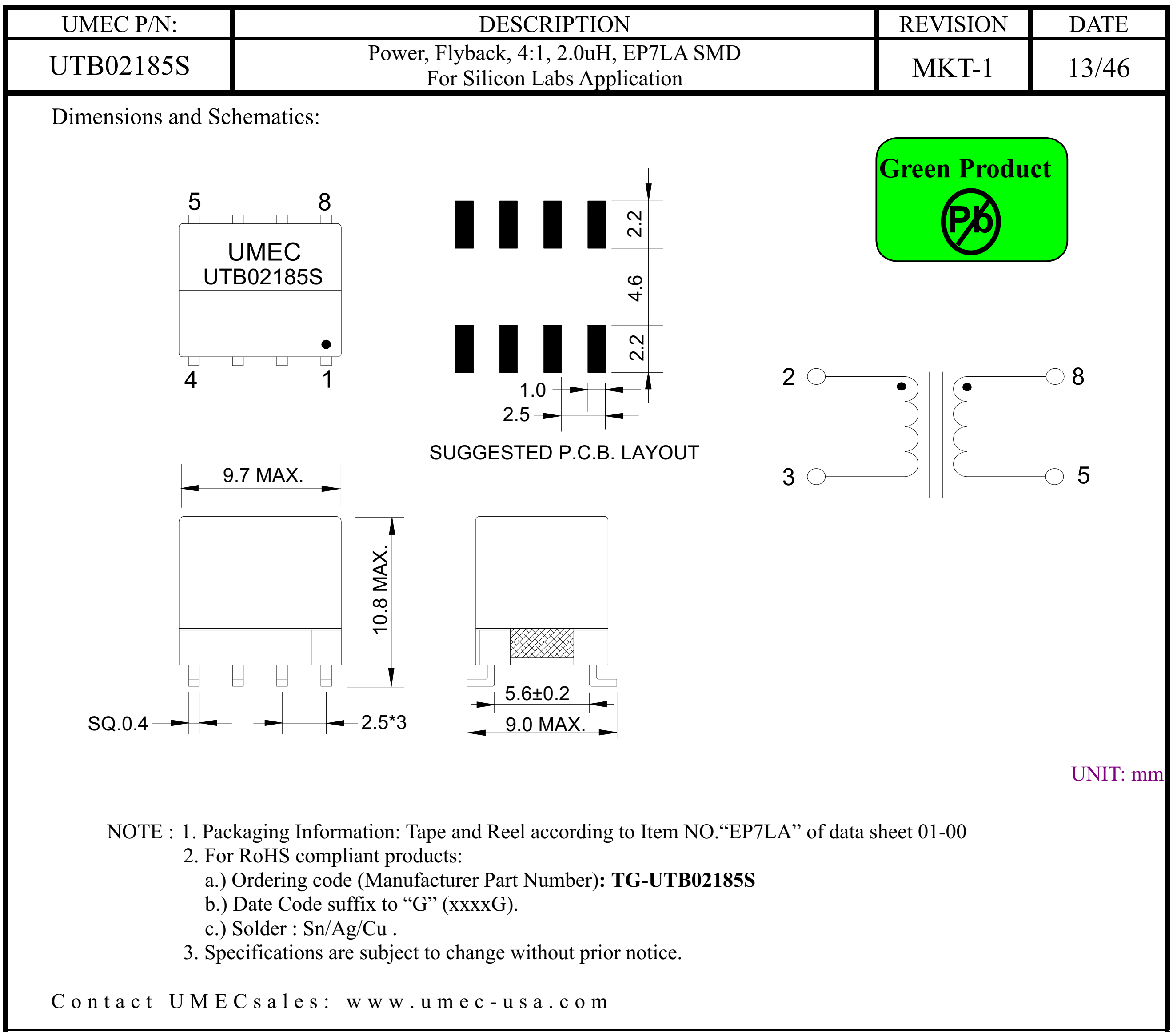

Figure 10. Transformer Specification

3. Digital Isolator Device Operation

Table 11. Si88xx Logic Operation

VI Input[1,2]	VDDI[1,2,3,4]	VDDO[1,2,3,4]	VO Output	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	L[4] H[4]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I.
X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I.

Notes:
1. VDDI and VDDO are the input and output power supplies. VI and VO are the respective input and output terminals.
2. P = powered; UP = unpowered.
3. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current. This situation should be avoided. We recommend that I/O's should not be driven high when primary side supply is turned off or when in dc-dc shutdown mode.
4. See "5. Ordering Guide" on page 36 for details. This is the selectable fail-safe operating mode (ordering option). When VDDB is powered via the primary side and the integrated dc-dc the default outputs are undetermined as secondary side power is not available when primary side power shuts off.

3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period t_{SU}. Following this, the outputs follow the states of inputs.

3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DDA} falls below V_{DDUV-} and exits UVLO when V_{DDA} rises above V_{DDUV+}. Side B operates the same as Side A with respect to its V_{DD} supply.

3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 4 on page 15 and Table 6 on page 16 detail the working voltage and creepage/clearance capabilities of the Si88xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1. Supply Bypass

The Si88xx family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.3.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.4. Fail-Safe Operating Mode

Si88xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 11 on page 24 and Table 13 on page 36 for more information.

3.5. Typical Performance Characteristics

The typical performance characteristics are for information only. Refer to Tables for specification limits.

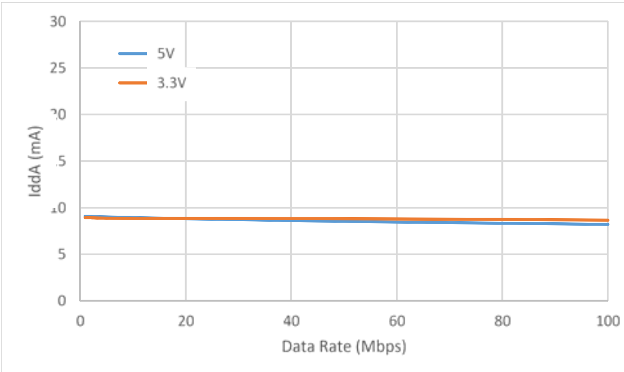

Figure 11. Si88240 Typical V_{DDA} Supply Current vs. Data Rate 5 and 3.3 V Operation

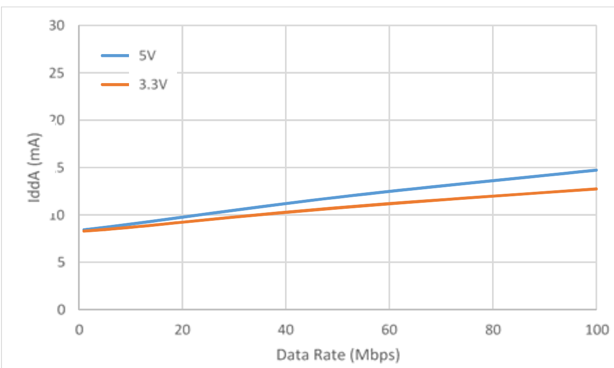

Figure 12. Si88241 Typical V_{DDA} Supply Current vs. Data Rate 5 and 3.3 V Operation

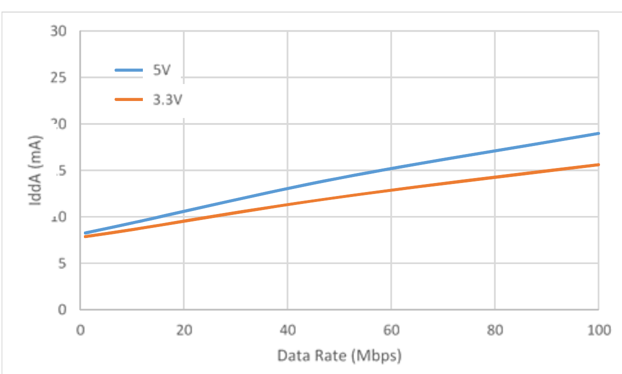

Figure 13. Si88242 Typical V_{DDA} Supply Current vs. Data Rate 5 and 3.3 V Operation

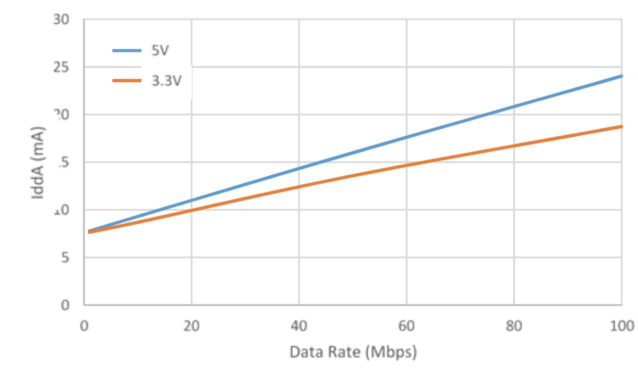

Figure 14. Si88243 Typical V_{DDA} Supply Current vs. Data Rate 5 and 3.3 V Operation

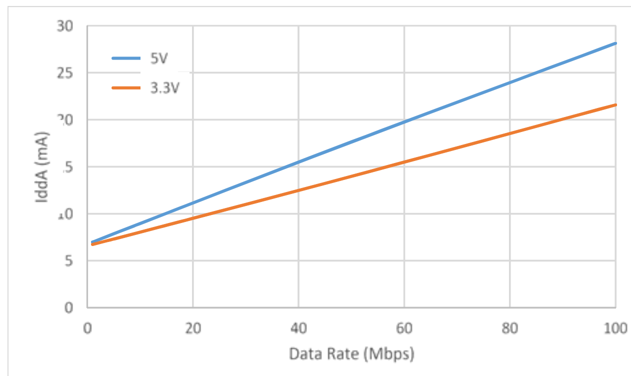

Figure 15. Si88244 Typical V_{DDA} Supply Current vs. Data Rate 5 and 3.3 V Operation

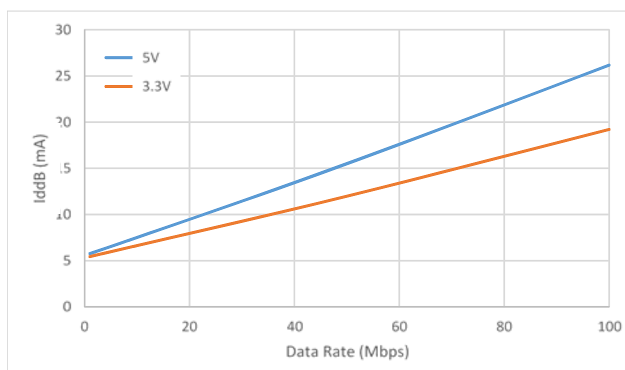

Figure 16. Si88240 Typical V_{DDB} Supply Current vs. Data Rate 5 and 3.3 V Operation

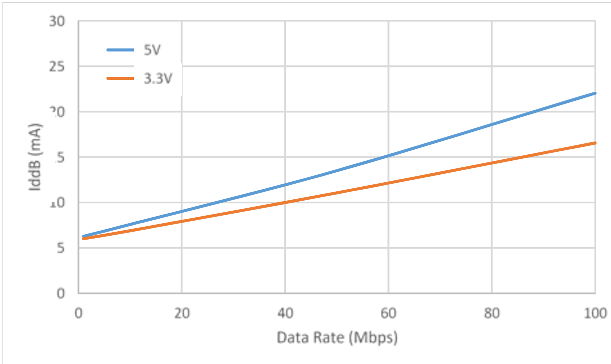

Figure 17. Si88241 Typical V_{DDB} Supply Current vs. Data Rate 5 and 3.3 V Operation

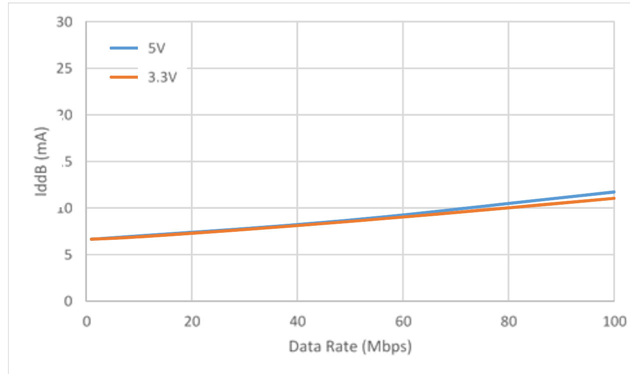

Figure 19. Si88243 Typical V_{DDB} Supply Current vs. Data Rate 5 and 3.3 V Operation

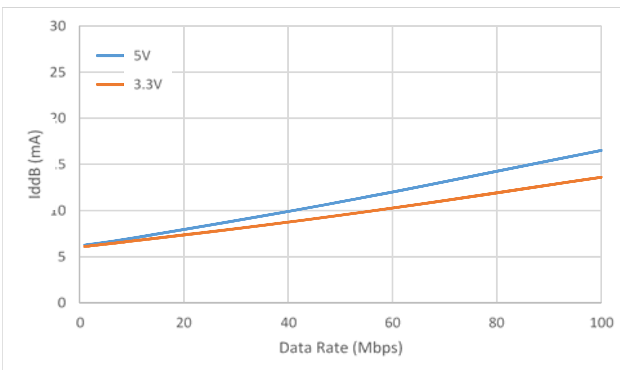

Figure 18. Si88242 Typical V_{DDB} Supply Current vs. Data Rate 5 and 3.3 V Operation

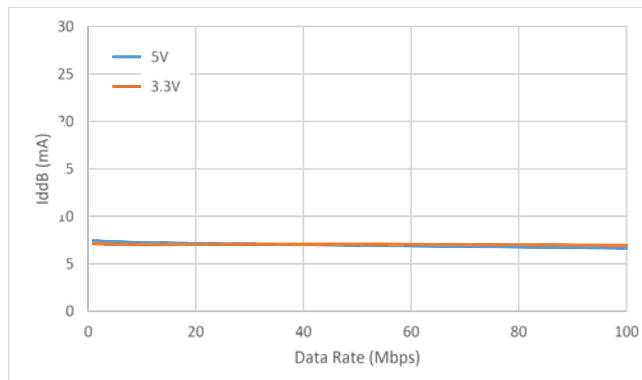

Figure 20. Si88244 Typical V_{DDB} Supply Current vs. Data Rate 5 and 3.3 V Operation

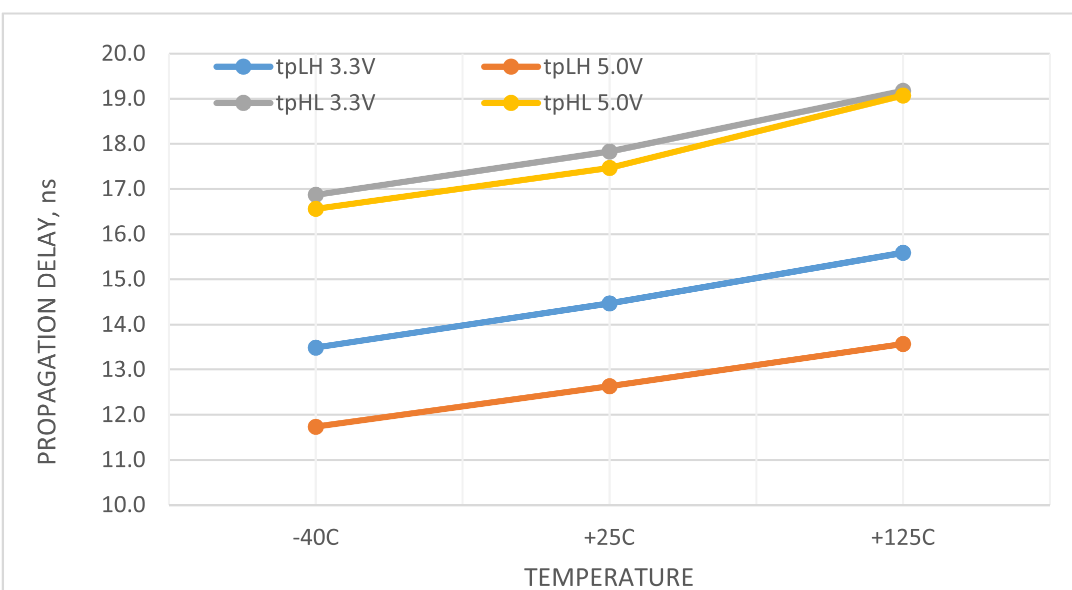

Figure 21. Propagation Delay vs. Temperature

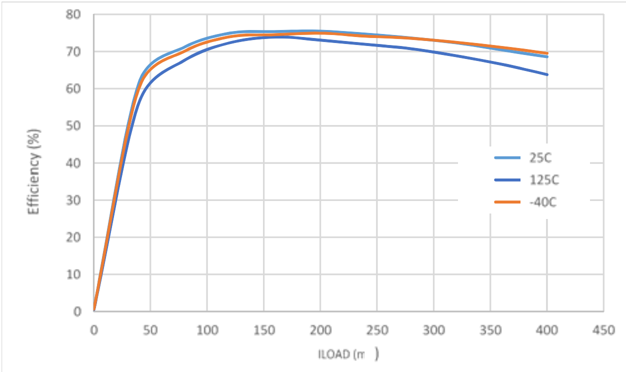

Figure 22a. Efficiency vs. Load Current over Temperature, 3.3 V–3.3 V

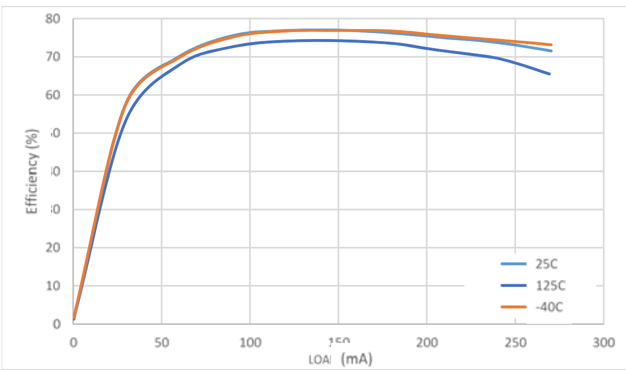

Figure 22b. Efficiency vs. Load Current over Temperature, 3.3 V–5.0 V

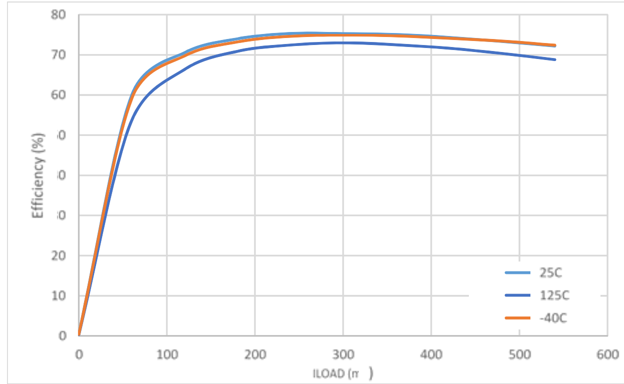

Figure 22c. Efficiency vs. Load Current over Temperature, 5.0 V–3.3 V

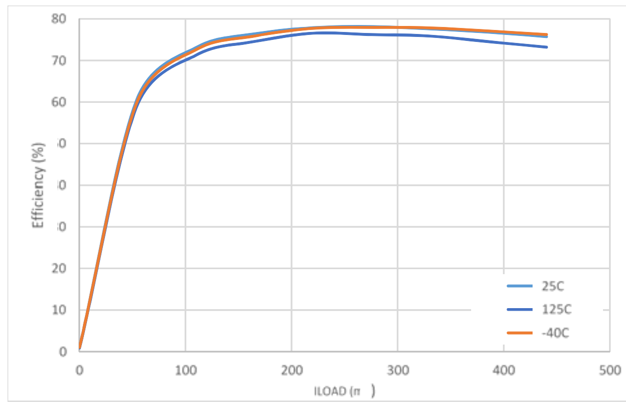

Figure 22d. Efficiency vs. Load Current over Temperature, 5.0 V–5.0 V

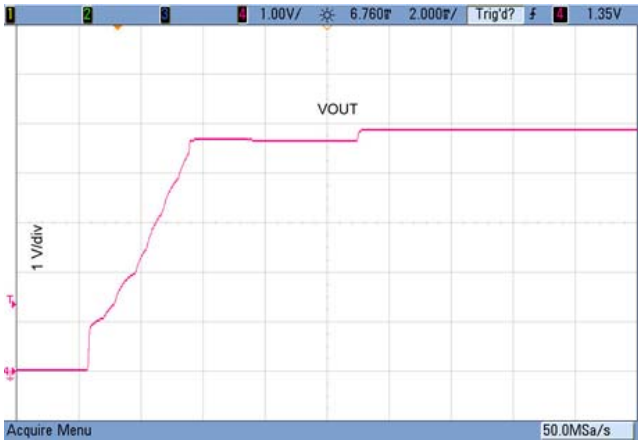

Figure 23a. 5 V–5 V VOUT Startup vs.Time, No Load

Figure 23c. 5 V–5 V VOUT Startup vs.Time, 50 mA Load Current

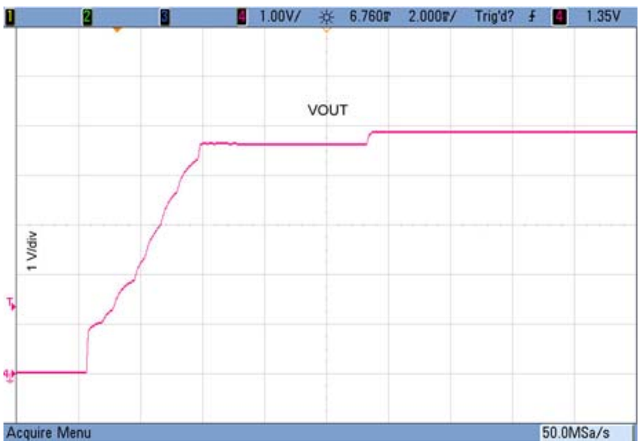

Figure 23b. 5 V–5 V VOUT Startup vs.Time, 10 mA Load Current

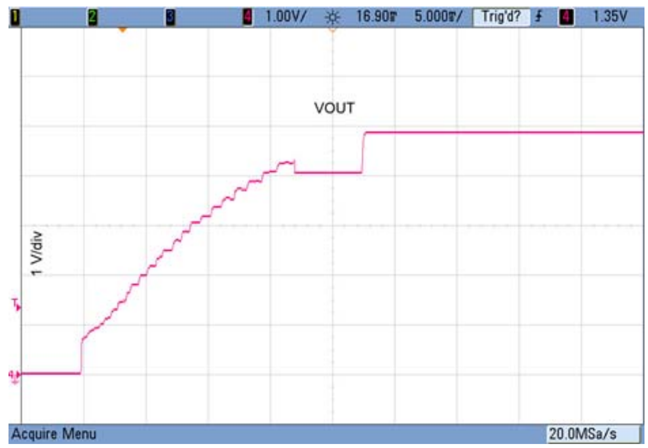

Figure 23d. 5 V–5 V VOUT Startup vs.Time, 400 mA Load Current

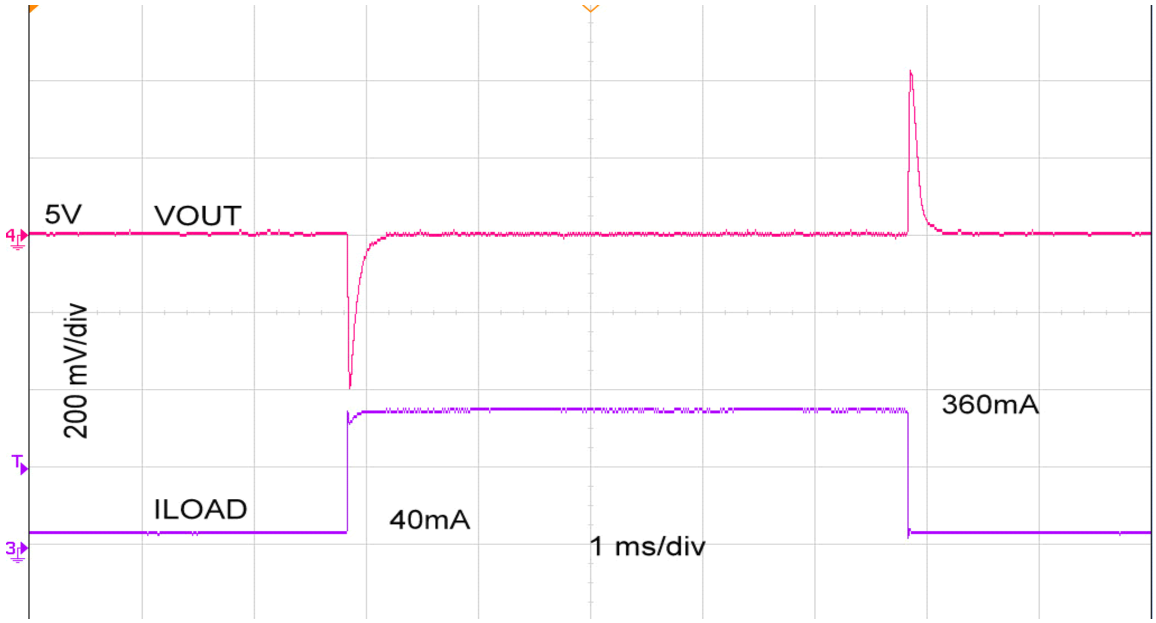

Figure 24. 5 V–5 V VOUT Load Transient Response, 10% to 90% Load

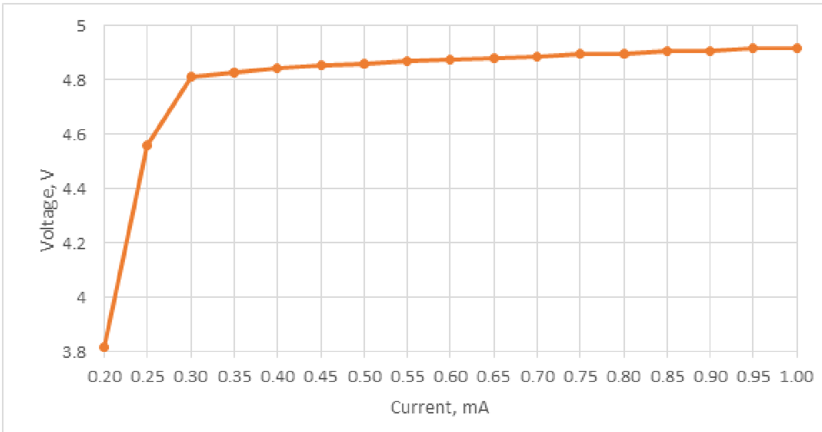

Figure 25. Typical I-V Curve for VREGA/B

4. Pin Descriptions

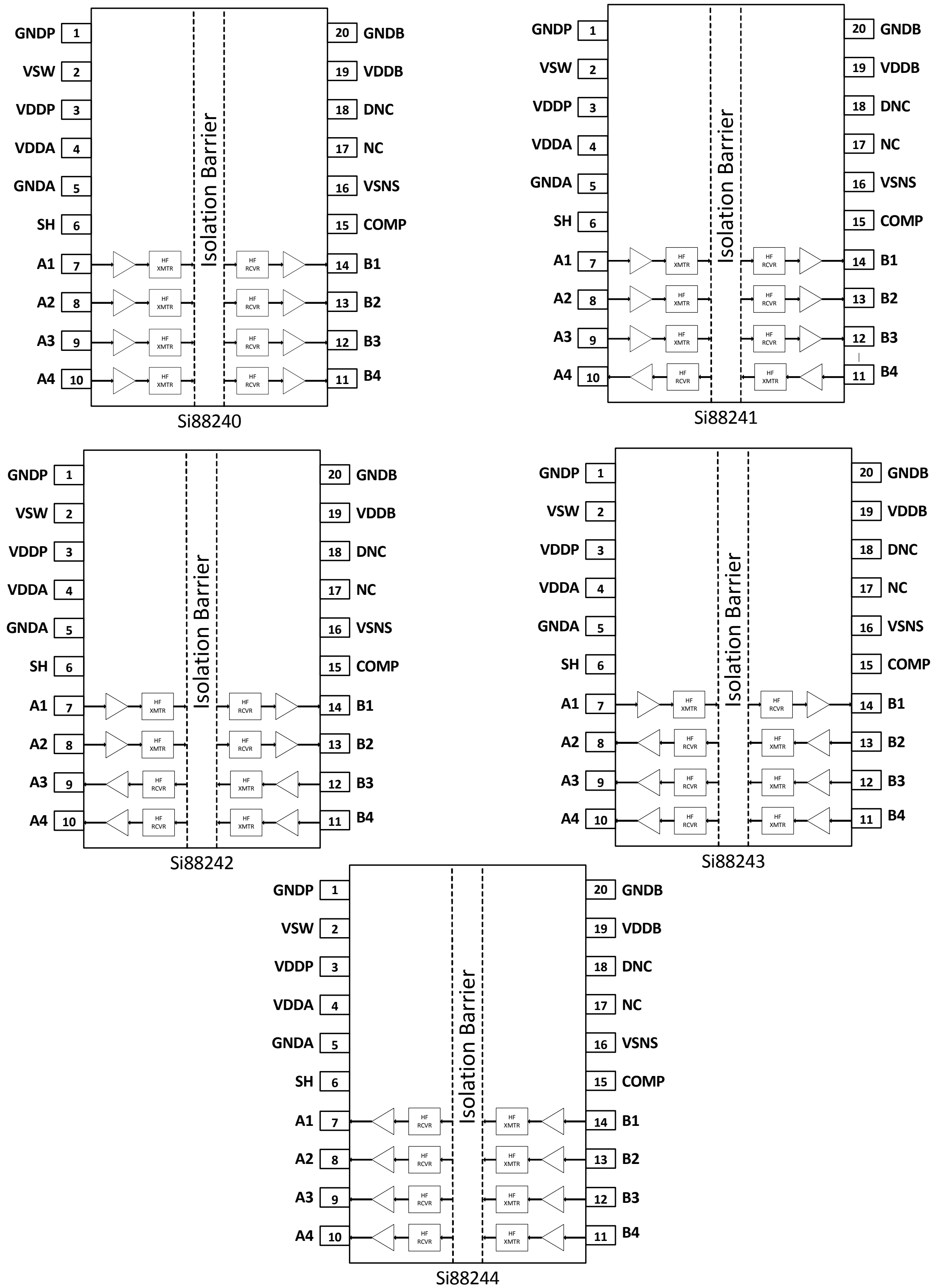

Figure 26. Si8824x Pin Configurations

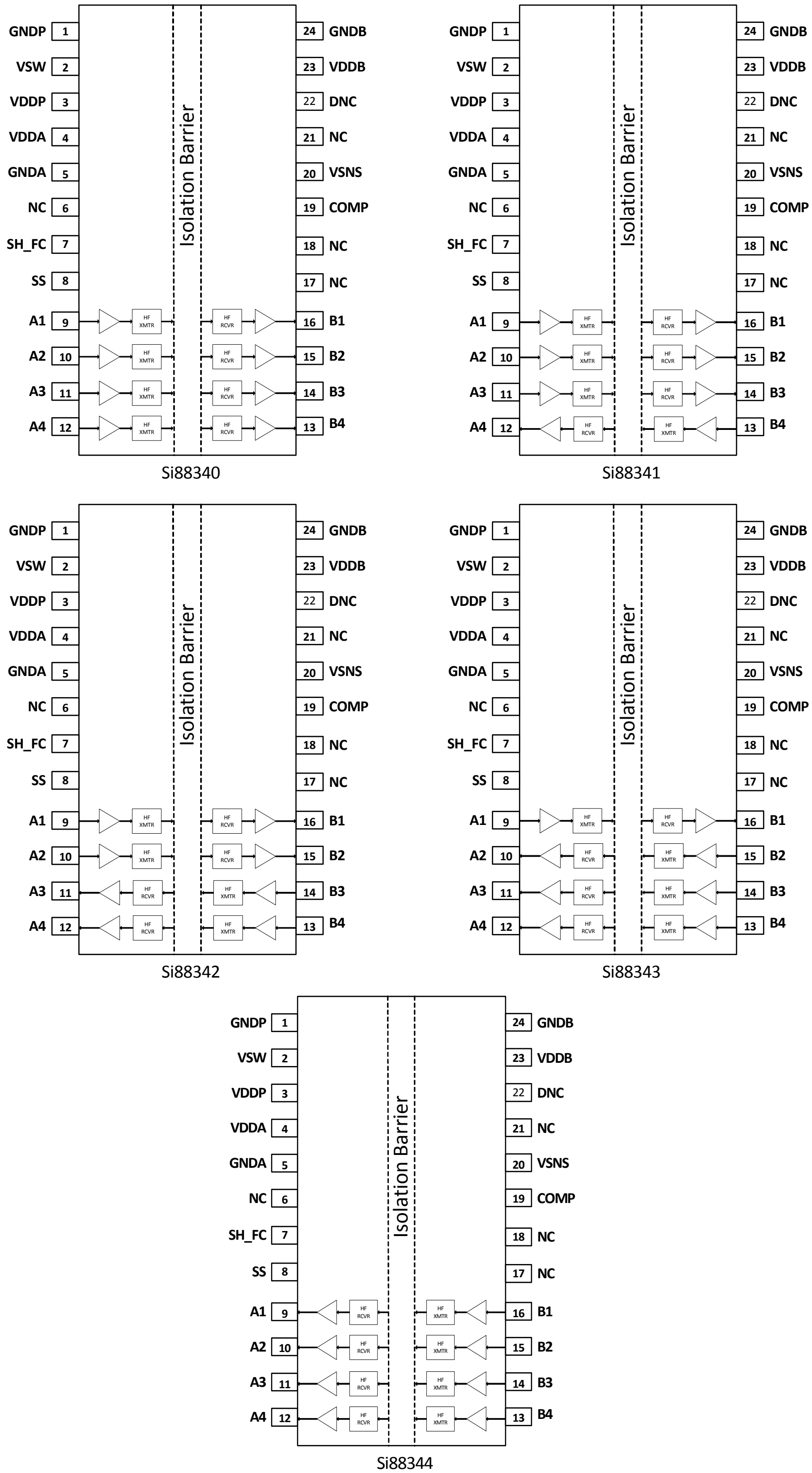

Figure 27. Si8834x Pinout Diagrams

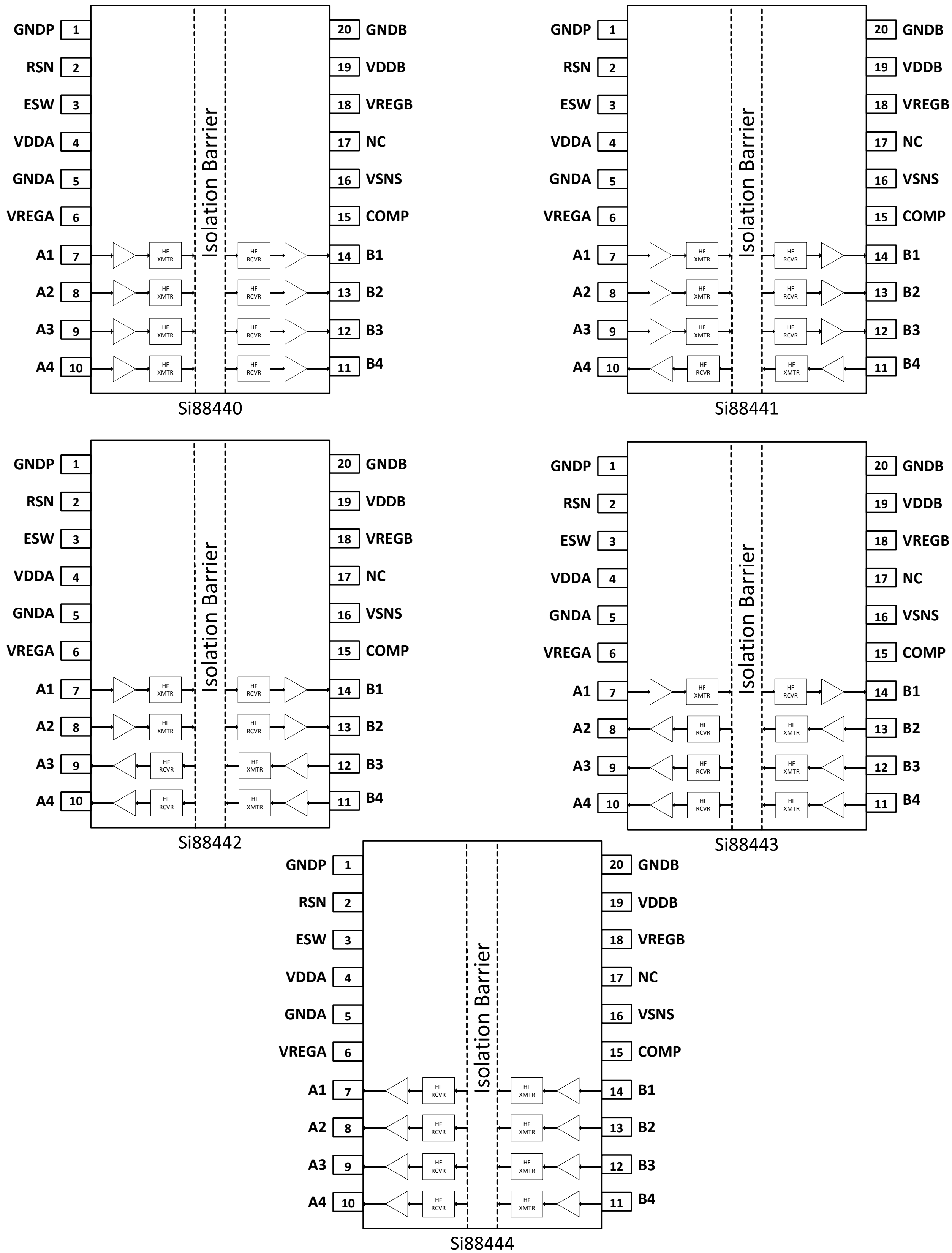

Figure 28. Si8844x Pinout Diagrams

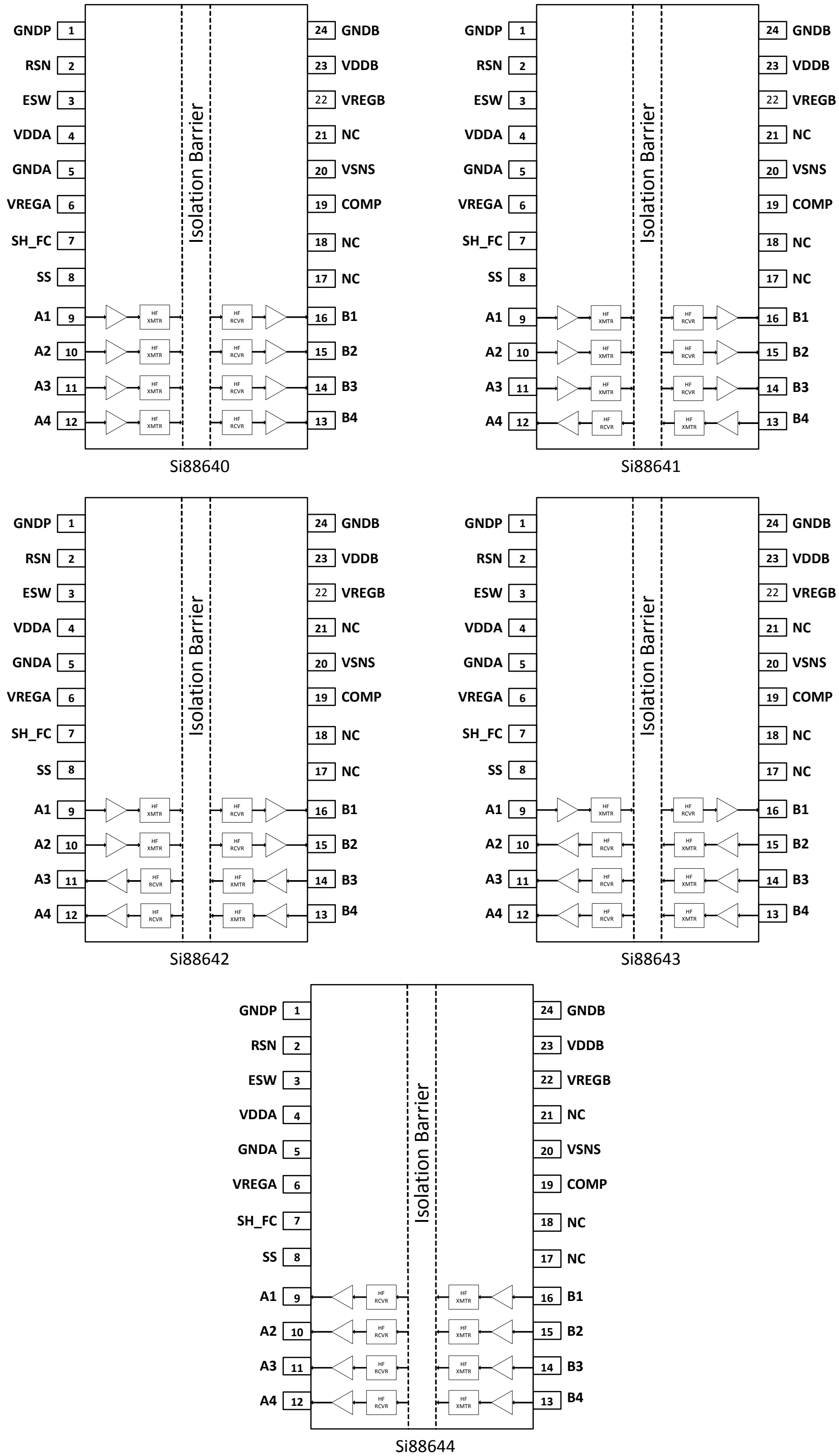

Figure 29. Si8864x Pinout Diagrams

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Table 12. Si88x4x Pin Descriptions

Pin Name	Description
DC-DC Input Side	
VDDP	Power stage primary power supply.
VREGA	Voltage reference output for external voltage regulator pin.
GNDP	Power stage ground.
ESW	Power stage external switch driver output.
VSW	Power stage internal switch output.
SS	Soft startup control.
SH_FC	Shutdown and Switch frequency control.
RSN	Power stage current sense input.
DC-DC Output Side	
VSNS	Power stage feedback input.
COMP	Power stage compensation.
VREGB	Voltage reference output for external voltage regulator pin.
DNC	Do not connect; leave open.
NC	No connect; this pin is not connected to the silicon.
Digital Isolator VDDA Side	
VDDA	Primary side signal power supply.
A1–A4	Input signal channel 1–4.
GNDA	Primary side signal ground.
Digital Isolator VDDB Side	
VDDB	Secondary side signal power supply.
B1–4	Output signal channel 1–4.
GNDB	Secondary side signal ground.

5. Ordering Guide

Table 13. Si88x4x Ordering Guide[1,2]

Part #	DC-DC Shutdown	Soft Start Control	Frequency Control	External Switch	Forward Digital	Reverse Digital	Package
Product Options Available Now							
Si88240ED-IS	Y	N	N	N	4	0	WB SOIC-20
Si88241ED-IS	Y	N	N	N	3	1	WB SOIC-20
Si88242ED-IS	Y	N	N	N	2	2	WB SOIC-20
Si88243ED-IS	Y	N	N	N	1	3	WB SOIC-20
Si88244ED-IS	Y	N	N	N	0	4	WB SOIC-20
Product Options Available in Sep 2015							
Si88240BD-IS	Y	N	N	N	4	0	WB SOIC-20
Si88241BD-IS	Y	N	N	N	3	1	WB SOIC-20
Si88242BD-IS	Y	N	N	N	2	2	WB SOIC-20
Si88243BD-IS	Y	N	N	N	1	3	WB SOIC-20
Si88244BD-IS	Y	N	N	N	0	4	WB SOIC-20
Si88340ED-IS	Y	Y	Y	N	4	0	WB SOIC-24
Si88341ED-IS	Y	Y	Y	N	3	1	WB SOIC-24
Si88342ED-IS	Y	Y	Y	N	2	2	WB SOIC-24
Si88343ED-IS	Y	Y	Y	N	1	3	WB SOIC-24
Si88344ED-IS	Y	Y	Y	N	0	4	WB SOIC-24
Si88440ED-IS	N	N	N	Y	4	0	WB SOIC-20
Si88441ED-IS	N	N	N	Y	3	1	WB SOIC-20
Si88442ED-IS	N	N	N	Y	2	2	WB SOIC-20
Si88443ED-IS	N	N	N	Y	1	3	WB SOIC-20
Si88444ED-IS	N	N	N	Y	0	4	WB SOIC-20
Si88640ED-IS	Y	Y	Y	Y	4	0	WB SOIC-24
Si88641ED-IS	Y	Y	Y	Y	3	1	WB SOIC-24
Si88642ED-IS	Y	Y	Y	Y	2	2	WB SOIC-24
Si88643ED-IS	Y	Y	Y	Y	1	3	WB SOIC-24
Si88644ED-IS	Y	Y	Y	Y	0	4	WB SOIC-24

Notes:

1. For valid orderable part numbers.
2. All Si88xxxEx product options are default output high on input power loss. All Si88xxxBx product options are default low. Please see “3. Digital Isolator Device Operation” for more details on default output behavior.

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6. Package Outline: 20-Pin Wide Body SOIC

Figure 30 illustrates the package details for the 20-pin wide-body SOIC package. Table 14 lists the values for the dimensions shown in the illustration.

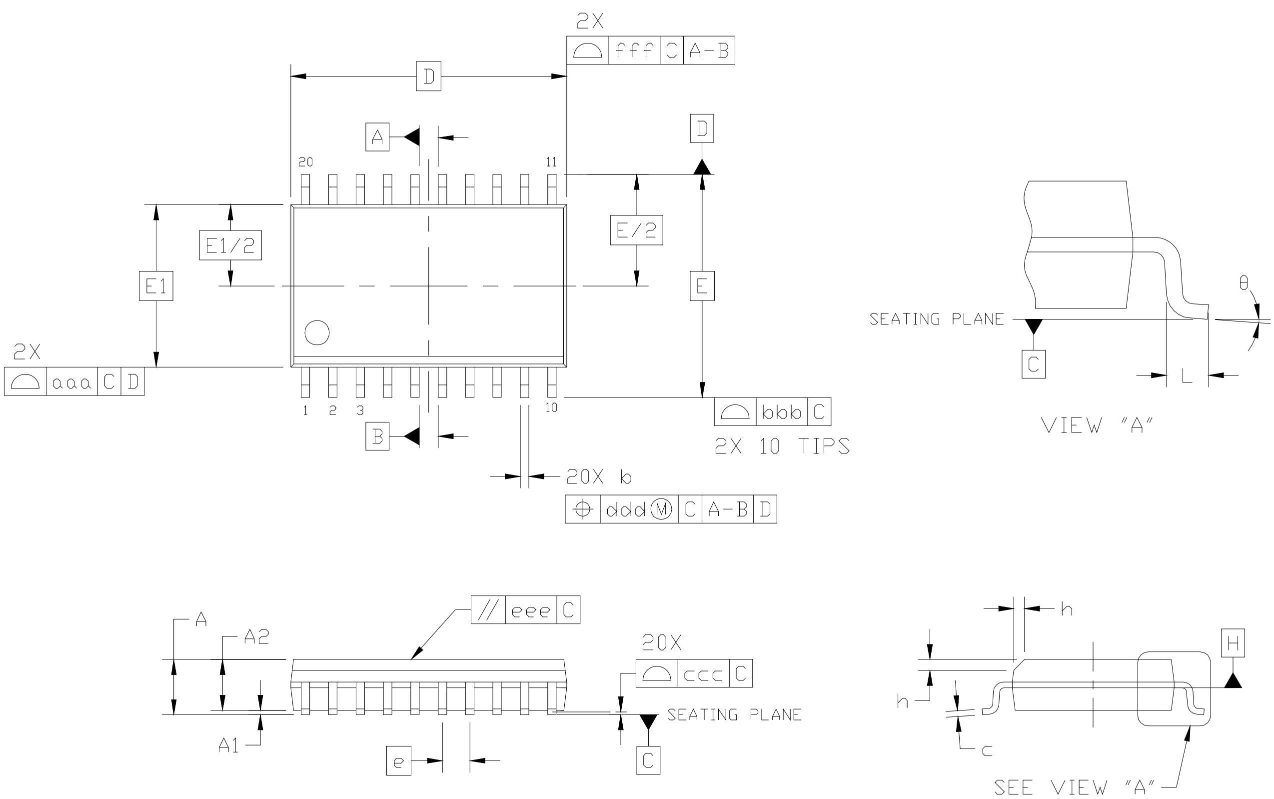


Figure 30. 20-Pin Wide Body SOIC

Table 14. 20-Pin Wide Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	12.80 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AC.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

7. Land Pattern: 20-Pin SOIC

Figure 31 illustrates the PCB land pattern details for the 20-pin SOIC package. Table 15 lists the values for the dimensions shown in the illustration.

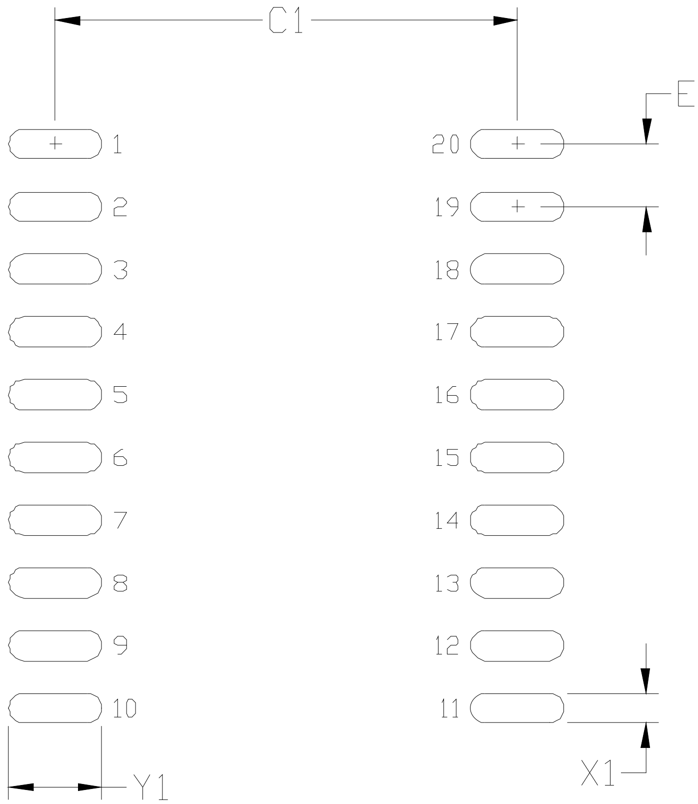


Figure 31. 20-Pin SOIC PCB Land Pattern

Table 15. 24-Pin SOIC PCB Land Pattern Dimensions

Dimension	mm
C1	9.40
E	1.27
X1	0.60
Y1	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

8. Package Outline: 24-Pin Wide Body SOIC

Figure 32 illustrates the package details for the 24-pin wide-body SOIC package. Table 16 lists the values for the dimensions shown in the illustration.

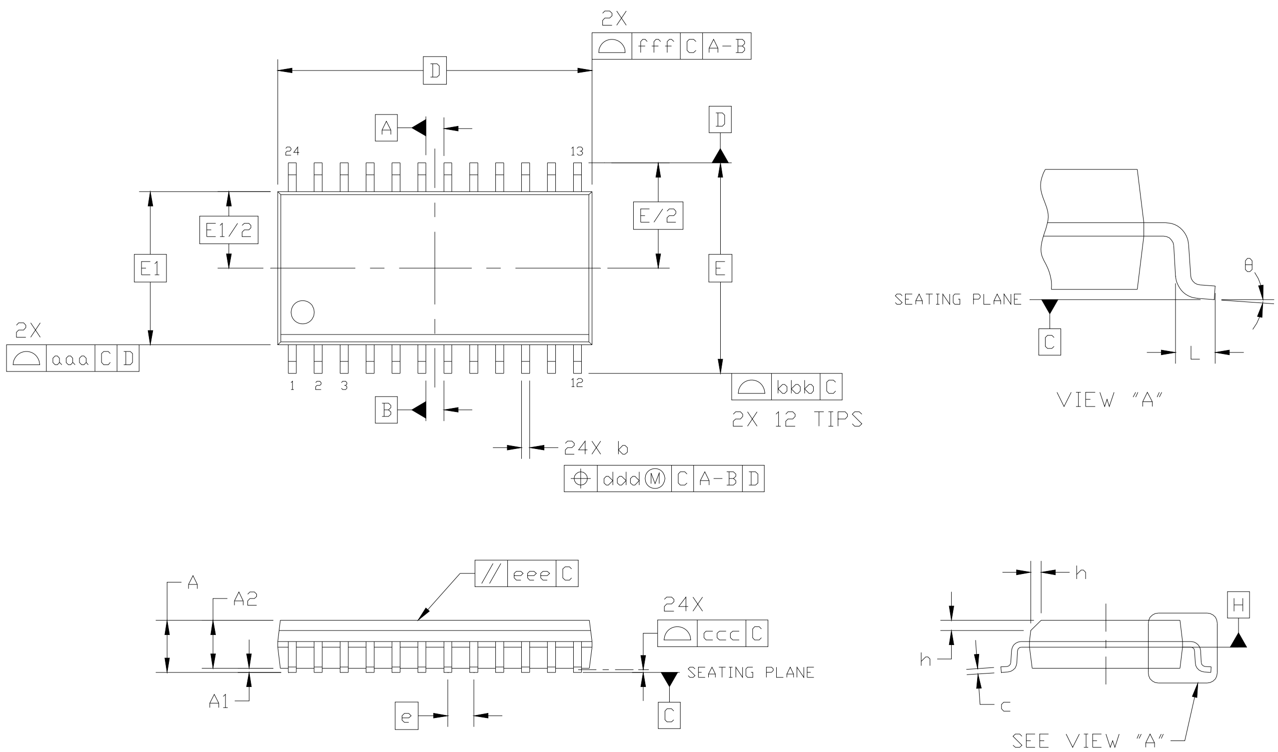


Figure 32. 24-Pin Wide Body SOIC

Table 16. 24-Pin Wide Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	15.40 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AD.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

9. Land Pattern: 24-Pin SOIC

Figure 33 illustrates the PCB land pattern details for the 24-pin SOIC package. Table 17 lists the values for the dimensions shown in the illustration.

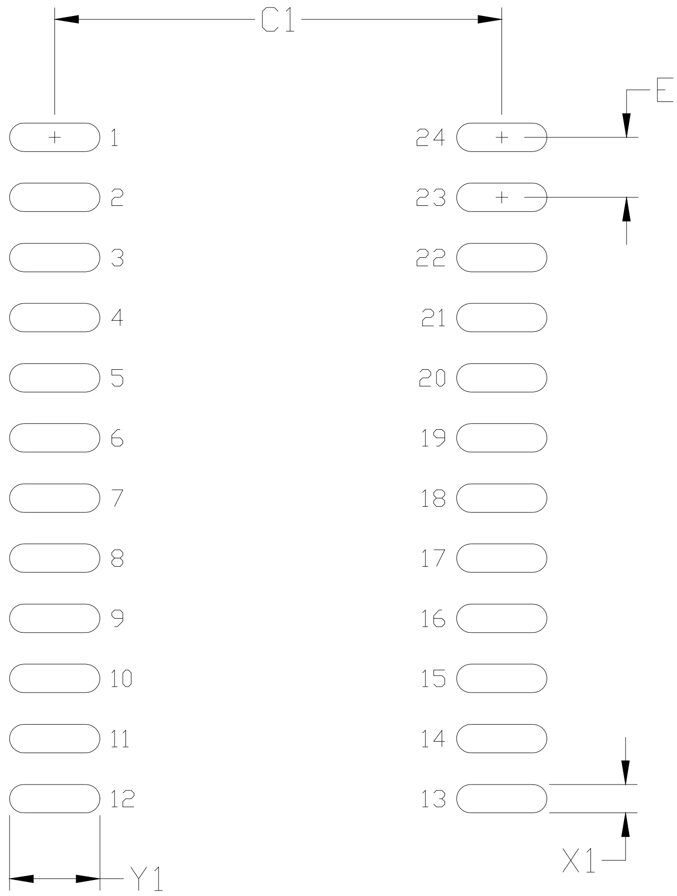


Figure 33. 24-Pin SOIC PCB Land Pattern

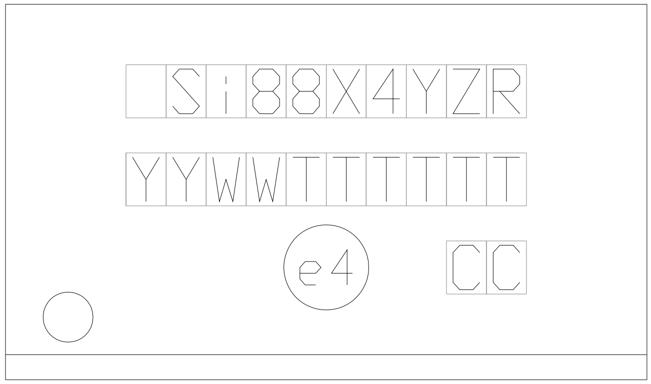
Table 17. 24-Pin SOIC PCB Land Pattern Dimensions

Dimension	mm
C1	9.40
E	1.27
X1	0.60
Y1	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Markings

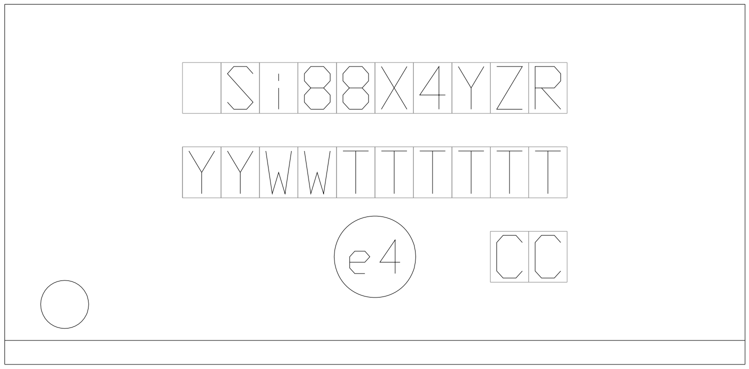
10.1. Si88x4x Top Marking (20-Pin Wide Body SOIC)



10.2. Top Marking Explanation (20-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si88x4 = 5 kV rated 4 channel digital isolator with dc-dc converter X = 2, 3, 4, 6 2 = dc-dc shutdown, 4 = external FET, 6 = full featured dc-dc with external FET 3 = Full-featured dc-dc with integrated FET Y = Number of reverse channels Z = E, B E = default high B = default low R = A, C, D A = 1 kVrms isolation rating C = 3.75 kVrms isolation rating D = 5 kVrms isolation rating
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

10.3. Si88x4x Top Marking (24-Pin Wide Body SOIC)



10.4. Top Marking Explanation (Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si88x4 = 5kV rated 4 channel digital isolator with dc-dc converter X = 2, 3, 4, 6 2 = dc-dc shutdown, 4 = external FET, 6 = full featured dc-dc with external FET 3 = Full-featured dc-dc with integrated FET Y = Number of reverse channels Z = E, B E = default high B = default low R = A, C, D A = 1 kVrms isolation rating C = 3.75 kVrms isolation rating D = 5 kVrms isolation rating
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

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