# Dual-Cell Lithium Ion Battery Control IC

## DESCRIPTION

The Si9730 monitors the charging and discharging of dual-cell lithium-ion battery packs (carbon or coke chemistry) ensuring that battery capacity is fully utilized while ensuring safe operation. The Si9730 provides protection against over-charge, over-discharge, and short circuit conditions which are hazardous to the battery and the environment.

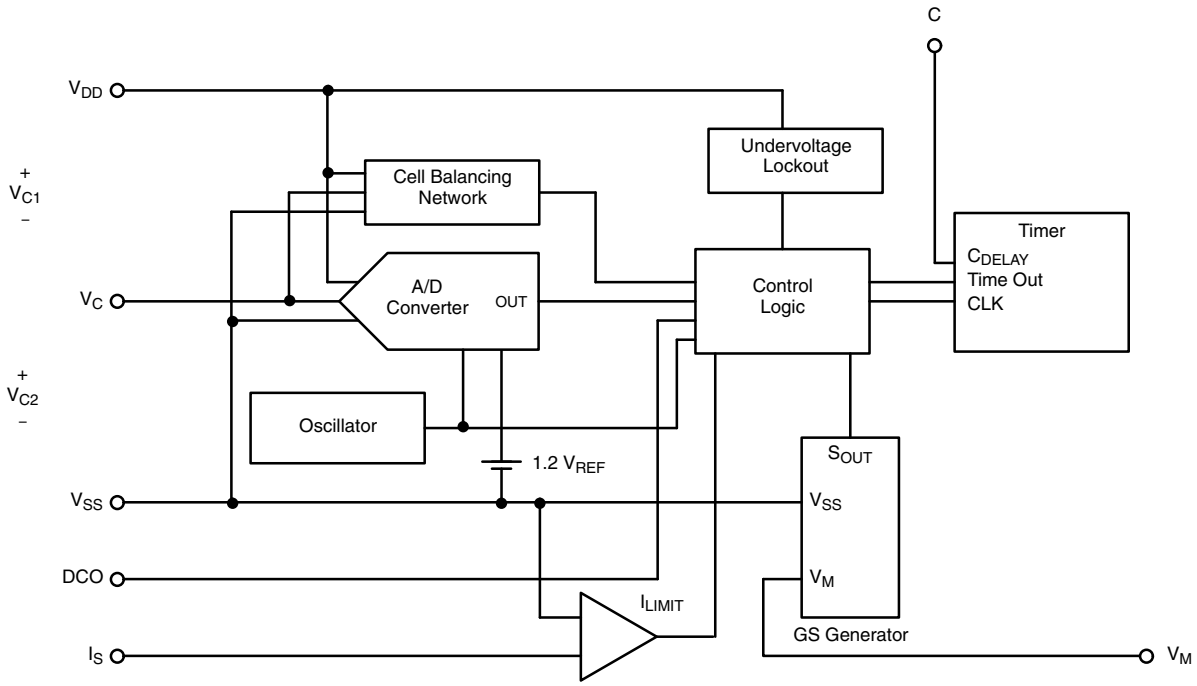
Battery voltages of each individual cell are monitored at the center-tap connection by an internal A/D converter through the $V_C$ pin. If one or both of the cells is determined to be overcharged, an internal cell balancing network "bleeds" off current at 15 µA until both cells are charged to the same maximum level. Depending on the condition of each cell, the Si9730 will switch two external source-connected N-Channel MOSFETs on or off to allow the cells to be charged or to provide current to the load.

The Si9730 is available in an 8-pin SOIC package with an operating temperature range of - 25 to 85 °C. The Si9730 is available in both standard and lead (Pb)-free packages.

## FEATURES

- Over-Charge Protection
- Over-Discharge Protection
- Short Circuit Current Limiting
- Battery Open-Circuit Center Tap Protection
- Cell Voltage Balancing
- Undervoltage Lockout
- Individual Cell Voltage Monitoring
- Low Operating Current (30 µA) and Shutdown Current (1 µA)
- Internal N-Channel MOSFET Driver
- High Noise Immunity
- Accurate (± 1.19 %) Over-Charge Voltage Detection
- Four Different Cell Types Covered

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Limit | Unit |
|---|---|---|---|
| $V_M$ | | $V_{DD}$ - 1.5 V to $V_{DD}$ + 15 V | V |
| $V_{DD}$ | | $V_{SS}$ - 0.3 V to $V_{SS}$ + 12 V | |
| $V_C$ | | $V_{SS}$ - 0.3 V to $V_{DD}$ + 0.3 V | |
| $I_S$ | ($V_{SS} \geq V_M$) | $V_M$ - 0.3 V to $V_{DD}$ + 0.3 V | |
| | ($V_M \geq V_{SS}$ ) | $V_{SS}$ - 0.3 V to $V_{DD}$ + 0.3 V | |
| Maximum Operating Junction Temperature | | 125 | °C |
| Power Dissipation | | 200 | mW |
| Thermal Impedance ($P_{\Theta JA}$) | | 80 | °C/W |
| Storage Temperature | | - 55 to 150 | °C |

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING RANGE

| Parameter | Limit | Unit |
|---|---|---|
| **$C_{VC}$ < 10 pF from $V_C$ to $V_{DD}$ and $V_{SS}$ , Total** | | |
| $C_D$ | Open to 1.0 | µF |
| $R_{IS}$ series resistance to sense resistor | < 27 | kΩ |
| DCO Load Capacitance | 0 to 2000 | pF |
| $V_{DD}$ to $V_{SS}$ | 9 | V |
| $V_{DD}$ to $V_M$ | 12 | |
| Operating Temperature Range | - 25 to 85 | °C |

## SPECIFICATIONS

| Parameter | Symbol | Test Conditions Unless Otherwise Specified | Limits $T_A$ = - 25 to 85 °C Min[a] | Typ[b] | Max[a] | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Supply Current, Charging Operation | $I_{DD\_C}$ | $V_{C1} = V_{C2}$ = 2.6 V, $V_{DD} - V_M$ = 8.4 V | | | 60 | µA |
| Supply Current, Normal Operation | $I_{DD}$ | $V_{C1} = V_{C2}$ = 4.05 V, $V_M = V_{SS}$ | | | 30 | |
| | $I_{DD\_UVL}$ | $V_M = V_{DD}$, $V_{C1} = V_{C2}$ = 1.7 V | | | 1 | |
| Undervoltage Lockout Threshold | $V_{UVL}$ | Measured at $V_{DD} - V_{SS}$ (Falling) $V_{C1} = V_{C2}$, $V_{DD} - V_M$ = 5.5 V | 3.5 | 3.7 | 4.0 | V |
| $V_M$ Leakage Current | $I_{VM\_UVL}$ | $V_{C1} = V_{C2}$ = 1.7 V, $V_{DD} = V_M$ | | | 1 | µA |
| $V_M$ Operating Current | $I_{VM}$ | $V_{C1} = V_{C2}$ = 2.6 V, $V_{DD} - V_M$ = 8.4 V | | | 30 | |
| **Control Logic** | | | | | | |
| DCO Output High Voltage | $V_{OH}$ | $I_{OH}$ = - 10 µA, $V_{C1} = V_{C2}$ = 3.3 V $V_{DD} - V_M$ = 6.6 V | $V_{DD}$ - 0.1 | | | V |
| DCO Rise Time (10 % to 80 %) | $t_r$ | $V_{C1}$ = 2 V, $V_{C2}$ = 2.4 V $V_{DD} - V_M$ = 8.4 V $C_L$ = 500 pF, DCO to $V_{SS}$ | | | 7.5 | µs |
| DCO Fall Time (80 % to 10 %) | $t_f$ | | | | 1 | |
| DCO Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 10 µA; $V_M = V_{DD}$, $V_{C1}$ = 2 V, $V_{C2}$ = 2.4 V | | | $V_{SS}$ + 0.4 | V |
| | | $I_{OL}$ = 10 µA; $V_M = V_{SS}$, $V_{C1} = V_{C2}$ = 4.4 V, $I_S = V_{DD}$ | | | $V_M$ + 0.52 | |
| **Analog Section** | | | | | | |
| Current-Limit Comparator Trip Point | $V_{ILIMIT}$ | $V_{C1} = V_{C2}$ = 4.05 V, $V_M = V_{SS}$ + 0.25 V $I_S$ Rising, $T_A$ = 25 °C | 25.5 | 28 | 32 | mV |
| Current-Limit Comparator Temperature Coefficient | $dV_{ILIMIT}/dT$ | | | 0.18 | | %/°C |
| Current-Limit Comparator Response Time | $t_{ILIMIT}$ | $V_{C1} = V_{C2}$ = 3.3 V, $V_M = V_{SS}$ + 0.25 V $C_L$ = 50 pF, DCO to $V_{SS}$, See Figure 2 | | | 25 | µs |
| Current Limit Comparator Input Bias Current | $I_{IS}$ | $V_{C1} = V_{C2}$ = 3.3 V, $V_{DD} = V_M$, $V_{IS} = V_{SS}$ | - 125 | | | nA |

## SPECIFICATIONS

| Parameter | | Symbol | Test Conditions Unless Otherwise Specified | | Limits $T_A$ = - 25 to 85 °C Min[a] | Typ[b] | Max[a] | Unit |
|---|---|---|---|---|---|---|---|---|
| **Analog Section (cont'd)** | | | | | | | | |
| Over-Charge Detect Threshold (Rising) | A Suffix | $V_{OC1}$ Cell 1 | $V_{C2}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.15 | 4.20 | 4.25 | V |
| | | | | $T_A$ = - 25 °C | 4.1 | | 4.27 | |
| | | | | $T_A$ = 85 °C | 4.1 | | 4.27 | |
| | | $V_{OC2}$ Cell 2 | $V_{C1}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.15 | 4.20 | 4.25 | |
| | | | | $T_A$ = - 25 °C | 4.1 | | 4.27 | |
| | | | | $T_A$ = 85 °C | 4.1 | | 4.27 | |
| | B Suffix | $V_{OC1}$ Cell 1 | $V_{C2}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.2 | 4.25 | 4.30 | |
| | | | | $T_A$ = - 25 °C | 4.15 | | 4.32 | |
| | | | | $T_A$ = 85 °C | 4.15 | | 4.32 | |
| | | $V_{OC2}$ Cell 2 | $V_{C1}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.2 | 4.25 | 4.30 | |
| | | | | $T_A$ = - 25 °C | 4.15 | | 4.32 | |
| | | | | $T_A$ = 85 °C | 4.15 | | 4.32 | |
| | C Suffix | $V_{OC1}$ Cell 1 | $V_{C2}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.18 | 4.22 | 4.25 | |
| | | | | $T_A$ = - 25 °C | 4.12 | | 4.30 | |
| | | | | $T_A$ = 85 °C | 4.12 | | 4.25 | |
| | | $V_{OC2}$ Cell 2 | $V_{C1}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.18 | 4.22 | 4.25 | |
| | | | | $T_A$ = - 25 °C | 4.12 | | 4.30 | |
| | | | | $T_A$ = 85 °C | 4.12 | | 4.25 | |
| | D Suffix | $V_{OC1}$ Cell 1 | $V_{C2}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.28 | 4.32 | 4.35 | |
| | | | | $T_A$ = - 25 °C | 4.22 | | 4.40 | |
| | | | | $T_A$ = 85 °C | 4.22 | | 4.35 | |
| | | $V_{OC2}$ Cell 2 | $V_{C1}$ = 4.05 V, $V_{DD}$ - $V_M$ = 8.6 V | $T_A$ = 25 °C | 4.28 | 4.32 | 4.35 | |
| | | | | $T_A$ = - 25 °C | 4.22 | | 4.40 | |
| | | | | $T_A$ = 85 °C | 4.22 | | 4.35 | |
| Over-Charge Threshold Difference | | $\lvert V_{OC1} - V_{OC2} \rvert$ | | | | | 20 | mV |
| Over-Charge Detect Threshold Hysteresis[c] | Cell 1 | $V_{OC\_H1}$ | $V_{DD}$ - $V_M$ = 8 6 V | $V_{C2}$ = 4.05 V | | | 10 | |
| | Cell 2 | $V_{OC\_H2}$ | | $V_{C1}$ = 4.05 V | | | 10 | |
| Over-Discharge Detect Threshold (Falling) | Cell 1 | $V_{ODC1}$ | $V_M$ = $V_{SS}$ | $V_{C2}$ = 2.6 V | 2.1 | 2.2 | 2.3 | V |
| | Cell 2 | $V_{ODC2}$ | | $V_{C1}$= 2.6 V | 2.1 | 2.2 | 2.3 | |
| Cell Balancing Current | Cell 1 | $I_{BAL1}$ | | $V_{C1}$ = 4.4 V, $V_{C2}$ = 4.05 V | 9 | 15 | 30 | µA |
| | Cell 2 | $I_{BAL2}$ | | $V_{C2}$ = 4.4 V, $V_{C1}$ = 4.05 V | 9 | 15 | 30 | |
| Timer Charge Current | | $I_{TIMER(C)}$ | $V_{C2}$ = 3.3 V, $V_M$ = $V_{SS}$, $V_C$ = $V_{SS}$, $T_A$ = 25 °C | | | - 0.5 | | |
| Timer Discharge Current | | $I_{TIMER(D)}$ | $V_{C1}$ = $V_{C2}$ = 3.3 V, $V_{DD}$ = $V_M$, $V_{DD}$ - $V_C$ = 6.1 V, $T_A$ = 25 °C | | | 1.0 | | mA |
| DL2 Time (Over-Charge) | | $t_{DL2OC}$ | $V_{C1}$ = 4.05 V, $V_{DD}$ - $V_M$ = 10 V, CD = 500 pF, $T_A$ = 25 °C, See Figure 4 | | 27 | 40 | 60 | ms |
| DL2 Time (Over-Discharge) | | $t_{DL2ODC}$ | $V_{C1}$ = 2.6 V, $V_M$ = $V_{SS}$, CD = 500 pF, $T_A$ = 25 °C, See Figure 5 | | 27 | 40 | 60 | |
| External Short Circuit Sense Current | | $I_{VMSHORT}$ | $V_{C1}$ = $V_{C2}$ = 4.4 V, $V_M$ = $V_{DD}$ | | 30 | | 300 | µA |
| Reset Threshold | | $V_{RTH}$ | $V_{C1}$ = $V_{C2}$ = 4.05 V, See Figure 3 | | 42 | 60 | 100 | mV |
| Center Tap, Average Bias Current | | $I_{VC}$ | $V_{C1}$ = $V_{C2}$ = 4.05 V, $V_M$ = $V_{DD}$ | | - 2 | | 2 | µA |
| Overcharge Load Detect | | $t_{OCC}$ | $V_{C1}$ = $V_{C2}$ = 4.4 V, CD = 500 pF, $C_L$ = 500 pF, DCO to $V_{SS}$, See Figure 1 | | | | 40 | µs |
| Power-Down Charger Detect Threshold | | $V_{CHPD}$ | $V_{C1}$ = 2 V, $V_{C2}$ = 2.4 V, See Figure 6 | | | | 1.1 | V |
| DCO Pulse Width | | $t_{PW}$ | $C_L$ = 500 pF, DCO to $V_{SS}$, See Figure 7 | | | 520 | | µs |

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Guaranteed by design, not subject to production test.

## TIMING DIAGRAMS

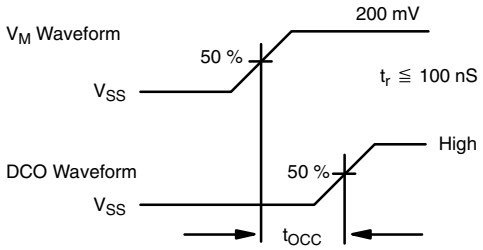



**Figure 1. OC Load Detect**

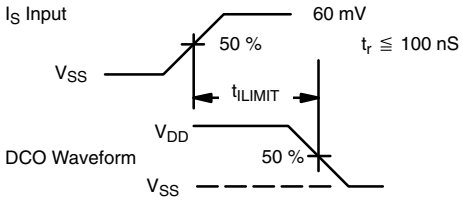



**Figure 2. Current-Limit Comparator Response Time**

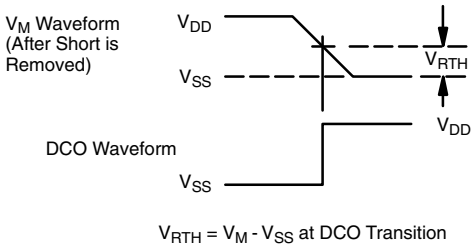



**Figure 3. Reset Threshold**

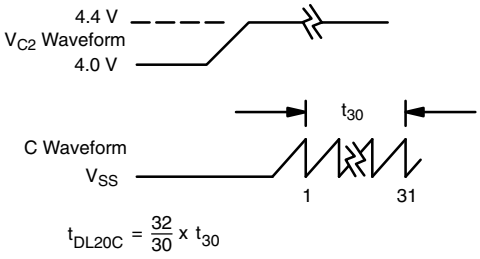



**Figure 4. DL2 Time (Over-Charge)**

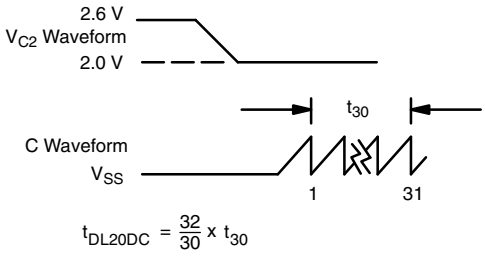



**Figure 5. DL2 Time (Over-Discharge)**

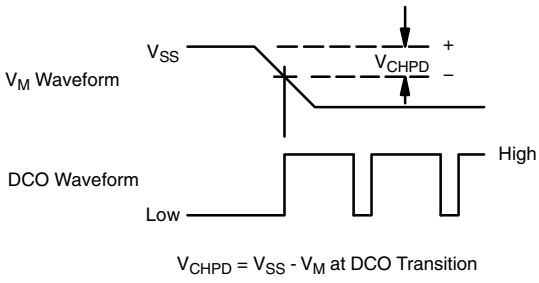



**Figure 6. Power-Down Charger Detect Threshold**

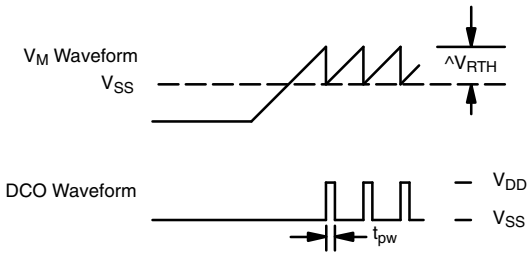
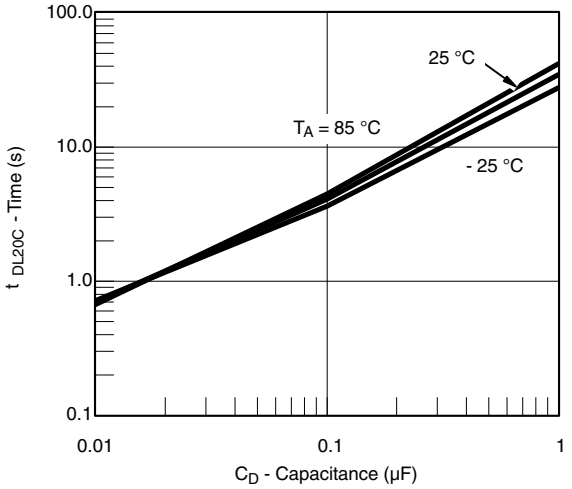
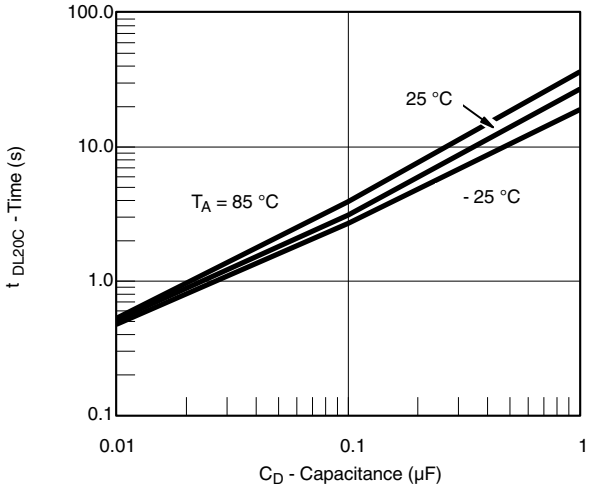



**Figure 7. Load Detection in Overcharge Mode**

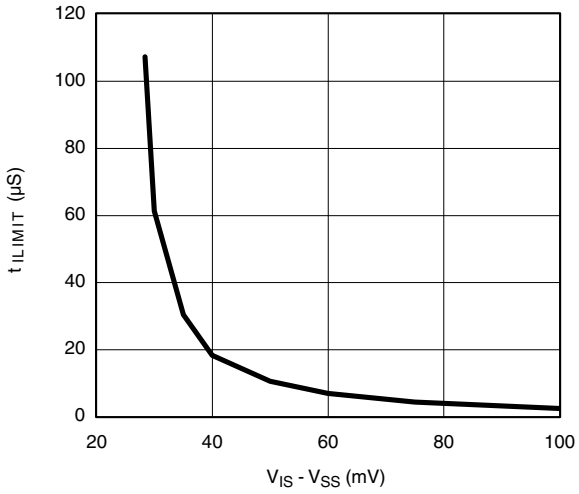
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



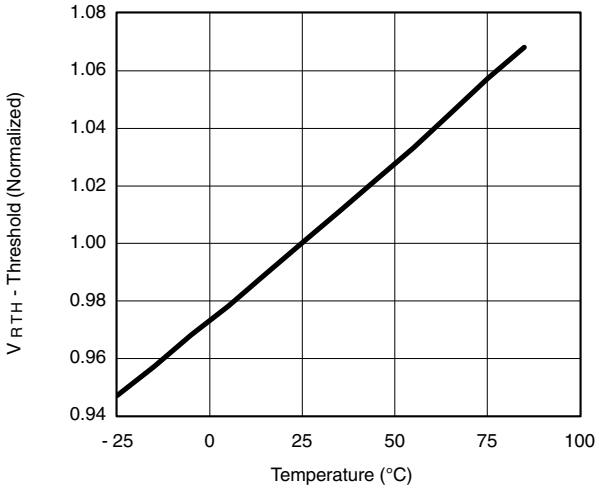

**DL2 Period (Over Charge) vs. Capacitance**



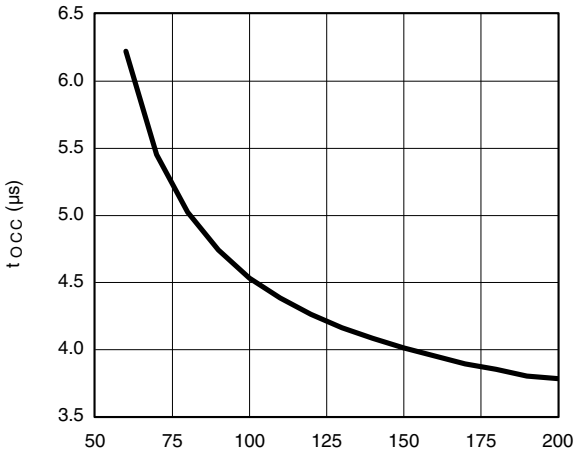

**DL2 Period (Over Discharge) vs. Capacitance**



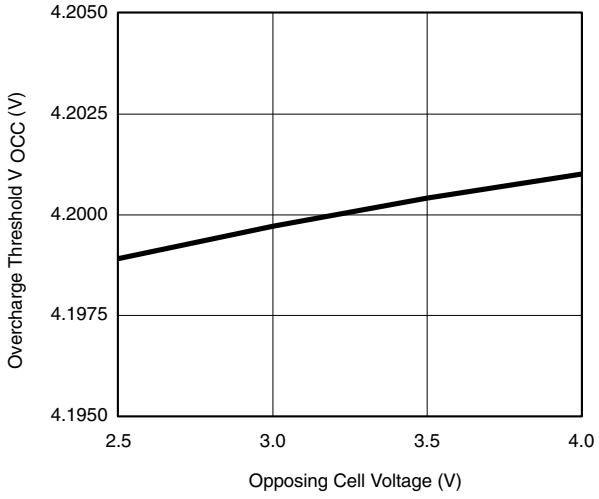

**Over Current Sense Voltage vs. Current Sense Time**




**Reset Threshold vs. Temperature**

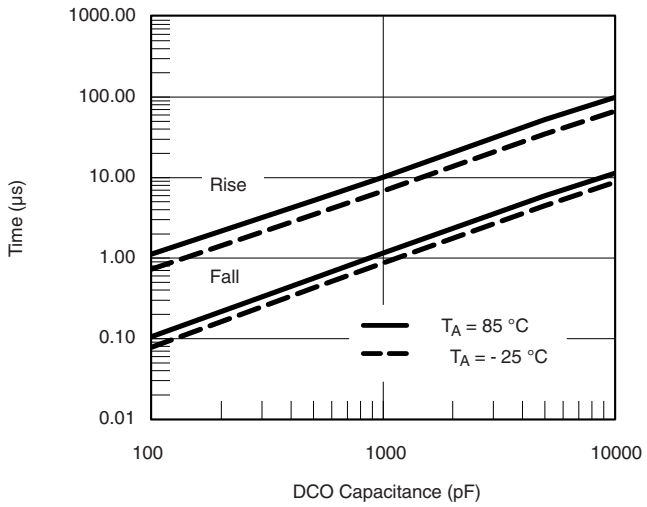



**Load Detect Time vs. $V_M$ - $V_{SS}$**



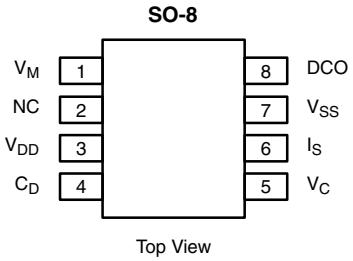

**Overcharge Threshold vs. Opposing Cell Voltage**

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted




**DCO Rise and Fall Times vs. Capacitance**

## PIN CONFIGURATION




| ORDERING INFORMATION | | |
|---|---|---|
| **Part Number** | **$V_{OC1/2}$ Typ.** | **Temp Range** |
| Si9730ABY-T1 | 4.20 V | - 25° to 85 °C |
| Si9730ABY-T1-E3 (Lead Free) | | |
| Si9730BBY-T1 | 4.25 V | |
| Si9730BBY-T1-E3 (Lead Free) | | |
| Si9730CBY-T1 | 4.22 V | |
| Si9730CBY-T1-E3 (Lead Free) | | |
| Si9730DBY-T1 | 4.32 V | |
| Si9730DBY-T1-E3 (Lead Free) | | |

| PIN DESCRIPTION | | |
|---|---|---|
| **Pin Number** | **Symbol** | **Description** |
| 1 | $V_M$ | Negative Battery Pack Terminal - connection for external negative terminal of the battery pack. |
| 2 | NC | No Connection, do not connect this pin. |
| 3 | $V_{DD}$ | Dual Cell Positive Terminal - connection for positive terminal of dual series connected LiI+ cells. |
| 4 | $C_D$ | Delay Capacitor Connection - an external capacitor connected across $C_D$ and Vss allows additional charge time (DL2, see Detailed Description ) after a charge error has occurred. Suggested capacitor values are shown in DL2 Period vs. Capacitance Curves. |
| 5 | $V_C$ | Dual Cell Center Tap Connection - monitors individual battery voltages for overcharge and overdischarge errors. |
| 6 | Is | Current Sense Comparator Input - monitors load current for short circuit conditions . If $V_{ILIMIT}$ is exceeded, then DCO opens the low-side switch, disconnecting the cell |
| 7 | $V_{SS}$ | Dual Cell Negative Terminal - connection for negative terminal of dual series connected LiI+ cells. |
| 8 | DCO | Low-side Switch Gate Driver Output - drives the gate of two external source connected N-Channel MOSFETs. DCO swings from $V_{OL}$ to $V_{DD}$. |

## DETAILED DESCRIPTION

### Overview

The purpose of the Si9730 is to safely and reliably control the charging and discharging of a two-cell lithium-ion battery (carbon or coke chemistry). It provides protection against all possible fault conditions, including:

- external short circuits
- reversed charger
- overcharged cell or cells
- undervoltage
- battery open center-tap

### General Concepts

The Si9730 operates by connecting or disconnecting the negative terminal of the battery to the negative side of the load and/or charger (see Figure 8); that is, it does ground side switching. It is important to bear the distinction between these two "grounds" in mind in order to understand the operation of the Si9730. The switching is accomplished by controlling two "back-to-back" MOSFETs: having the two MOSFETs in this arrangement is mandatory to ensure that current cannot flow in either direction when the MOSFETs are off. To turn the switch on, the Si9730 applies a gate-source voltage to both MOSFETs (from the DCO pin) that is high with respect to the sources. The Si9730 DCO signal is referenced to the $V_M$ pin while the battery is being charged, and to the Vss pin while the battery is being discharged. The Si9730 causes the DCO to be referenced to the lower of the two voltages. This prevents the switch from turning on or off unintentionally.

The Si9730 is designed to operate only with a current-limited lithium-ion battery charger. Specifically, the battery charger must have an open-circuit voltage that does not exceed the absolute maximum IC voltage, and it must have a limited short-circuit current that does not exceed the allowed charging current of the battery.

The following descriptions cover all the common operational scenarios; additional information on unusual battery conditions can be found in the state transition table.

### Normal Charging

The cells are in normal charging conditions if a) both cells are above the Over-Discharge Detect Threshold ($V_{ODC}$ ~ 2.2 V); b) both cells are under the Over-Charge Detect Threshold ($V_{OC}$ ~ 4.2 V); and c) the center tap is connected to the $V_C$ pin. When a charger is present in these conditions, the switch will be on, charging the cells at the current limit of the charger.

### Normal Discharging

The cells are in normal discharging conditions if a, b, and c above are satisfied, and if in addition d) the load current is less than the discharge current limit. With no charger present, the switch will be on, discharging the cells and powering the load.

### Overcharged Cell(s) Charging

The most destructive condition that a LiI+ cell can experience is overcharging. If the cell becomes overcharged beyond its recommended limits, it can become permanently disabled.

If one or both cells rise above the over-charge detect threshold ($V_{OC1}$ and $V_{OC2}$), and a charger is present, the Si9730 will open the switch (to prevent further charging) and begin bleeding off charge (15 µA typical) from the overcharged cell or cells.

The details of this operation depend on the fact that the voltage level of lithium-ion batteries drops for a short time after charging ceases (due to momentary changes in battery chemistry, ESR, etc.). Because of this recovery, the Si9730 allows the battery to continue charging for a short time (the overcharge time, $t_{DL2OC}$). This additional charge time only occurs if the overcharge condition persists for more than 8 msec (two periods of an internal 4msec oscillator). $T_{DL2OC}$ is determined by the capacitor attached to the $C_D$ pin, see Figure 8.

Once the overcharge time has ended, the switch is opened, preventing the battery from further overcharging. Now, the Si9730 begins bleeding current off the overcharged cell or cells ($I_{BAL1}$ and $I_{BAL2}$), as long as a charger is present. Eventually, the cell(s) will return into their normal range, and charging will begin, starting the whole cycle over again.

### Overcharged Cell(s) Discharging

If one or more cells is overcharged, and a load is connected, the switch is turned on, permitting the battery to power the load.

### Over-Discharged Cell(s) Discharging

Repeated over-discharging of LiI+ cells can cause irreversible reactions in the cells which lead to decreased cycle life. To avoid this, if one or both cells becomes over-discharged ($V_{CELL} < V_{ODC}$) and no charger is present, the Si9730 opens the switch to prevent further discharging, and goes into a shutdown mode in which it draws minute power from the battery ($I_{DD\_UVL}$ < 1 µA).

### Over-Discharged Cell(s) Charging

If one or both cells is over-discharged, and a charger is present, charging can begin, and so the Si9730 closes the switch. However, removal of the charger in this condition could potentially damage the battery if the removal is not recognized and the cells are discharged. Since the voltage drop across the switch is small, the Si9730 actually cycles the switch at a 7/8 duty cycle; during the 1/8 time when the switch is open, the IC checks that the charger is still present.

Once both cells are back into the normal operating range, normal charging resumes.

### Undervoltage Charging

If for some reason the battery drops below about 3.7 V ($V_{UVL}$), there is insufficient voltage for the Si9730 to properly monitor fault conditions. Of course, the switch is already open, since $V_{UVL} < V_{ODC} \times 2$. However, when a charger is detected, the Si9730 recovers and goes into an undervoltage mode. (A charger is detected if the $V_S$ pin is higher than the $V_M$ pin by at least $V_{CHPD}$ = 1.1 V, see Figure 6). In this undervoltage mode, the switch is on at a 1/8 duty cycle, to limit the power dissipation across the switch, and, again, to detect the continuing presence of the charger.

Once the battery voltage is above $V_{UVL}$, the charging continues in the over-discharged state.

### Output Short

If too much current is drawn from the battery due to a load short, the switch must be opened quickly to prevent damage to the battery. The Si9730 monitors the load current by looking at the voltage across an external sense resistor (see Figure 8). If the voltage across the sense resistor exceeds $V_{ILIMIT}$ ~ 28 mV, the switch is opened. The Si9730 leaves the switch open until the load is *completely* removed.

Of course, the IC must have some way of detecting that the load *has* been removed. For this purpose, a small current ($I_{VMSHORT}$) passes through the Si9730, from pin $V_M$ to pin $V_{SS}$ once the short is detected and the switch is turned off. The $I_{VMSHORT}$ current causes the voltage on the $V_M$ pin to equal the voltage on the $V_{DD}$ pin while the short is present, or the voltage on the $V_M$ pin to equal the voltage on the $V_{SS}$ pin if the short is removed. If the short is not removed, $I_{VMSHORT}$ current will continue to flow until the battery voltage becomes overdischarged. Once the short is removed, the IC is allowed to turn the switch back on.

The current limit threshold has a temperature coefficient of 0.18 %/°C. This can partially compensate for a copper circuit board trace being used as the sense resistor.

### Open Center Tap

An open center tap is a mechanical failure of the battery pack such that the Si9730's $V_C$ pin is disconnected from the center point of the two-cell battery. If this connection is open, the IC opens the switch, as it cannot measure the cell voltages in this condition. The switch is left open until connection is re-established. If the battery is under-voltaged and the charger is present in this case, the battery is allowed to charge even with the center tap open. In this state, batteries are almost impossible to damage by 1/8 duty cycle charging. Once the battery voltage reaches the over-discharged voltage, the switch is turned off.

### State Transition Table

The number of different states of the Si9730 can seem overwhelming at first. This state transition table will help to organize thinking about the different operational conditions of the IC, by listing each possible transition from one condition to another.

Reading the table is straightforward. There are two cells constituting the battery, one with its positive terminal connected to $V_{DD}$ and its negative terminal connected to $V_C$, referred to as the high cell (see Figure 8); and one cell with its positive terminal connected to $V_C$ and its negative terminal connected to $V_{SS}$, referred to as the low cell. Each cell can be in one of three voltages:

- Over-discharge (ODC), where $V_{CELL} < V_{ODC}$;
- Normal Operation (NO), where $V_{ODC} < V_{CELL} < V_{OC}$;

or

- Overcharge (OC), where $V_{OC} < V_{CELL}$.

Additionally, the battery as a whole can be undervoltage (UV), where $V_{BATTERY} < V_{UVL}$. Note that this final condition is not *necessarily* (though normally) mutually exclusive with the other cell conditions: if one cell were at 0 V, the other cell could be in NO, and the battery could still be in UV.

The charger can be either present (ON) or not present (OFF); the "X" in the table means the condition is true regardless of the state of the charger. The load current can be either 0, normal ($0 < I_{LOAD} < I_{ILIMIT}$) or a short ($I_{ILIMIT} < I_{LOAD}$) where $I_{ILIMIT}$ is set by $V_{ILIMIT}/R_{SENSE}$; the "X" in the table refers to a load current that can be either 0 or normal. Finally, the switch can be either ON, OFF, or cycling at either 1/8 or 7/8 duty cycle, where the duty cycle refers to the portion of the period when the switch is on; the notation On->On simply means that the switch does not change state, it remains on; the notation ->Off means that the switch turns off regardless of its previous state.

| STATE TRANSITION TABLE | | | | |
|---|---|---|---|---|
| **High-Cell Voltage** | **Low-Cell Voltage** | **Charger On/Off** | **Load Current** | **Switch State** |
| NO | NO | Off>On | X | On->On |
| NO->OC | NO | Off | 0 | On->Off |
| NO | NO->OC | Off | 0 | On->Off |
| NO->OC | NO | Off | Normal | Cycles at very high duty cycle |
| NO | NO->OC | Off | Normal | Cycles at very high duty cycle |
| OC | NO | Off->On | X | Off->Off |
| NO | OC | Off->On | X | Off->Off |
| OC | OC | Off->On | X | Off->Off |
| NO | NO | Off | Normal->Short | On->Off |
| OC | NO | Off | Normal->Short | On->Off |
| NO | OC | Off | Normal->Short | On->Off |
| NO->ODC | NO | Off | 0 | On->Off |
| NO | NO->ODC | Off | 0 | On->Off |
| NO->ODC | NO | Off | Normal | On->Off |
| NO | NO->ODC | Off | Normal | On->Off |
| ODC | NO | Off->On | X | Off->Cycle at 7/8 duty cycle |
| NO | ODC | Off->On | X | Off->Cycle at 7/8 duty cycle |
| ODC | ODC | Off->On | X | Off->Cycle at 7/8 duty cycle |
| UV | | Off->On | X | Off->Cycle at 1/8 duty cycle |
| NO->ODC | OC | Off | 0 | Cycle->Off |
| OC | NO->OC | Off | 0 | Off |
| NO | NO | V<0 | X | Off |
| UV | | On | Center Tap->Open | Cycle at 1/8 duty cycle |
| ODC | ODC | X | Center Tap->Open | ->Off |
| NO | ODC | X | Center Tap->Open | ->Off |
| ODC | NO | X | Center Tap->Open | ->Off |
| NO | NO | X | Center Tap->Open | ->Off |
| OC | OC | X | Center Tap->Open | ->Off |

## APPLICATION CIRCUIT

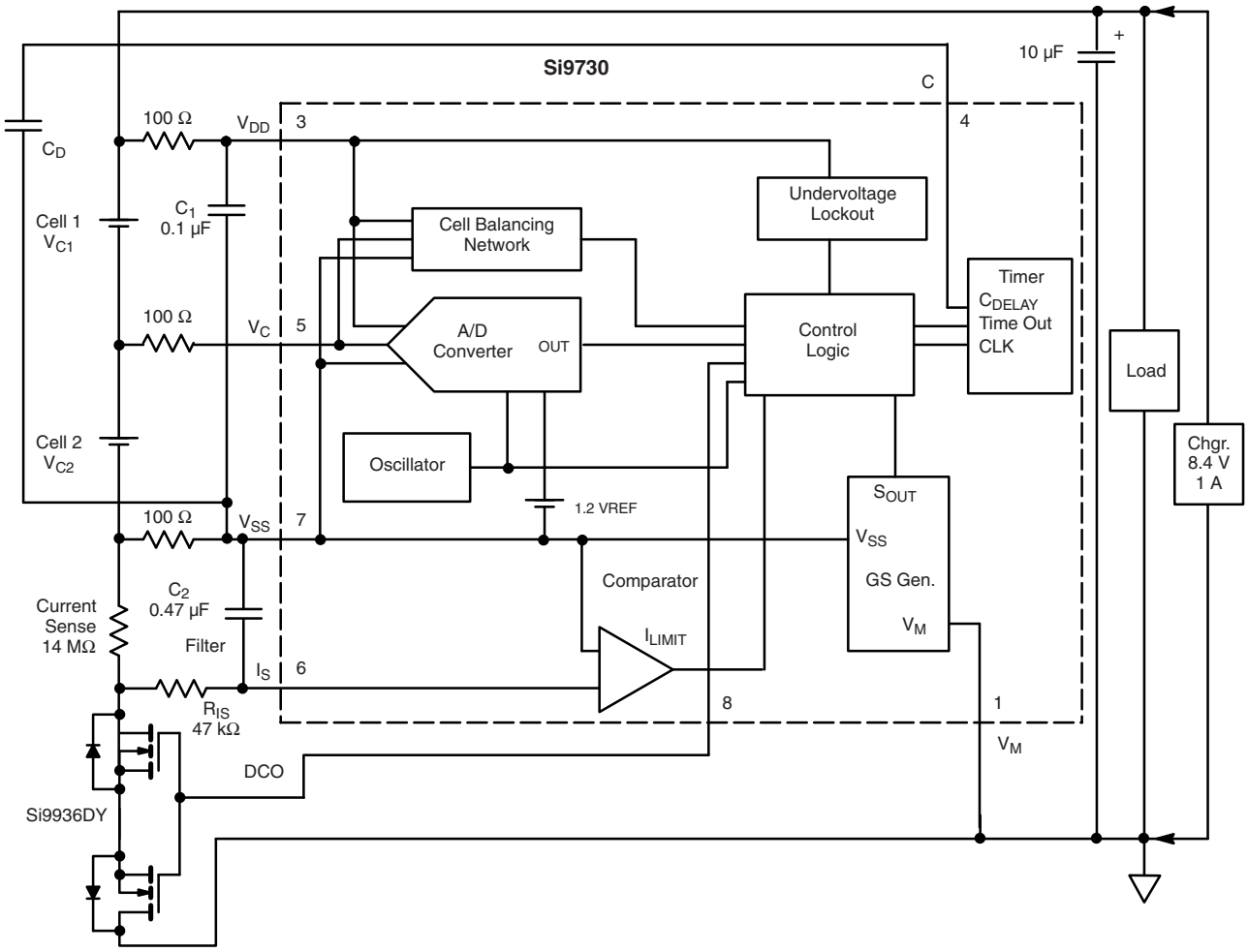



**Figure 8. Typical 2 -Cell Circuit**

## GENERAL CONSIDERATIONS

Figure 8 shows a typical application of the Si9730, controlling a 2-cell lithium-ion battery (carbon or coke chemistry). Specifics of the selection of MOSFETs, current sensing resistor, and output capacitor are detailed below. In addition, there are several typical features of this circuit to be observed.

First, each connection from a cell to the IC has a 100 Ω resistor in series with it. The purpose of the resistor is to ensure that in the unlikely event of the IC shorting, the cells themselves will not see a short. The maximum size of this resistance is set by the current drain of the IC; for example, the $V_{DD}$ pin draws a maximum of 60 µA, which will drop V = 60 µA * 100 Ω = 6 mV across the resistor. This drop constitutes an error in the measured cell voltage, and so the resistor must be small enough that the error voltage is acceptable.

A second typical feature demonstrated in Figure 8 is the current sense filter formed by RIS and C2. This provides a noise filter, to prevent the Si9730 from opening the connection to the battery if there is noise on its current sense pin. It also causes a delay in the response of the IC to a genuine overcurrent, the amount of the delay being inversely proportional to the amount of overcurrent, since the Is pin senses a voltage. Increasing this filter's time constant could be used to allow short-time surges of current out of the battery without compromising its ability to protect the battery.

### Output Capacitor

Depending on the MOSFET selected, the Si9730 can open the switch quite rapidly, in a matter of a few microseconds. However, the various monitoring operations take 10-100 times longer than this, and the basic period of the Si9730's oscillator is 4 msec. In order to prevent false readings by the Si9730, it is necessary to attach a capacitor across the output of the battery charger/load (this is not in parallel with the battery, because of the switch). A 10 µF capacitor is recommended for this purpose; see Figure 8.

### Selecting a Current Sense Resistor

The current sense resistor should be selected based on the maximum current the battery can source or charge at; above this current, the Si9730 will open the switch, disconnecting the battery from its load or charger.

$$R_{sense} = V_{ILIMIT}/I_{ILIMIT} \approx 28\ mV/I_{ILIMIT}$$

Of course, the resistor must be rated to take the power dissipated in it as well:

$$P_{RSENSE} = I_{ILIMIT} * V_{ILIMIT} \approx 28\ mV * I_{ILIMIT}$$

For example, suppose that the maximum current the battery will see is 1.8 A. Then, $I_{LIMIT}$ might be chosen to be 2 A. We would then select a resistor of

$$R_{SENSE} = 28\ mV/2\ A = 14\ m\Omega.$$

The power dissipation in this resistor is

$$P_{RSENSE} = 28\ mV * 2\ A = 56\ mW$$

and so a 100 mW surface mount resistor would be suitable.

Another possibility is to use a thin copper trace as the sense resistor. The copper has a temperature coefficient of 0.39 %/°C, but this is partially compensated for by the temperature coefficient of the current limit comparator in the Si9730, which is 0.18 %/°C. A simple formula for selecting a trace to act as a current sensor is:

$$R = 0.5\ m\Omega \times \frac{\text{length}}{\text{width}} (1\ \text{oz. Copper})$$

For example, to get a 14 mΩ. resistor, we need length/width = 28; with a trace width of 0.01", the length of the trace should be 0.28".

### MOSFET Selection

Two MOSFETs in series, with their sources and gates connected together, are used as the switch. This prevents current from flowing in either direction when the gate is low; if only one MOSFET were used, the body diode could conduct current in the opposing direction.

LITTLE FOOT® MOSFETs are recommended for this application, because of their size, performance and cost benefits. SO-8 and TSSOP-8 MOSFETs allow for space efficient designs with performance equal to or better than their DPAK and TO-220 predecessors. Further, their availability from multiple sources permits a cost effective solution.

There are two important parameters to consider in MOSFET selection: gate threshold voltage; and on-resistance, which determines power dissipation.

Even when the DCO pin of the Si9730 is low, the specification allows its value to be as high as 0.4 V. If this voltage were close to the gate threshold voltage, leakage current through the MOSFETs could be hundreds of microamps, which would result in the battery quickly becoming discharged. To ensure that leakage is minimized, N-Channel MOSFETs with a minimum gate threshold voltage of 0.8 V should be chosen.

On resistance of the MOSFETs needs to be selected to limit power dissipation into the MOSFETs' package. For example, a dual MOSFET SO-8 package is rated at 2 W, and a dual MOSFET TSSOP-8 package is rated at 1 W (both at 25 °C; if the ambient temperature is higher, the allowable power dissipation in these packages is less). For example, if the maximum current is 2 A, and a dual MOSFET SO-8 package is being used, the maximum on-resistance of the two MOSFETs in series must not exceed

$$1\ W = (2\ A)^2 * R_{ON}$$

or $R_{ON} = 0.25\ \Omega$; each MOSFET can be allotted half of this, $R_{ON} = 125\ m\Omega$. Account must also be taken of the fact that MOSFETs' on-resistance is a function of temperature; a conservative approach would give a discount of 1/3, $R_{ON} = 125\ m\Omega * (2/3) = 80\ m\Omega$ per MOSFET.

A list of recommended MOSFETs, which Vishay Siliconix supplies, follows.

| N-CHANNEL MOSFET SELECTION GUIDE | | | | | | | |
|---|---|---|---|---|---|---|---|
| Part Number | $r_{DS\ (on)}$ (Ω) at $V_{GS}$ = 10 V | $r_{DS(on)}$ (Ω) at $V_{GS}$ = 4.5 V | $I_D$ (A) | $V_{GS(th)}$ (V) | Config. | Package | Recommended Application Current (A) at 25 °C |
| Si4410DY | 0.0135 | 0.020 | 10 | 1.0 | Single | SO-8 | 9 |
| Si4412DY | 0.028 | 0.042 | 7 | 1.0 | Single | SO-8 | 6.3 |
| Si6434DQ | 0.028 | 0.042 | 5.6 | 1.0 | Single | TSSOP-8 | 4.9 |
| Si4936DY | 0.037 | 0.055 | 5.8 | 1.0 | Dual | SO-8 | 3.5 |
| Si9936DY | 0.050 | 0.080 | 5 | 1.0 | Dual | SO-8 | 2.9 |
| Si6954DQ | 0.065 | 0.095 | 3.9 | 1.0 | Dual | TSSOP-8 | 1.9 |

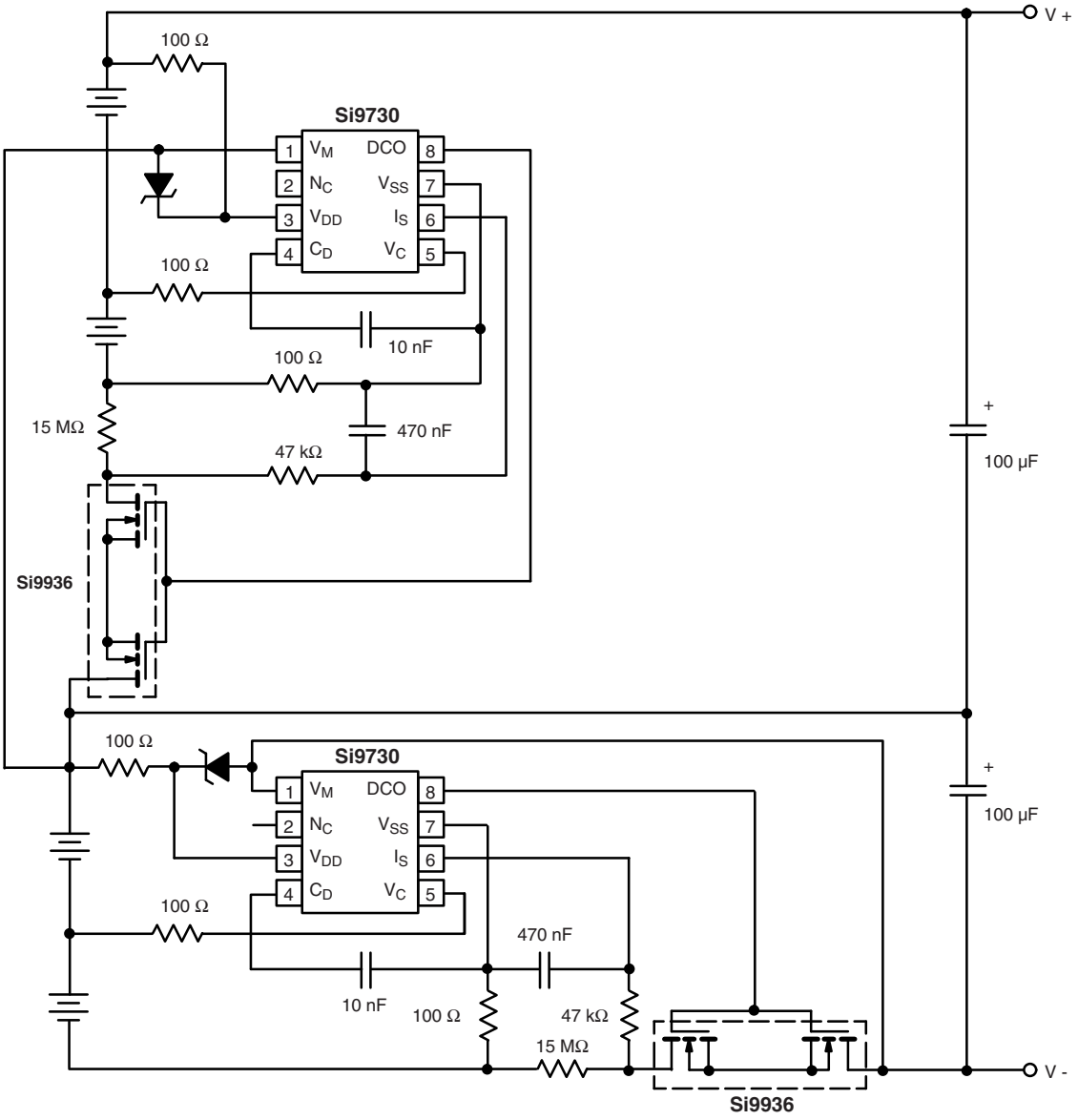



**Figure 9. 4-Cell Battery Circuit**

### Four Cell Application

Figure 9 shows a method for using the Si9730 in a 4-cell application. Basically, this is two complete 2-cell circuits stacked in series. Each half of the complete circuit monitors its own 2-cell portion of the battery, and opens its own MOSFET switch under any of the appropriate conditions. Observe that the total percent power loss in this circuit is identical to that in the 2-cell application; although there are now two sets of MOSFETs in series, there is also double the battery voltage, and so total efficiency is the same.

One novel feature of this 4-cell circuit is the increase in the size of the bypass capacitors. Each half of the circuit retains its own output cap, to reduce noise seen by the circuit. Since the two halves interact with each other (when one opens its switch, the other one is also opened), there can be additional noise, which must be rejected for proper operation. The capacitors have been increased to 100 µF for this reason; remember that they must be rated to take the full maximum voltage rating of the charger, not half of it, since if one switch is closed and the other open, the charger (minus two cells' voltage drop, which might be zero) is applied across the other capacitor.

A second addition on this circuit is the (optional) two zeners, one each for each Si9730, placed from $V_{DD}$ to $V_M$. These are necessary only if the charger voltage is higher than the 15 V absolute maximum of the IC plus two cells' voltage drop. Just as with the capacitor, if one switch is open and the other closed, the IC will see this charger voltage, and must be protected. The power rating of the zener can be inferred by observing that the current through it is limited by the 100 Ω resistor. A trade off can be made here between the power rating of the zener, which can be decreased by increasing the resistor value, and the accuracy of the voltage measurement by the Si9730, which can be increased by decreasing the resistor value.

### Reset from Shutdown

There are two specialized conditions that can place the Si9730 in shutdown mode. The first condition can occur when the circuit is first attached to a battery in the factory. When the IC comes up, it will be in the undervoltage shutdown mode. The Si9730 may also enter this mode when the ambient temperature drops and the battery is nearly in UV. When the temperature drops, the battery pack voltage will drop and the IC may enter the shutdown mode. In either case, the Si9730 must be reset by raising the $V_{SS}$ pin higher than the $V_M$ pin by $V_{CPHD}$. Figure 10 shows a circuit that resets the circuit once it has entered the shutdown mode.

The circuit works by initially connecting the 0.1 µF capacitor to the battery's center tap and placing the switch in position #1. Although the MOSFETs are open, the 1 mΩ resistor is sufficient to allow the capacitor to charge up in about 300 - 400 msec. Once the capacitor is charged, the switch is placed in position #2, momentarily making $V_{SS}$ higher than $V_M$, thus placing the Si9730 in the normal operating mode. The entire circuit provides a leakage of only a few microamps, which is much lower than the self discharge current of the LiIon battery.

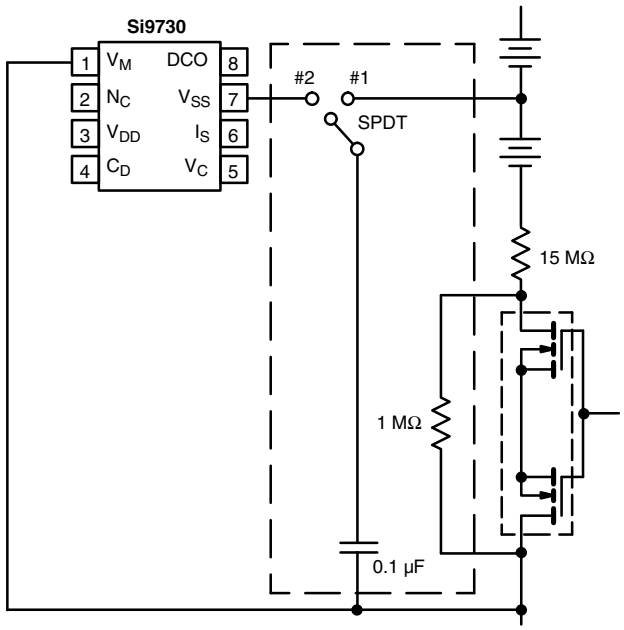



**Figure 10. Factory Startup Circuit**

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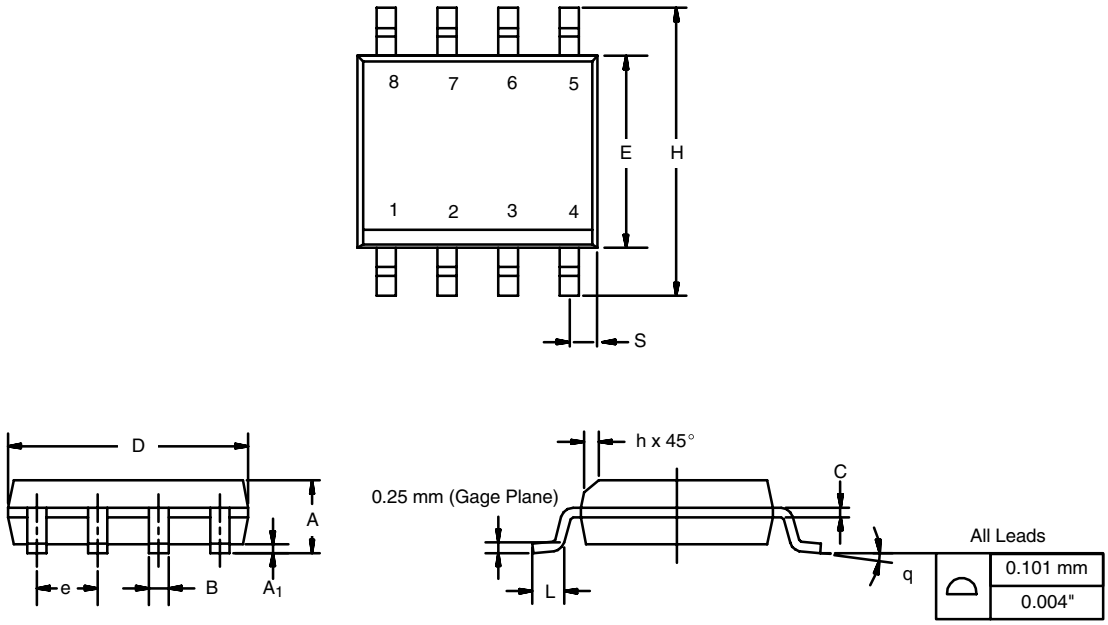
**SOIC (NARROW): 8-LEAD**
JEDEC Part Number: MS-012




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| $A_1$ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |
| ECN: C-06527-Rev. I, 11-Sep-06<br>DWG: 5498 | | | | |

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