

## 500-kHz Half-Bridge DC/DC Controller with Integrated Secondary Synchronous Rectification Drivers

### DESCRIPTION

Si9122E is a half-bridge controller IC ideally suited to fixed telecom applications where high efficiency is required at low output voltages (e.g. < 3.3 V). Designed to operate within the fixed telecom voltage range of 36 V to 75 V, the IC is capable of controlling and driving both the low and high-side switching devices of a half bridge circuit and also controlling the switching devices on the secondary side of the bridge. Due to the very low on-resistance of the secondary MOSFETs, a significant increase in conversion efficiency can be achieved as compared with conventional Schottky diodes. Control of the secondary devices is by means of a pulse transformer and a pair of inverters. Such a system has efficiencies well in excess of 90 % even for low output voltages.

On-chip control of the dead time delays between the primary and secondary synchronous signals keep efficiencies high and prevent shorting of the power transformer. An external resistor sets the oscillator frequency from 200 kHz to 500 kHz.

Si9122E has advanced current monitoring and control circuitry which allow the user to set the maximum current in the primary circuit. Such a feature acts as protection against output shorting and also provides constant current into large capacitive loads during start-up or when paralleling power supplies. Current sensing is by means of a sense resistor on the low-side primary device.

### FEATURES

- 92 % primary/secondary duty cycle
- 135 °C over temperature protection
- Compatible with ETSI 300 132-2
- 28 V to 75 V input voltage range
- Integrated  $\pm 1$  A half bridge primary drivers
- Secondary synchronous rectifier control signals with programmable deadtime delay
- Voltage mode control
- Voltage feedforward compensation
- High voltage pre-regulator operates during start-up
- Current sensing on low-side primary device
- Frequency foldback eliminates constant current tail
- Advanced maximum current control during start-up and shorted load
- Low input voltage detection
- Programmable soft-start function



RoHS  
COMPLIANT

### APPLICATIONS

- Network cards
- Power supply modules
- Distributed power systems
- Intermediate bus converter
- Brick converter

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

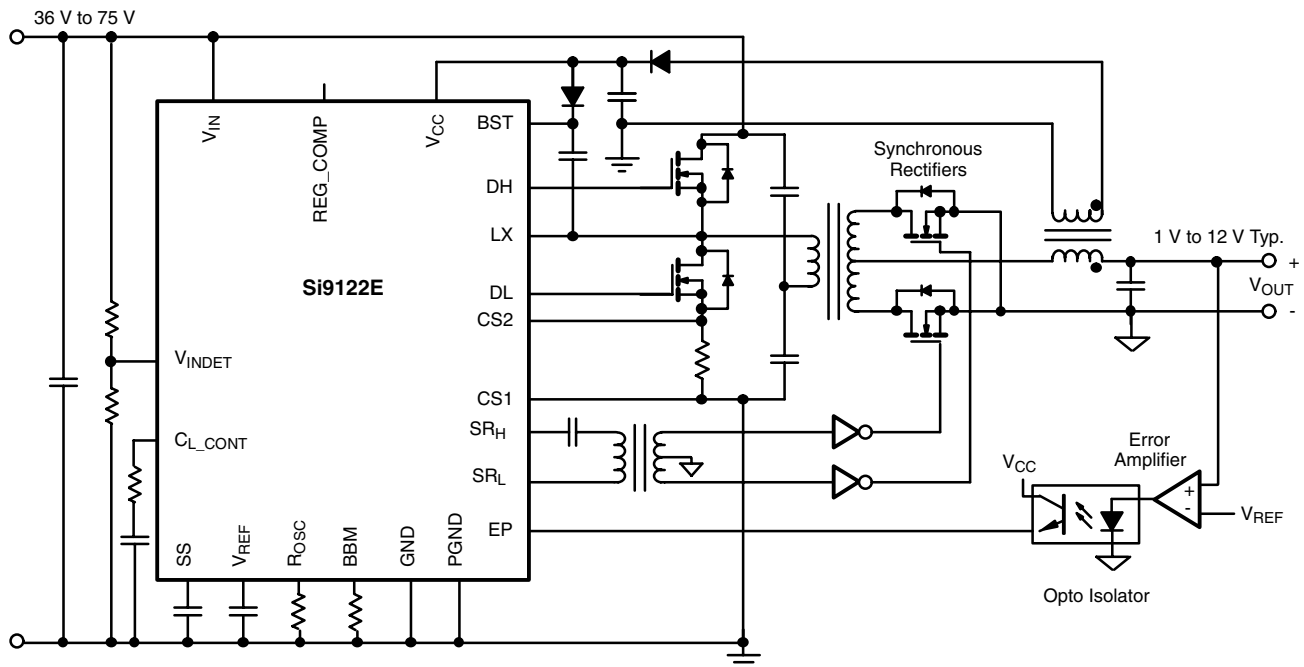


Figure 1.

## TECHNICAL DESCRIPTION

Si9122E is a voltage mode controller for the half-bridge topology. With 100 V depletion mode MOSFET, the Si9122E is capable of powering directly from the high voltage bus to  $V_{CC}$  through an external PNP pass transistor, or may be powered through an external regulator directly through the  $V_{CC}$  pin. With PWM control, Si9122E provides peak efficiency throughout the entire line and load range. In order to simplify the design of efficient secondary synchronous rectification circuitry, the Si9122E provides intelligent gate drive signals to control the secondary MOSFETs. With independent gate drive signals from the controller, transformer design is no longer limited by the gate to source rating of the secondary-side MOSFETs. Si9122E provides constant  $V_{GS}$  voltage, independent of the line voltage to minimize the gate charge loss as well as conduction loss.

To prevent shoot-through current or transformer shorting, adjustable Break-Before-Make (BBM) time is incorporated into the IC and is programmed by an external precision resistor.

Si9122E is assembled in lead (Pb)-free TSSOP-20 and MLP65-20 packages. To satisfy stringent ambient temperature requirements, Si9122E is rated to handle the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . When a situation arises which results in a rapid increase in primary (or secondary) current such as output shorted or start-up with a large output capacitor, control of the PWM generator is handed over to the current loop. Monitoring of the load current is by means of an external current sense resistor in the source of the primary low-side switch. With the lower OTP set at  $135^{\circ}\text{C}$ , the DNF20 package improves the thermal headroom.

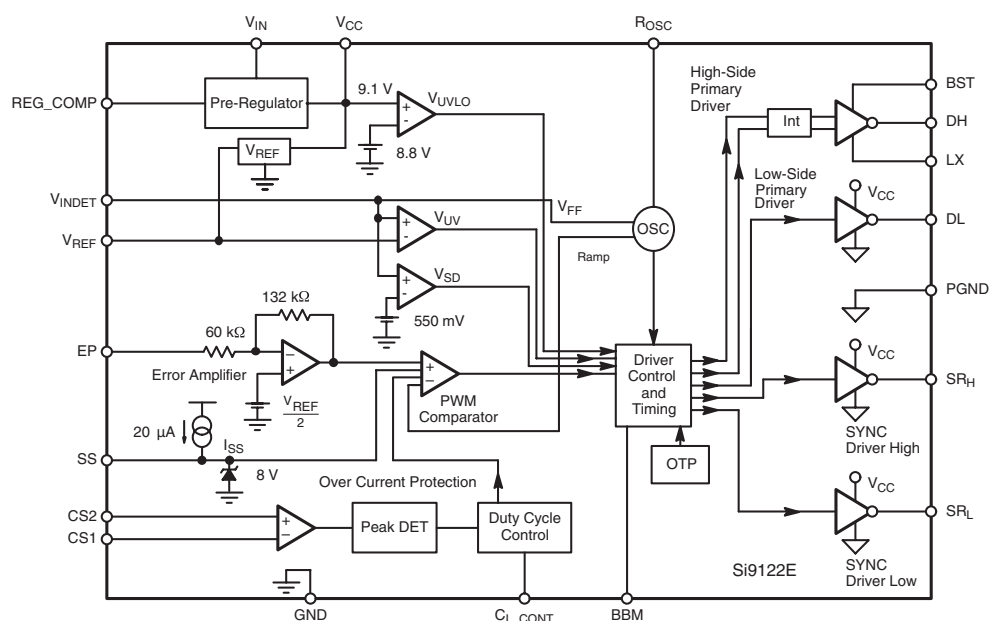


Figure 2.

ABSOLUTE MAXIMUM RATINGS All voltages referenced to GND = 0 V			
Parameter		Limit	Unit
$V_{IN}$ (Continuous)		80	V
$V_{IN}$ (100 ms)		100	
$V_{CC}$		14.5	
$V_{BST}$	Continuous	95	
	100 ms	113.2	
$V_{LX}$		100	
$V_{BST} - V_{LX}$		15	
$V_{REF}$ $R_{OSC}$		- 0.3 to $V_{CC} + 0.3$	
Logic Inputs		- 0.3 to $V_{CC} + 0.3$	
Analog Inputs		- 0.3 to $V_{CC} + 0.3$	
HV Pre-Regulator Input Current	Continuous	5	mA



<b>ABSOLUTE MAXIMUM RATINGS</b> All voltages referenced to GND = 0 V			
Parameter		Limit	Unit
Storage Temperature		- 65 to 150	°C
Operating Junction Temperature		150	
Power Dissipation <sup>a</sup>	TSSOP-20 <sup>b</sup>	850	mW
	MLP65-20 <sup>c</sup>	2500	
Thermal Impedance ( $\theta_{JA}$ )	TSSOP-20	75	°C/W
	MLP65-20	38	

Notes:

a. Device mounted on JEDEC compliant 1S2P test board.

b. Derate 14 mW/°C above 25 °C.

c. Derate 26 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<b>RECOMMENDED OPERATING RANGE</b> All voltages referenced to GND = 0 V			
Parameter		Limit	Unit
$V_{IN}$		36 to 75	V
$V_{CC}$		10.5 to 13.2	
$CV_{CC}$		$\geq 4.7$	$\mu F$
$f_{OSC}$		200 to 500	kHz
$R_{OSC}$		30 to 72	$k\Omega$
$R_{BBM}$		22 to 50	
$C_{REF}$		0.1	$\mu F$
$C_{BOOST}$		0.1	
Analog Inputs		0 to $V_{CC} - 2$	V
Digital Inputs		0 to $V_{CC}$	
Reference Voltage Output Current		0.1 to 2.5	mA

SPECIFICATIONS <sup>a</sup>						
Parameter	Symbol	Test Conditions Unless Otherwise Specified f <sub>NOM</sub> = 500 kHz, V <sub>IN</sub> = 75 V V <sub>INDET</sub> = 7.5 V; 10.5 V ≤ V <sub>CC</sub> ≤ 13.2 V	Limits - 40 to 85 °C			Unit
			Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
Reference (3.3 V)						
Output Voltage	V <sub>REF</sub>	V <sub>CC</sub> = 12 V, 25 °C Load = 0 mA	3.2	3.3	3.4	V
Short Circuit Current	I <sub>SREF</sub>	V <sub>REF</sub> = 0 V			- 50	mA
Load Regulation	dVr/dir	I <sub>REF</sub> = 0 to - 2.5 mA		- 30	- 75	mV
Power Supply Rejection	PSRR	at 100 Hz		60		dB
Oscillator						
Accuracy (1 % R <sub>OSC</sub> )		R <sub>OSC</sub> = 30 kΩ, f <sub>NOM</sub> = 500 kHz	- 20		20	%
Max Frequency <sup>g</sup>	F <sub>MAX</sub>	R <sub>OSC</sub> = 22.6 kΩ	400	500	600	kHz
Foldback Frequency <sup>d</sup>	F <sub>FOBK</sub>	f <sub>NOM</sub> = 500 kHz, V <sub>CS2</sub> - V <sub>CS1</sub> > 150 mV		100		
Error Amplifier						
Input Bias Current	I <sub>BIAS</sub>	V <sub>EP</sub> = 0 V	- 40		- 15	μA
Gain	A <sub>V</sub>			- 2.2		V/V
Bandwidth	BW			5		MHz
Power Supply Rejection	PSRR	at 110 Hz		60		dB
Slew State	SR			0.5		V/μs

SPECIFICATIONS <sup>a</sup>								
Parameter	Symbol	Test Conditions Unless Otherwise Specified f <sub>NOM</sub> = 500 kHz, V <sub>IN</sub> = 75 V V <sub>INDET</sub> = 7.5 V; 10.5 V ≤ V <sub>CC</sub> ≤ 13.2 V		Limits - 40 to 85 °C			Unit	
				Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>		
Current Sense Amplifier								
Input Voltage CM Range	V <sub>CM</sub>	V <sub>CS1</sub> - GND, V <sub>CS2</sub> - GND			± 150		mV	
Current Sense Amplifier								
Input Amplifier Gain	A <sub>VOL</sub>				17.5		dB	
Input Amplifier Bandwidth	BW				5		MHz	
Input Amplifier Offset Voltage	V <sub>OS</sub>				± 5		mV	
C <sub>L_CONT</sub> Current	I <sub>CL_CONT</sub>	dV <sub>CS</sub> = 0			120		μA	
		dV <sub>CS</sub> = 100 mV			0			
		dV <sub>CS</sub> = 100 mV			> 2		mA	
Lower Current Limit Threshold	V <sub>TLCL</sub>	I <sub>PD</sub> = I <sub>PU</sub> - I <sub>CL_CONT</sub> = 0			100		mV	
Upper Current Limit Threshold	V <sub>THCL</sub>	I <sub>PD</sub> > 2 mA			150			
Hysteresis		I <sub>PU</sub> < 500 μA			- 50			
C <sub>L_CONT</sub> Clamp Level	C <sub>L_CONT</sub>	I <sub>PU</sub> = 500 μA		0.6		1.5	V	
PWM Operation								
Duty Cycle	D <sub>MAX</sub>	f <sub>OSC</sub> = 500 kHz, 25 °C V <sub>INDET</sub> = 4.8 V, V <sub>IN</sub> = 48 V	V <sub>EP</sub> = 0 V	Primary	88	91	94	%
				Secondary	90	93	95	%
	D <sub>MIN</sub>	V <sub>EP</sub> = 1.75 V			< 17			
		V <sub>CS2</sub> - V <sub>CS1</sub> > 150 mV			3			
Pre-Regulator								
Input Voltage	+ V <sub>IN</sub>	I <sub>IN</sub> = 10 μA		36		75	V	
Input Leakage Current	I <sub>LKG</sub>	V <sub>IN</sub> = 75 V, V <sub>CC</sub> > V <sub>REG</sub>				10	μA	
Regulator Bias Current	I <sub>REG1</sub>	V <sub>IN</sub> = 75 V, V <sub>INDET</sub> < V <sub>SD</sub>			86	200		
	I <sub>REG2</sub>	V <sub>IN</sub> = 75 V, V <sub>INDET</sub> > V <sub>REF</sub>			8	14	mA	
Regulator_Comp	I <sub>SOURCE</sub>	V <sub>CC</sub> = 12 V		- 29	- 19	- 9	μA	
	I <sub>SINK</sub>			50	82	110		
Pre-Regulator drive Capability	I <sub>START</sub>	V <sub>CC</sub> < V <sub>REG</sub>		20			mA	
V <sub>CC</sub> Pre-Regulator Turn Off Threshold Voltage	V <sub>REG1</sub>	V <sub>INDET</sub> > V <sub>REF</sub>	T <sub>A</sub> = 25 °C	7.4	9.1	10.4	V	
	V <sub>REG2</sub>				8.5	9.1		9.7
Undervoltage Lockout	V <sub>UVLO</sub>	V <sub>CC</sub> Rising	T <sub>A</sub> = 25 °C		9.2			
				7.15	8.8	9.8		
V <sub>ULVO</sub> Hysteresis <sup>f</sup>	V <sub>UVLOHYS</sub>			8.1	8.8	9.3		
					0.5			
Soft-Start								
Soft-Start Current Output	I <sub>SS</sub>	Start-Up Condition		12	20	28	μA	
Soft-Start Completion Voltage	V <sub>SS_COMP</sub>	Normal Operation		7.35	8.05	8.85	V	
Shutdown								
V <sub>INDET</sub> Shutdown	V <sub>SD</sub>	V <sub>INDET</sub> Rising		350	550	720	mV	
V <sub>SD</sub> Hysteresis		V <sub>INDET</sub> Falling			200			
V <sub>INDET</sub> Input Threshold Protection								
V <sub>INDET</sub> - V <sub>IN</sub> Under Voltage	V <sub>UV</sub>	V <sub>INDET</sub> Rising		3.13	3.3	3.46	V	
V <sub>UV</sub> Hysteresis		V <sub>INDET</sub> Falling		0.23	0.3	0.35		
Over Temperature Voltages								
Activating Temperature	OTP_on	T <sub>J</sub> Increasing			135		°C	
De-Activating Temperature	OTP_off	T <sub>J</sub> Decreasing			113			



SPECIFICATIONS <sup>a</sup>						
Parameter	Symbol	Test Conditions Unless Otherwise Specified $f_{\text{NOM}} = 500 \text{ kHz}$ , $V_{\text{IN}} = 75 \text{ V}$ $V_{\text{INDET}} = 7.5 \text{ V}$ ; $10.5 \text{ V} \leq V_{\text{CC}} \leq 13.2 \text{ V}$	Limits - 40 to 85 °C			Unit
			Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
Converter Supply Current ( $V_{\text{CC}}$ )						
Shutdown	$I_{\text{CC1}}$	Shutdown, $V_{\text{INDET}} = 0 \text{ V}$	50		350	$\mu\text{A}$
Converter Supply Current ( $V_{\text{CC}}$ )						
Switching Disabled	$I_{\text{CC2}}$	$V_{\text{INDET}} < V_{\text{REF}}$	4	8	12	mA
Switching w/o Load	$I_{\text{CC3}}$	$V_{\text{INDET}} > V_{\text{REF}}$ , $f_{\text{NOM}} = 500 \text{ kHz}$	5	10	15	
Switching with $C_{\text{LOAD}}$	$I_{\text{CC4}}$	$V_{\text{CC}} = 12 \text{ V}$ , $C_{\text{DH}} = C_{\text{DL}} = 3 \text{ nF}$ $C_{\text{SRH}} = C_{\text{SRL}} = 0.3 \text{ nF}$		21		
Output MOSFET DH Driver (High-Side)						
Output High Voltage	$V_{\text{OH}}$	Sourcing 10 mA	$V_{\text{BST}} - 0.3$			V
Output Low Voltage	$V_{\text{OL}}$	Sinking 10 mA			$V_{\text{LX}} + 0.3$	
Boost Current	$I_{\text{BST}}$	$V_{\text{LX}} = 48 \text{ V}$ , $V_{\text{BST}} = V_{\text{LX}} + V_{\text{CC}}$	1.3	1.9	2.7	mA
LX Current	$I_{\text{LX}}$	$V_{\text{LX}} = 48 \text{ V}$ , $V_{\text{BST}} = V_{\text{LX}} + V_{\text{CC}}$	- 1.3	- 0.7	- 0.4	
Peak Output Source	$I_{\text{SOURCE}}$	$V_{\text{CC}} = 10.5 \text{ V}$		- 1.0	- 0.75	A
Peak Output Sink	$I_{\text{SINK}}$		0.75	1.0		
Rise Time	$t_{\text{r}}$	$C_{\text{DH}} = 3 \text{ nF}$		35		ns
Fall Time	$t_{\text{f}}$			35		
Output MOSFET DL Driver (Low-Side)						
Output High Voltage	$V_{\text{OH}}$	Sourcing 10 mA	$V_{\text{CC}} - 0.3$			V
Output Low Voltage	$V_{\text{OL}}$	Sinking 10 mA			0.3	
Peak Output Source	$I_{\text{SOURCE}}$	$V_{\text{CC}} = 10.5 \text{ V}$		- 1.0	- 0.75	A
Peak Output Sink	$I_{\text{SINK}}$		0.75	1.0		
Rise Time	$t_{\text{r}}$	$C_{\text{DH}} = 3 \text{ nF}$		35		ns
Fall Time	$t_{\text{f}}$			35		
Synchronous Rectifier ( $\text{SR}_{\text{H}}$ , $\text{SR}_{\text{L}}$ ) Drivers						
Output High Voltage	$V_{\text{OH}}$	Sourcing 10 mA	$V_{\text{CC}} - 0.4$			V
Output Low Voltage	$V_{\text{OL}}$	Sinking 10 mA			0.4	
Break-Before-Make Time <sup>e</sup>	$t_{\text{BBM1}}$	$T_{\text{A}} = 25 \text{ }^{\circ}\text{C}$ , $R_{\text{BBM}} = 33 \text{ k}\Omega$ , $V_{\text{INDET}} = 4.8 \text{ V}$ , $V_{\text{EP}} = 0 \text{ V}$ , $V_{\text{IN}} = 48 \text{ V}$		48		ns
	$t_{\text{BBM2}}$			9		
	$t_{\text{BBM3}}$	$T_{\text{A}} = 25 \text{ }^{\circ}\text{C}$ , $R_{\text{BBM}} = 33 \text{ k}\Omega$ , $\text{BST} = 60 \text{ V}$ , $V_{\text{INDET}} = 4.8 \text{ V}$ , $V_{\text{EP}} = 0 \text{ V}$ , $V_{\text{IN}} = 48 \text{ V} = \text{LX}$		24		
	$t_{\text{BBM4}}$			18		
Peak Output Source	$I_{\text{SOURCE}}$	$V_{\text{CC}} = 10.5 \text{ V}$		- 100		mA
Peak Output Sink	$I_{\text{SINK}}$			100		
Rise Time	$t_{\text{r}}$	$C_{\text{DH}} = 3 \text{ nF}$		35		ns
Fall Time	$t_{\text{f}}$			35		
Voltage Mode						
Error Amplifier	$t_{\text{d1DH}}$	Input to High-Side Switch Off		< 200		ns
	$t_{\text{d2DL}}$	Input to Low-Side Switch Off		< 200		
Current Mode						
Current Amplifier	$t_{\text{d3DH}}$	Input to High-Side Switch Off		< 200		ns
	$t_{\text{d4DL}}$	Input to Low-Side Switch Off		< 200		

Notes:

a. Refer to PROCESS OPTION FLOWCHART for additional information.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (- 40 °C to 85 °C).

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d.  $F_{\text{MIN}}$  when  $V_{\text{CL\_CONT}}$  at clamp level. Typical foldback frequency change + 20 %, - 30 % over temperature.

e. See Figure 3 for Break-Before-Make time definition.

f.  $V_{\text{UVLO}}$  tracks  $V_{\text{REG1}}$  by a diode drop.

g. Guaranteed by design and characterization, not tested in production.

## TIMING DIAGRAM FOR MOS DRIVERS

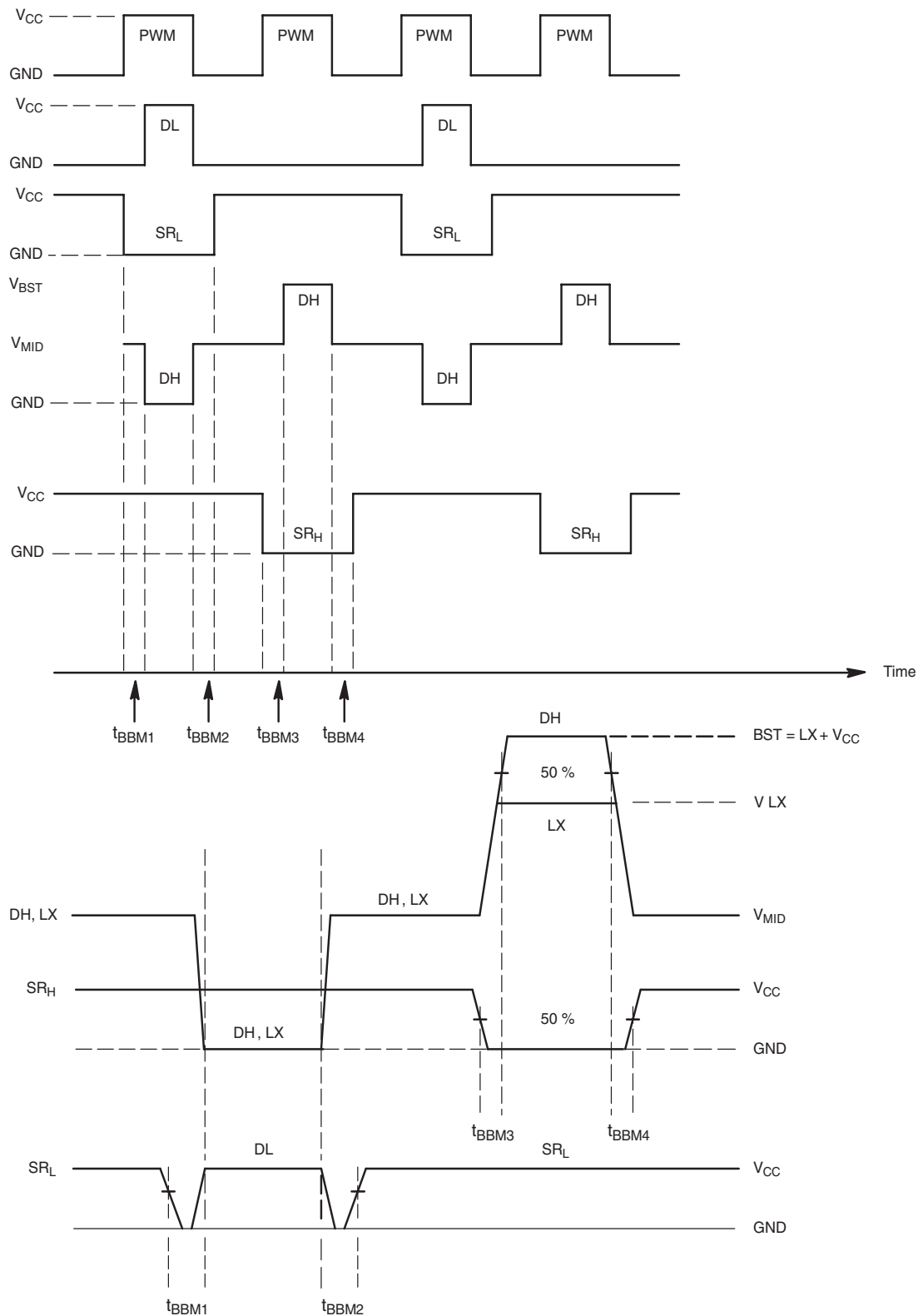
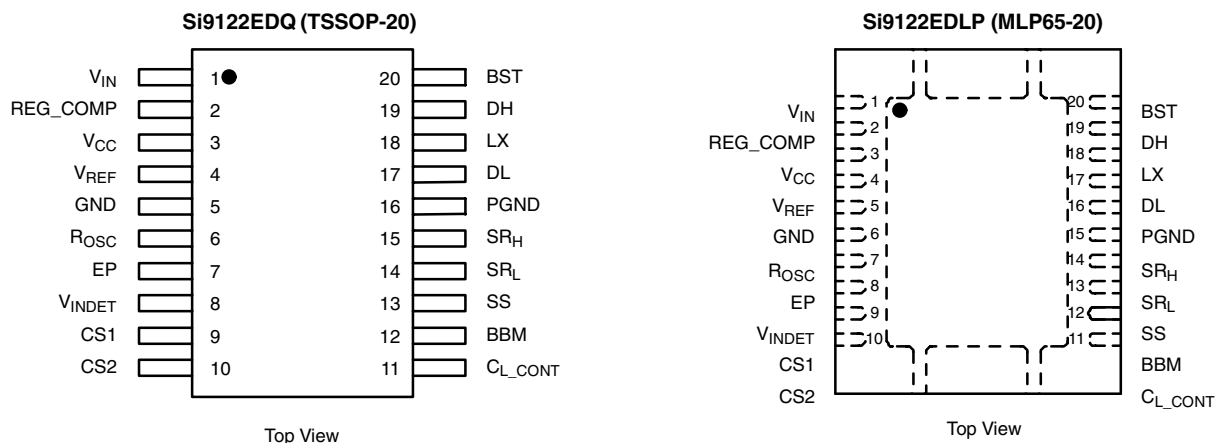


Figure 3.

## PIN CONFIGURATION



## ORDERING INFORMATION

Part Number	Temperature Range	Package
Si9122EDQ-T1-E3	- 40 °C to 85 °C	TSSOP-20
Si9122EDLP-T1-E3		MLP65-20

Eval Board	Temperature Range	Board Type
Contact Factory	- 10 °C to 70 °C	Surface Mount and Thru-Hole

## PIN DESCRIPTION

1	V <sub>IN</sub>	Input supply voltage for the start-up circuit
2	REG_COMP	Control signal for an external pass transistor
3	V <sub>CC</sub>	Supply voltage for internal circuitry
4	V <sub>REF</sub>	3.3 V reference
5	GND	Ground
6	R <sub>OSC</sub>	External resistor connection to oscillator
7	EP	Voltage control input
8	V <sub>INDET</sub>	V <sub>IN</sub> under voltage detect and shutdown function input. Shuts down or disables switching when V <sub>INDET</sub> falls below preset threshold voltages and provides the feed forward voltage.
9	CS1	Current limit amplifier negative input
10	CS2	Current limit amplifier positive input
11	C <sub>L_CONT</sub>	Current limit compensation
12	BBM	Programmable Break-Before-Make time connection to an external resistor to set time delay
13	SS	Soft-Start control - external capacitor connection
14	SR <sub>L</sub>	Signal transformer drive, sequenced with the primary side.
15	SR <sub>H</sub>	Signal transformer drive, sequenced with the primary side
16	PGND	Power ground
17	DL	Low-side gate drive signal - primary
18	LX	High-side source and transformer connection node
19	DH	High-side gate drive signal - primary
20	BST	Bootstrap voltage to drive the high-side n-channel MOSFET switch

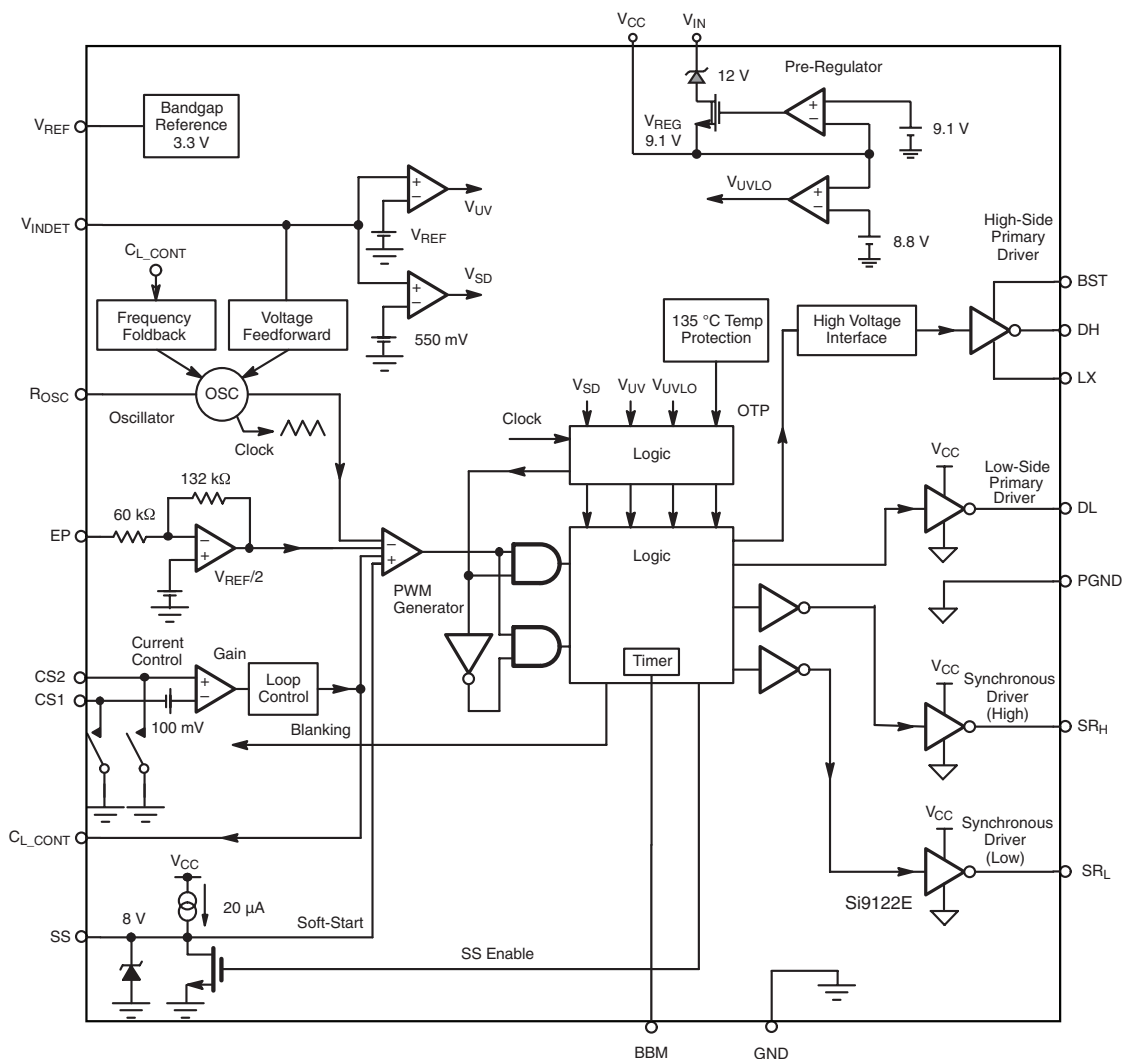


Figure 4. Detailed Si9122E Block Diagram

## DETAILED OPTION

### Start-Up

When  $V_{INEXT}$  rises above 0 V, the internal pre-regulator begins to charge up the  $V_{CC}$  capacitor. Current into the external  $V_{CC}$  capacitor is limited to typically 40 mA by the internal DMOS device. When  $V_{CC}$  exceeds the UVLO voltage of 8.8 V a soft-start cycle of the switch mode supply is initiated. The  $V_{CC}$  supply continues to be charged by the pre-regulator until  $V_{CC}$  equals  $V_{REG}$ . During this period, between  $V_{UVLO}$  and  $V_{REG}$ , excessive load current will result in  $V_{CC}$  falling below  $V_{UVLO}$  and stopping switch mode operation. This situation is avoided by the hysteresis between  $V_{REG}$  and  $V_{UVLO}$  and correct sizing of the  $V_{CC}$  capacitor, bootstrap capacitor and the soft-start capacitor. The value of the  $V_{CC}$  capacitor should therefore be chosen to be capable of maintaining switch mode operation until the required  $V_{CC}$  current can be supplied from the external circuit (e.g via a power transformer winding and zener regulator). Feedback from the output of the switch mode supply charges  $V_{CC}$  above  $V_{REG}$  and fully disconnects the pre-regulator,

isolating  $V_{CC}$  from  $V_{IN}$ .  $V_{CC}$  is then maintained above  $V_{REG}$  for the duration of switch mode operation. In the event of an over voltage condition on  $V_{CC}$ , an internal voltage clamp turns on at 14.5 V to shunt excessive current to GND. Care needs to be taken if there is a delay prior to the external circuit feeding back to the  $V_{CC}$  supply. To prevent excessive power dissipation within the IC it is advisable to use an external PNP device. A pin has been incorporated on the IC, (REG\_COMP) to provide compensation when employing the external device. In this case the  $V_{IN}$  pin is connected to the base of the PNP device and controls the current, while the REG\_COMP pin determines the frequency compensation of the circuit. The value of the REG\_COMP capacitor cannot be too big, otherwise it will slow down the response of the pre-regulator in the case that fault situations occur and pre-regulator needs to be turned on again. To understand the operation, please refer to figure 5.



The soft-start circuit is designed for the dc-dc converter to start-up in an orderly manner and reduce component stresses on the Converter. This feature is programmable by selecting an external  $C_{SS}$ . An internal 20  $\mu$ A current source charges  $C_{SS}$  from 0 V to the final clamped voltage of 8 V. In the event of UVLO or shutdown,  $V_{SS}$  will be held low ( $< 1$  V) disabling driver switching. To prevent oscillations, a longer soft-start time may be needed for highly capacitive loads and/or high peak output current applications.

## Reference

The reference voltage of Si9122E is set at 3.3 V. The reference voltage should be de-coupled externally with 0.1  $\mu$ F capacitor. The  $V_{REF}$  voltage is 0 V in shutdown mode and has 50 mA source capability.

## Voltage Mode PWM Operation

Under normal load conditions, the IC operates in voltage mode and generates a fixed frequency pulse width modulated signal to the drivers. Duty cycle is controlled over a wide range to maintain output voltage under line and load variation. Voltage feedforward is also included to take account of variations in supply voltage  $V_{IN}$ .

In the half-bridge topology requiring isolation between output and input, the reference voltage and error amplifier must be supplied externally, usually on the secondary side. The error information is thus passed to the power controller through an opto-coupling device. This information is inverted, hence 0 V represents the maximum duty cycle, while 2 V represents minimum duty cycle. The error information enters the IC via pin EP, and is passed to the PWM generator via an inverting amplifier. The relationship between Duty cycle and  $V_{EP}$  is shown in the Typical Characteristic Graph, Duty Cycle vs.  $V_{EP}$  25  $^{\circ}$ C, page 12. Voltage feedforward is implemented by taking the attenuated  $V_{IN}$  signal at  $V_{INDET}$  and directly modulating the duty cycle.

At start-up, i.e., once  $V_{CC}$  is greater than  $V_{UVLO}$ , switching is initiated under soft-start control which increases primary switch on-times linearly from  $D_{MIN}$  to  $D_{MAX}$  over the soft-start period. Start-up from a  $V_{INDET}$  power down is also initiated under soft-start control.

## Half Bridge and Synchronous Rectification Timing Sequence

The PWM signal generated within the Si9122E controls the low and high-side bridge drivers on alternative cycles. A period of inactivity always results after initiation of the soft-start cycle until the soft-start voltage reaches approximately 1.2 V and PWM controlled switching begins. The first bridge driver to switch is always the low-side (DL), as this allows charging of the high-side boost capacitor.

The timing and coordination of the drives to the primary and secondary stages is very important and shown in figure 3. It is essential to avoid the situation where both of the secondary MOSFETs are on when either the high or the low-side switch are active. In this situation the transformer would effectively be presented with a short across the output. To

avoid this, a dedicated break-before-make circuit is included which will generate non-overlapping waveforms for the primary and the secondary drive signals. This is achieved by a programmable timer which delays the on switching of the primary driver relative to the off switching of the related secondary and subsequently delays the on switching of the secondary relative to the off switching of the related primary. Typical variations of BBM times with respect to  $R_{BBM}$  and other operating parameters are shown on page 14 and 15.

## Primary High- and Low-Side MOSFET Drivers

The drive voltage for the low-side MOSFET switch is provided directly from  $V_{CC}$ . The high-side MOSFET however requires the gate voltage to be enhanced above  $V_{IN}$ . This is achieved by bootstrapping the  $V_{CC}$  voltage onto the LX voltage (the high-side MOSFET source). In order to provide the bootstrapping an external diode and capacitor are required as shown on the application schematic. The capacitor will charge up after the low-side driver has turned on. The switch gatedrive signals DH and DL are shown in figure 3.

## Secondary MOSFET Drivers

The secondary side MOSFETs are driven from the Si9122E via a center tapped pulse transformer and inverter drivers. The waveforms from  $SR_H$  and  $SR_L$  are shown in figure 3. Of importance is the relative voltage between  $SR_H$  and  $SR_L$ , i.e. that which is presented across the primary of the pulse transformer. When both potentials of  $SR_L$  and  $SR_H$  are equal then by the action of the inverting drivers both secondary MOSFETs are turned on.

## Oscillator

The oscillator is designed to operate at a nominal frequency of 500 kHz. The 500 kHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. The oscillator and therefore the switching frequency is programmable by attaching a resistor to the  $R_{OSC}$  pin. Under overload conditions the oscillator frequency is reduced by the current overload protection to enable a constant current to be maintained into a low impedance circuit.

## Current Limit

Current mode control providing constant current operation is achieved by monitoring the differential voltage  $V_{CS}$  between the CS1 and CS2 pins, which are connected to a current sense resistor on the primary low-side MOSFET. In the absence of an overcurrent condition,  $V_{CS}$  is less than lower current limit threshold  $V_{TLCL}$  (typical 100 mV);  $C_{L\_CONT}$  is pulled up linearly via the 120  $\mu$ A current source ( $I_{PU}$ ) and both DL and DH switch at half the oscillator set frequency. When a moderate overcurrent condition occurs ( $V_{TLCL} < V_{CS} < V_{THCL}$ ), the  $C_{L\_CONT}$  capacitor will be discharged at a rate that is proportional to  $V_{CS} - 100$  mV by the  $I_{PD}$  current source. Both driver outputs are in frequency fold-back mode and the switching frequency becomes roughly 20 % of

normal switching frequency. When a severe overcurrent condition occurs ( $V_{THCL} < V_{CS}$ ), the NMOS discharges  $C_{L\_CONT}$  capacitor immediately at 2 mA rate and the  $C_{L\_CONT}$  voltage will be clamped to 1.2 V disabling both DL and DH outputs.

Before  $V_{CS}$  reaches severe overcurrent condition, a lowering of the  $C_{L\_CONT}$  voltage results in PWM control of the output drive being taken over by the current limit control loop through  $C_{L\_CONT}$ . Current control initially reduces the switching duty cycle toward the minimum the chip can reach ( $D_{MIN}$ ). If this duty cycle reduction still cannot lower the load current, then the switching frequency will start to fold back to minimum 1/5 of the nominal frequency. This prevents the on-time of the primary drivers from being reduced to below 100 ns and avoids current tails. If  $V_{CS} > V_{THCL}$ , the switching will then stop.

With constant current mode control and frequency foldback, protection of the MOSFET switches is increased. The converter reverts to voltage mode operation immediately when the primary current falls below the limit level, and  $C_{L\_CONT}$  capacitor is charged up and clamped to 6.5 V. The soft-start function does not apply during current limit period, as this would constitute hiccup mode operation.

### $V_{IN}$ Voltage Monitor - $V_{INDET}$

The chip provides a means of sensing the voltage of  $V_{IN}$ , and withholding operation of the output drivers until a minimum voltage of  $V_{REF}$  (3.3 V, 300 mV hysteresis), is achieved. This is achieved by choosing an appropriate resistive tap between the ground and  $V_{IN}$ , and comparing this voltage with the reference voltage. When the applied voltage is greater than  $V_{REF}$ , the output drivers are activated as normal.  $V_{INDET}$  also provides the input to the voltage feedforward function.

However, if the divided voltage applied to the  $V_{INDET}$  pin is greater than  $V_{CC} - 0.3$  V, the high-side driver, DH, will stop switching until the voltage drops below  $V_{CC} - 0.3$  V. Thus, the resistive tap on the  $V_{IN}$  divider must be set to accommodate the normal  $V_{CC}$  operating voltage to avoid this condition. Alternatively, a zener clamp diode from  $V_{INDET}$  to GND may also be used.

### Shutdown Mode

If  $V_{INDET}$  is forced below the lower  $V_{SD}$  threshold, the device will enter SHUTDOWN mode. This powers down all unnecessary functions of the controller, ensures that the primary switches are off, and results in a low level current demand from the  $V_{IN}$  or  $V_{CC}$  supplies.

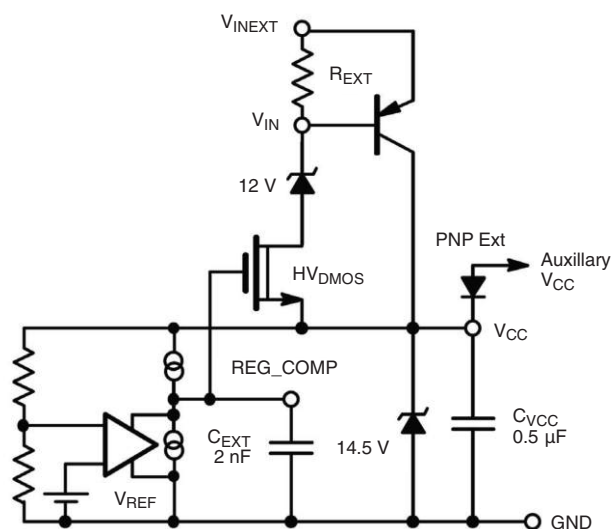


Figure 5. High-Voltage Pre-Regulator Circuit

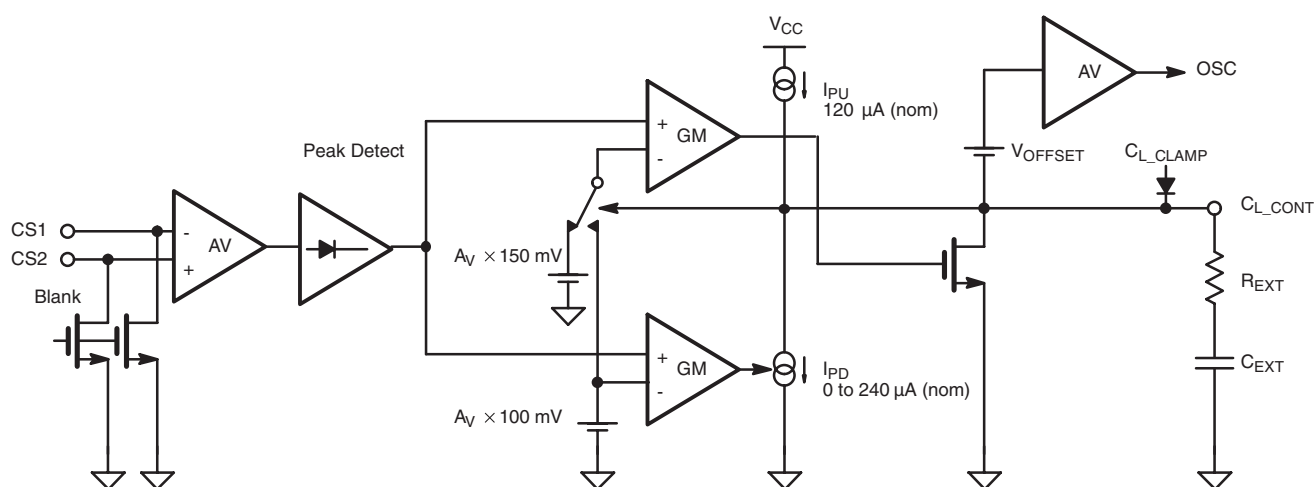


Figure 6. Current Limit Circuit

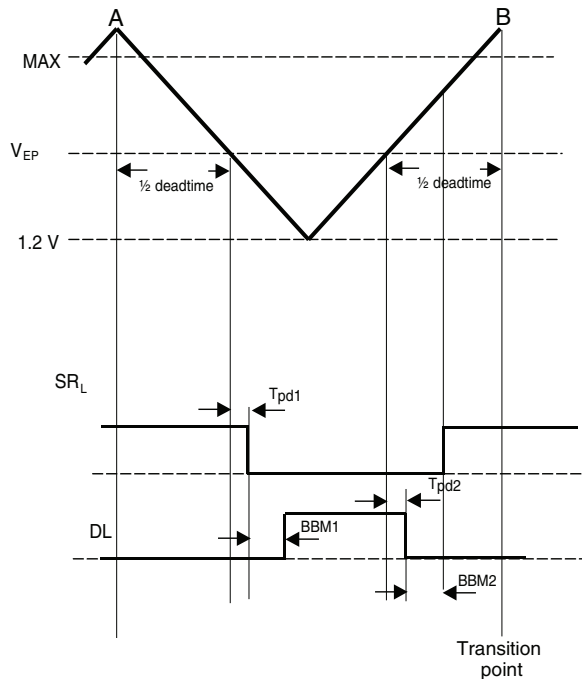
## REDUCTION OF $t_{BBM2,4}$ AT HIGHER $f_{osc}$

The start of a switching period is defined as the turning point of the oscillator, marked in Figure 7 as A, with the end of a switching period marked as B. For a half bridge, two switching periods are required for both the primary high-side and low-side drivers to operate as shown in Figure 3. For a given oscillator frequency there is a finite time in which all events from equation (1) have to occur. These are  $t_{dt}$  dead-time duration which is a function of  $V_{EP}$ ,  $t_{pd1}$  is the propagation delay from the PWM to  $SR_L$  (or  $SR_H$ ) output going low,  $t_{BBM1}$  (or  $t_{BBM3}$ ) rise delay, DL (or DH) primary driver on-time,  $t_{pd2}$  is the propagation delay from PWM to DL (or DH) output going low and  $t_{BBM2}$  (or  $t_{BBM4}$ ) fall delay.

Figure 7 shows the switching cycle for the low side primary driver and associated synchronous driver and equation (1) shows the switching time components.

At 500 kHz and maximum duty  $t_{pd2}$  is typically 60 ns.

$$T_{switch} = 1/2 t_{dt} + t_{pd1} + t_{SRLOFF} + 1/2 t_{dt} - t_{pd2} - t_{BBM2} \quad (1)$$



**Figure 7. Components of a Low-Side Switching Period**

The Si9122E has an improved primary and secondary duty cycles with typical maximum secondary duty at 93.2 %. Hence the dead-time is 6.8 % or 136 ns at 500 kHz. Half of the dead-time is 68 ns and during this time  $t_{pd2}$  plus  $t_{BBM2}$  has to occur before the next transition point of the oscillator cycle.  $R_{BBM}$  contributes 1.2 ns/k $\Omega$  to  $t_{BBM2}$ ; with 33 k $\Omega$  this amounts to 40 ns. If  $t_{BBM2}$  is set beyond the transition point,  $SR_L$  will be forced high due to logic conditions and a reduction in the set  $t_{BBM2}$  will be determined by the half dead-time minus  $t_{pd2}$  and will be independent of the  $R_{BBM}$  value as shown in figure 8.

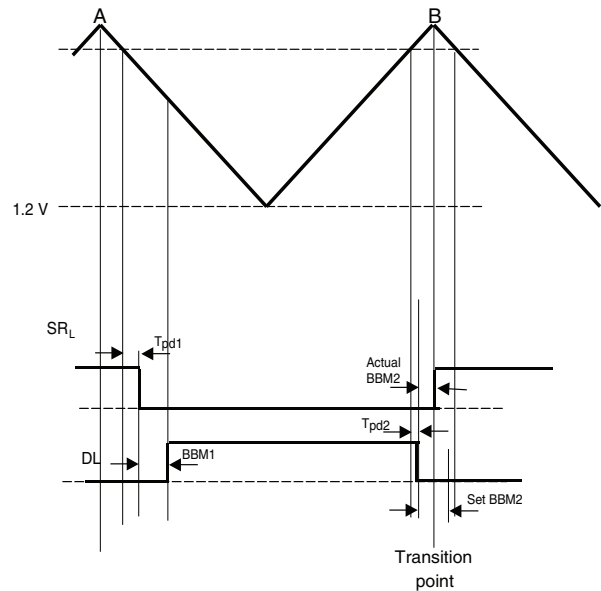
Note: this applies to  $t_{BBM4}$  as well.

To mitigate the decrease in set  $t_{BBM2}$  and  $t_{BBM4}$ , the following criteria must be met. The set  $t_{BBM2}$  plus its associated  $t_{pd2}$  must not exceed 3.4 % of the oscillator period. The typical  $t_{BBM2}$  and  $t_{BBM4}$  delays are provided in figure 9 to facilitate setting these delays for a given frequency with  $R_{BBM}$  of 33 k $\Omega$ .

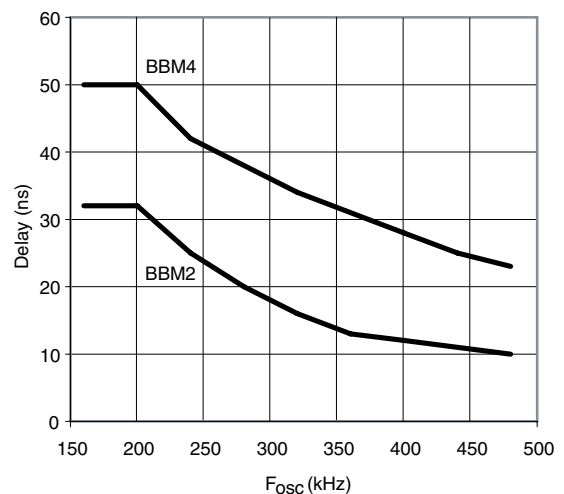
$$t_{BBM2} + t_{pd2} < 3.4 \% \text{ of oscillator period} \quad (2)$$

$$t_{BBM4} + t_{pd4} < 3.4 \% \text{ of oscillator period} \quad (3)$$

It is critical to avoid the condition where the sum of  $t_{BBM2}$  (set) and  $t_{pd2}$  is greater than 6.8 % of oscillator period whereby the correct sequence of logic signals cannot be guaranteed.

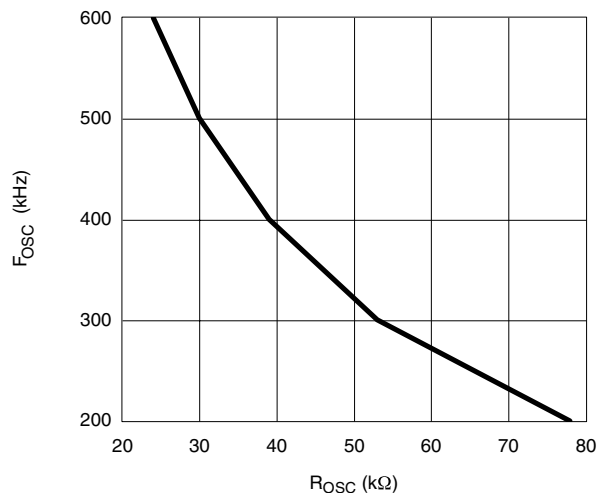
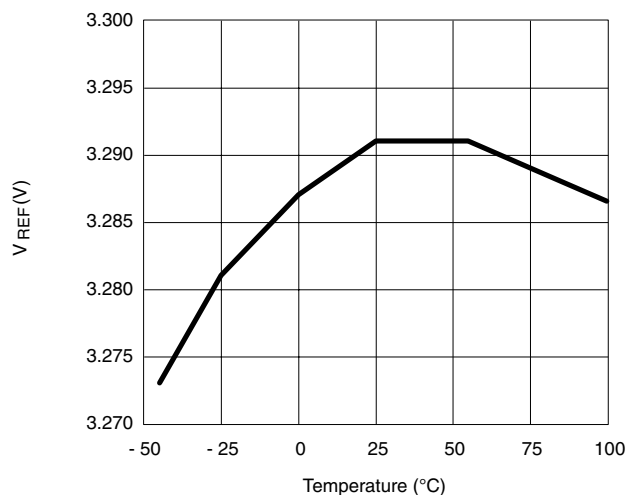
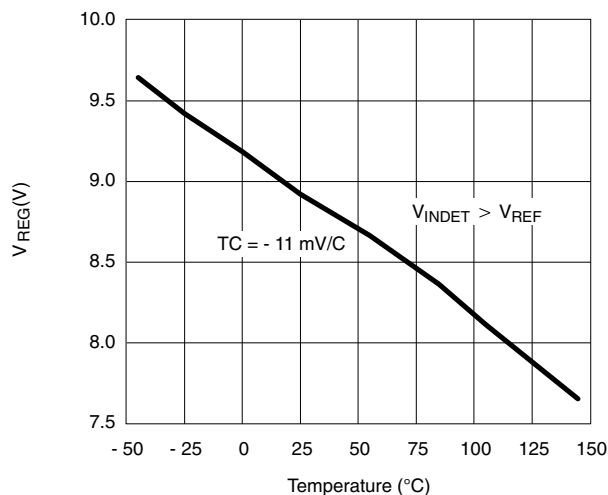
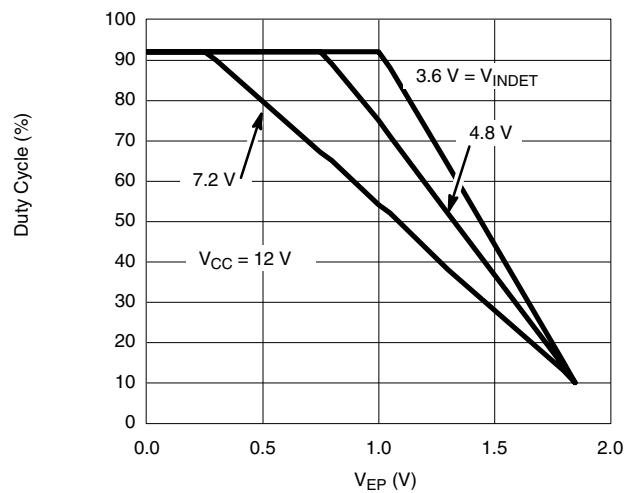
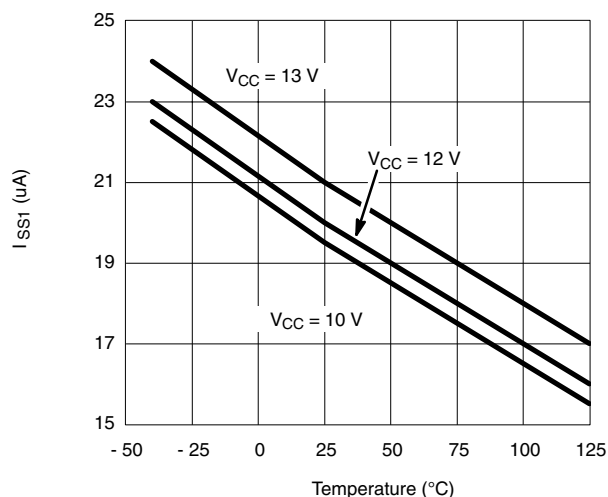
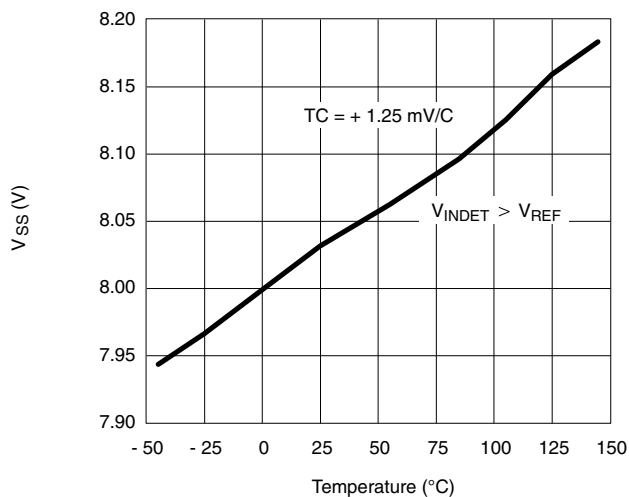


**Figure 8. Components of a Low-Side Switching Period with Maximum Duty and Limited BBM2**

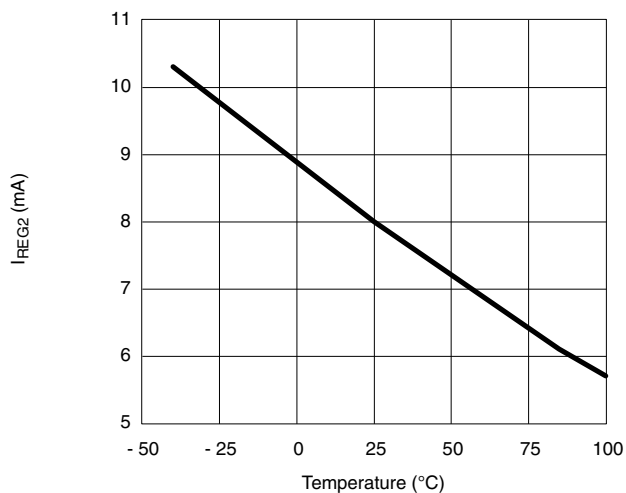


**Figure 9. Reduction in BBM2 and BBM4**  
Si9122E BBM vs.  $F_{osc}$ ;  $V_{IN} = 50$  V,  $V_{CC} = 10$  V,  
BST = 60 V, LX = 50 V,  $V_{EP} = 0$  V

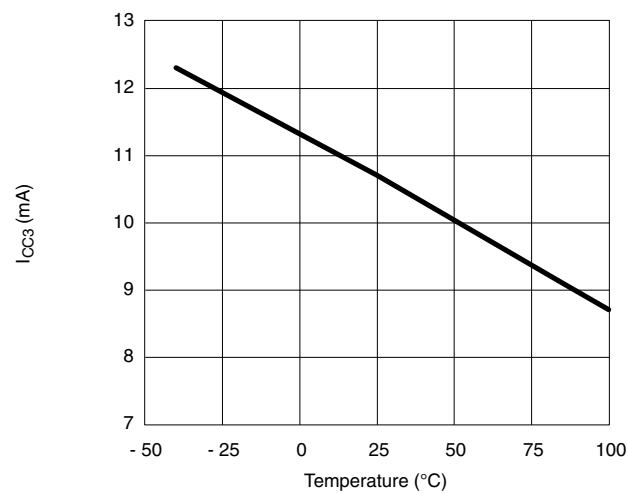
## TYPICAL CHARACTERISTICS

F<sub>OSC</sub> vs. R<sub>OSC</sub> at V<sub>CC</sub> = 12 VV<sub>REF</sub> vs. Temperature, V<sub>CC</sub> = 12 VV<sub>REG</sub> vs. Temperature, V<sub>IN</sub> = 48 VSR<sub>L</sub>, SR<sub>H</sub> Duty Cycle vs. V<sub>EP</sub>I<sub>SS</sub> vs. TemperatureV<sub>SS</sub> vs. Temperature, V = 12 V

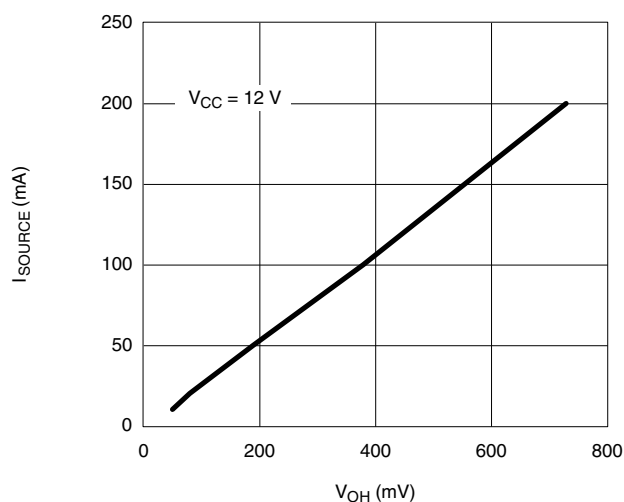
## TYPICAL CHARACTERISTICS



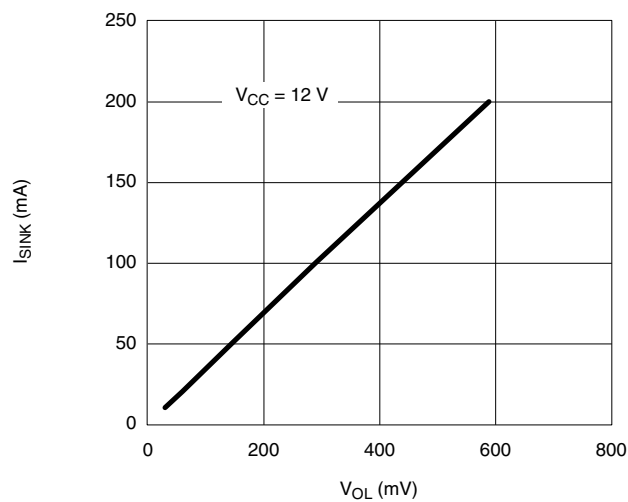
$I_{REG2}$  vs. Temperature,  $V_{CC} = 12 V$



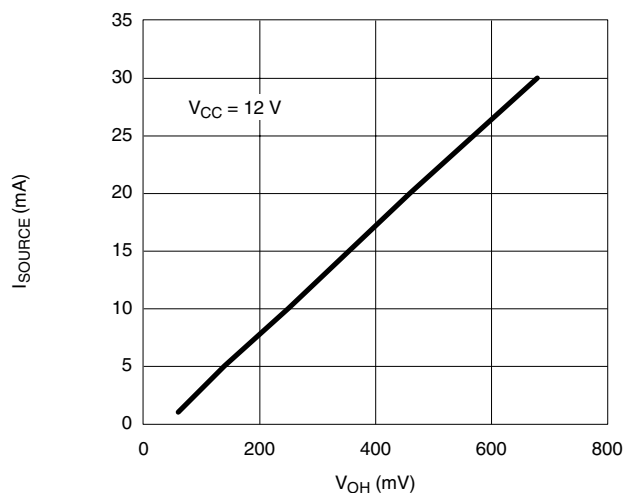
$I_{CC3}$  vs. Temperature  $V_{CC} = 12 V$



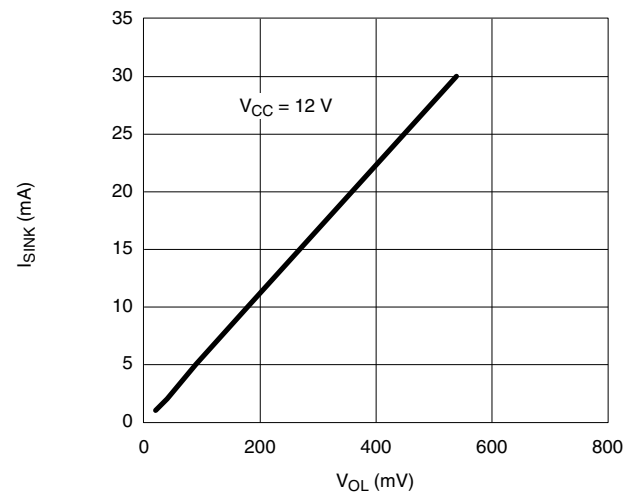
DH, DL  $I_{SOURCE}$  vs.  $V_{OH}$



DH, DL  $I_{SINK}$  vs.  $V_{OL}$

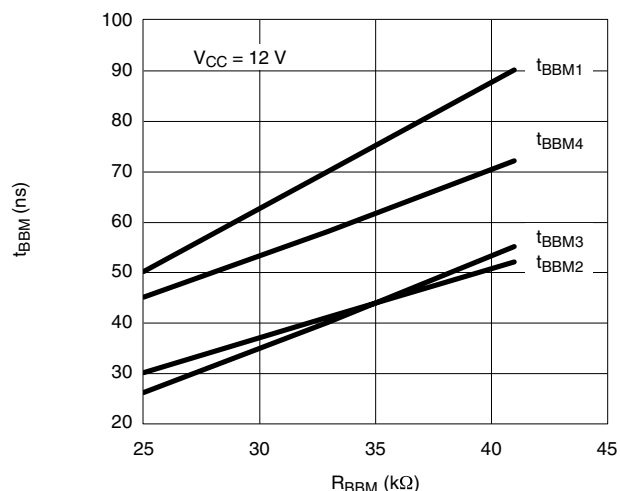


SR<sub>L</sub>, SR<sub>H</sub>  $I_{SOURCE}$  vs.  $V_{OH}$

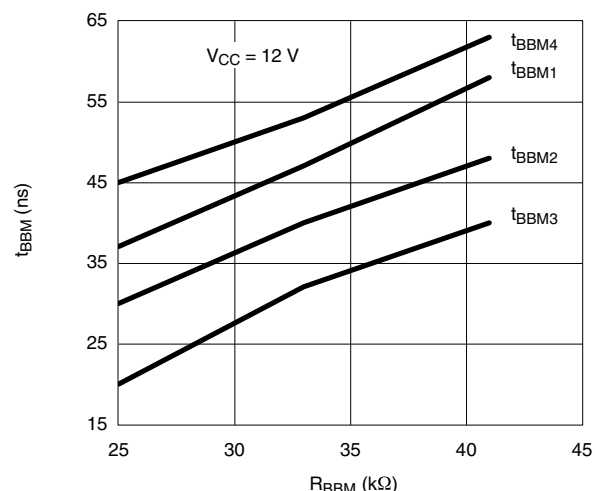


SR<sub>L</sub>, SR<sub>H</sub>  $I_{SINK}$  vs.  $V_{OL}$

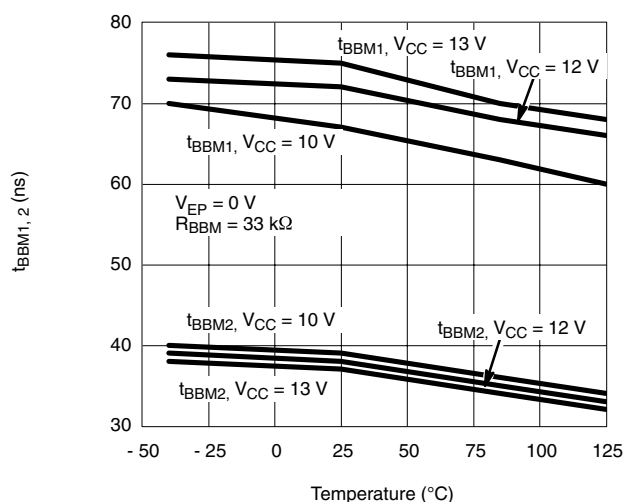
## TYPICAL CHARACTERISTICS



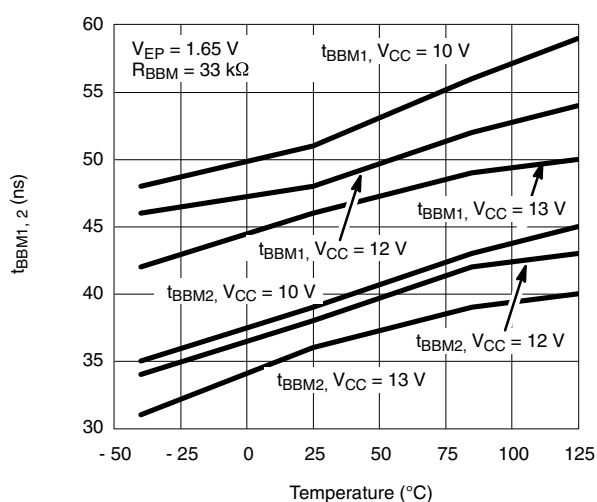
$t_{BBM}$  vs.  $R_{BBM}$ ,  $V_{EP} = 0\text{ V}$ ,  $V_{LX} = 48\text{ V}$ ,  $BST = 60\text{ V}$ ,  $V_{INDET} = 4.8\text{ V}$ ,  $f_{OSC} < 200\text{ kHz}$



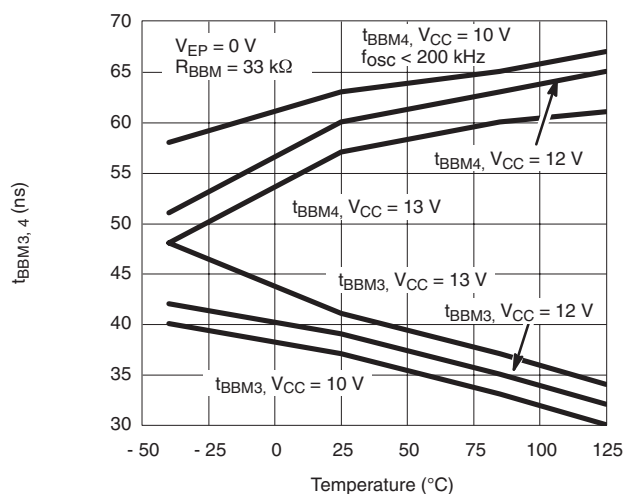
$t_{BBM}$  vs.  $R_{BBM}$ ,  $V_{EP} = 1.65\text{ V}$ ,  $V_{LX} = 48\text{ V}$ ,  $BST = 60\text{ V}$ ,  $V_{INDET} = 4.8\text{ V}$



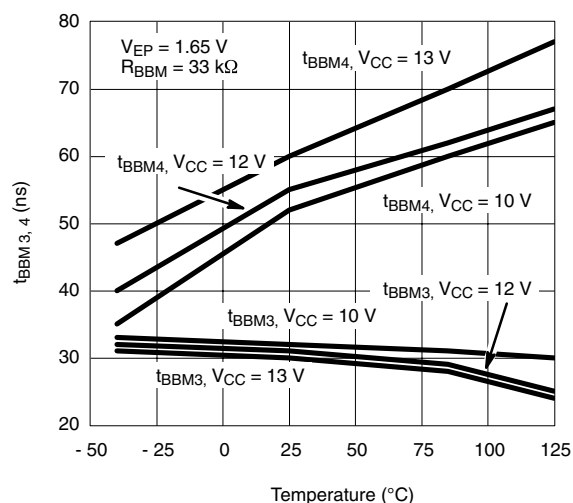
$t_{BBM1,2}$  vs. Temperature,  $V_{EP} = 0\text{ V}$ ,  $f_{OSC} < 200\text{ kHz}$



$t_{BBM1,2}$  vs. Temperature,  $V_{EP} = 1.65\text{ V}$

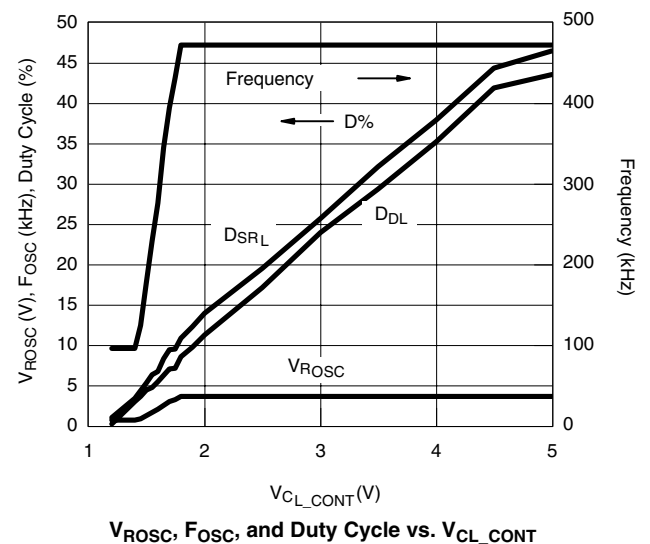
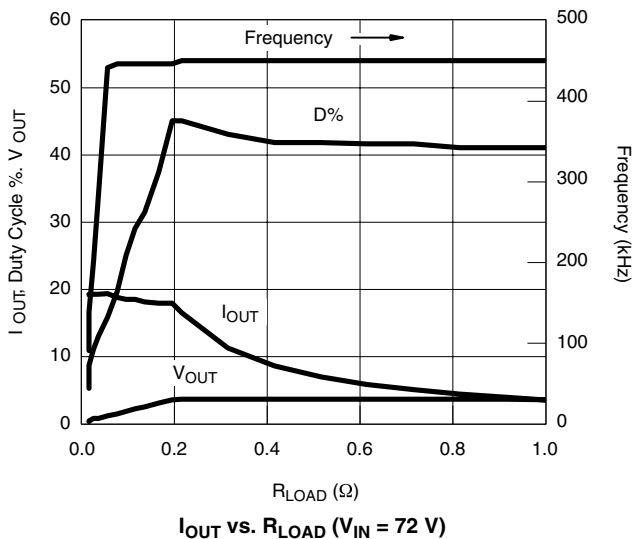
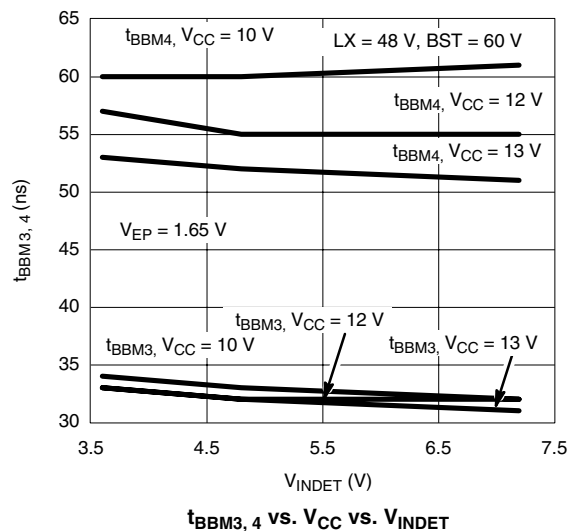
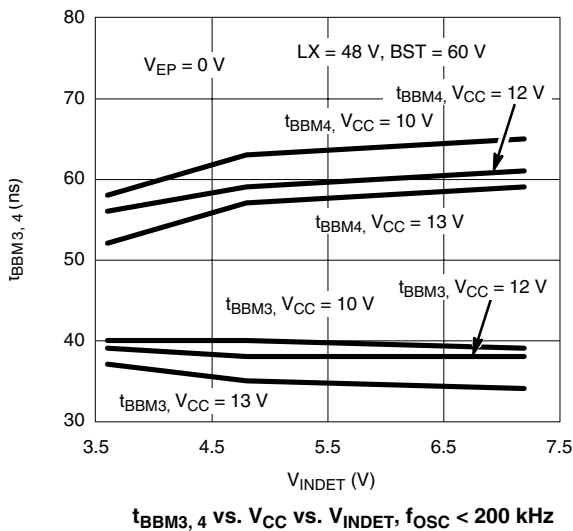
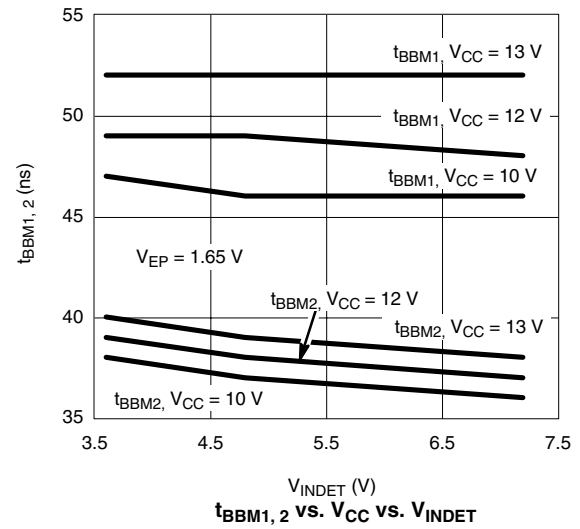
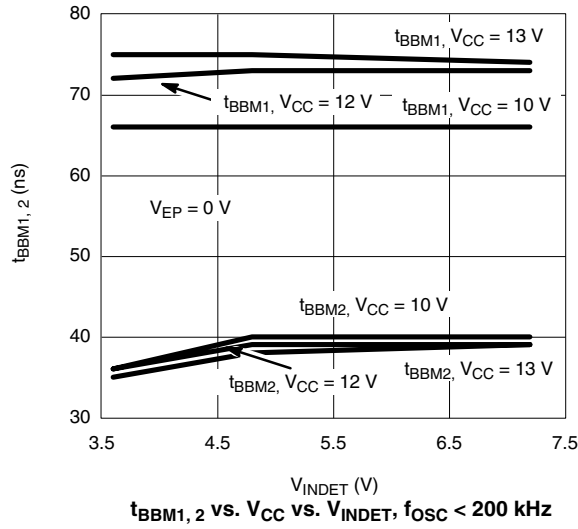


$t_{BBM3,4}$  vs. Temperature,  $V_{EP} = 0\text{ V}$ ,  $f_{OSC} < 200\text{ kHz}$



$t_{BBM3,4}$  vs. Temperature,  $V_{EP} = 1.65\text{ V}$

## TYPICAL CHARACTERISTICS



## TYPICAL WAVEFORMS

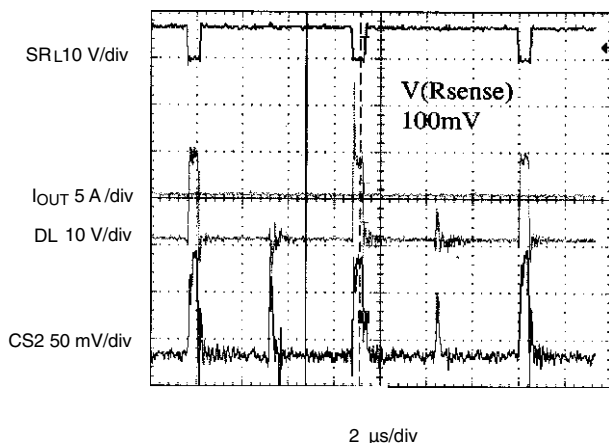
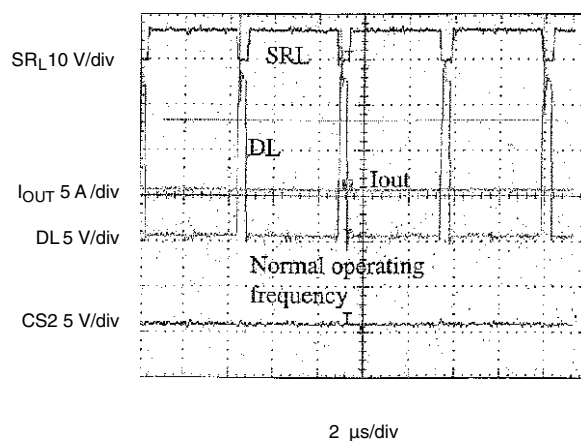
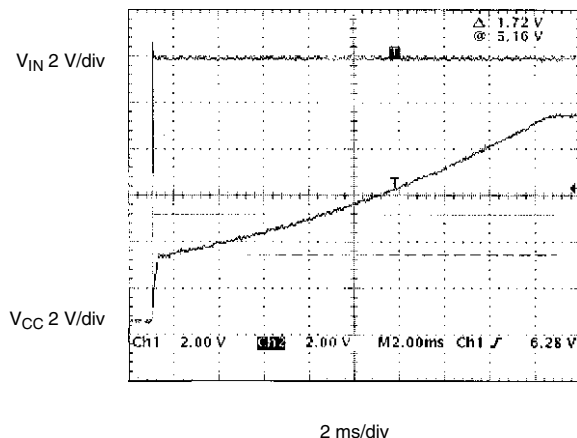
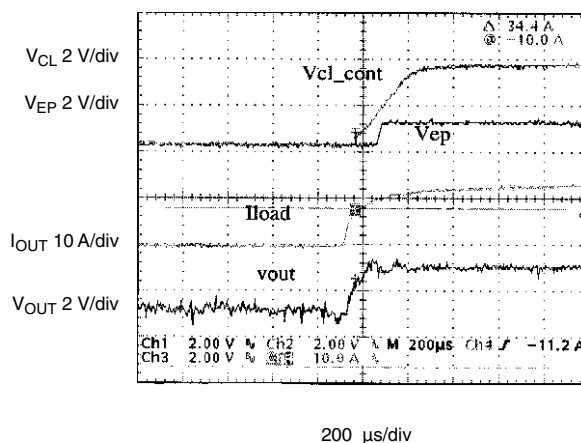
Figure 10. Foldback Mode,  $R_L = 0.02 \Omega$ Figure 11. Normal Mode,  $R_L = 0.1 \Omega$ Figure 12.  $V_{CC}$  Ramp-Up

Figure 13. Overload Recovery

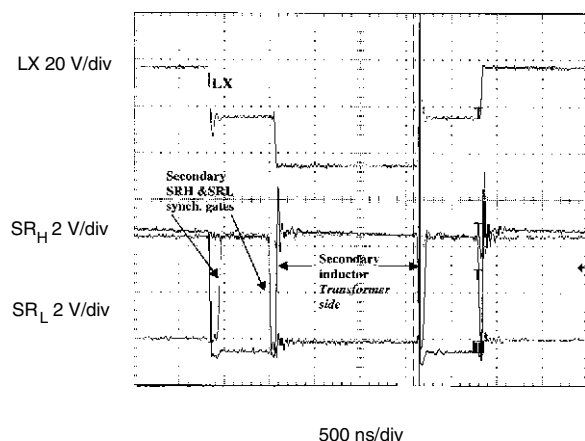


Figure 14. Effective BBM - Measured On Secondary

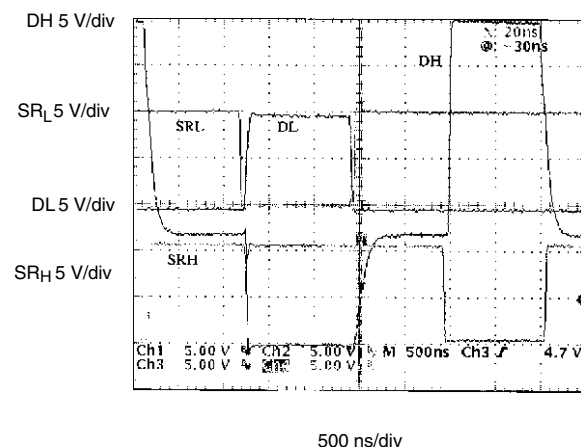


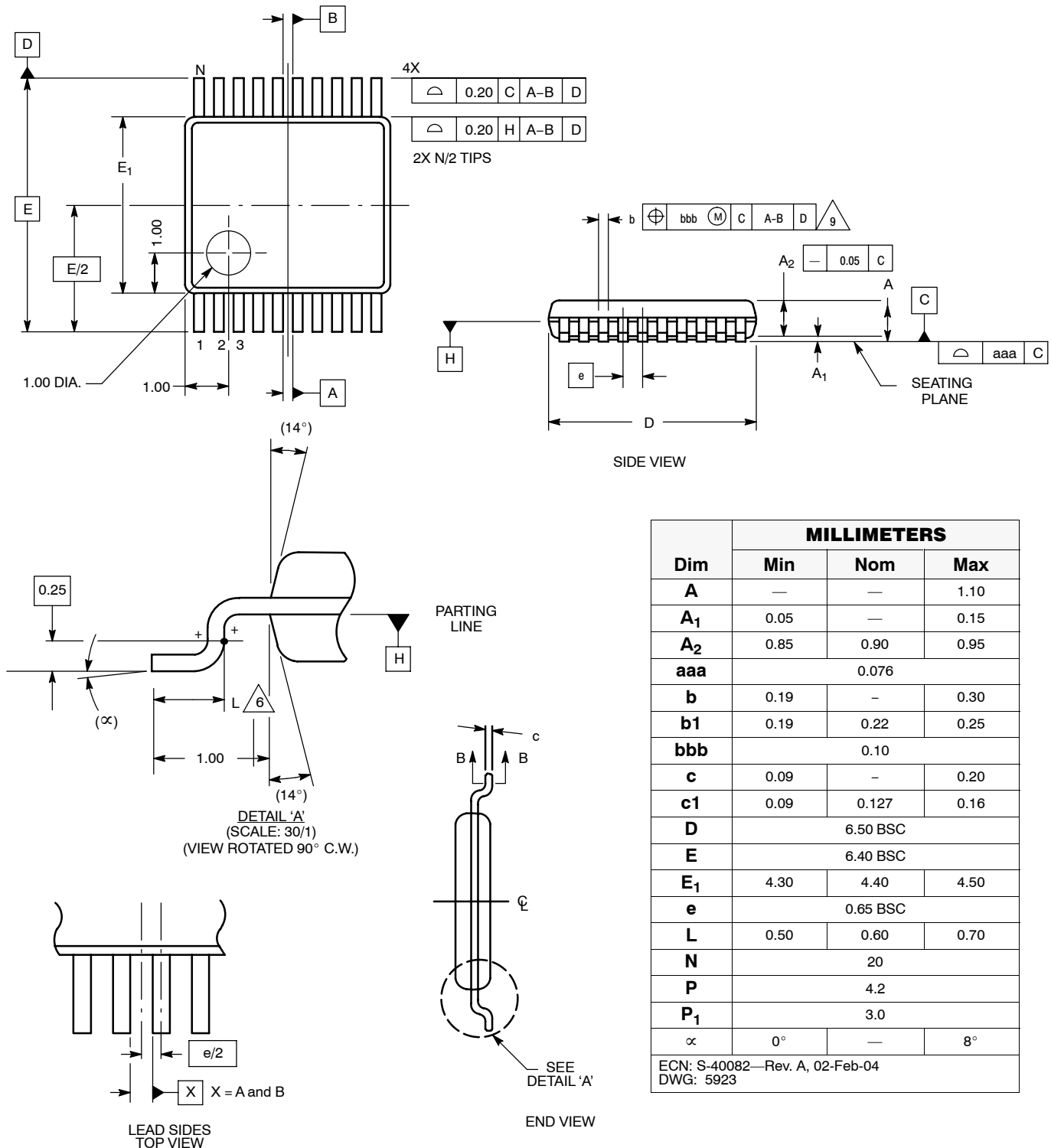
Figure 15. Drive Waveforms

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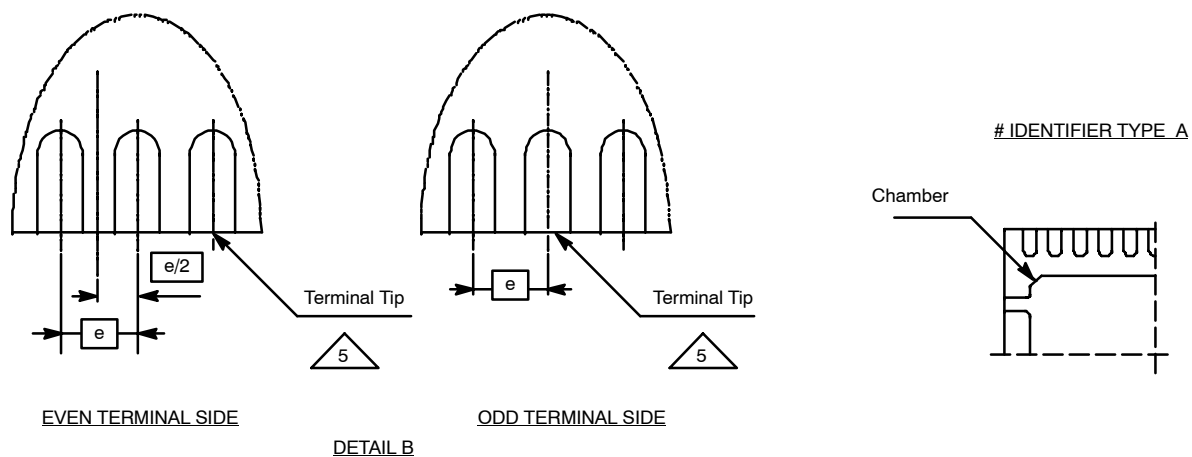
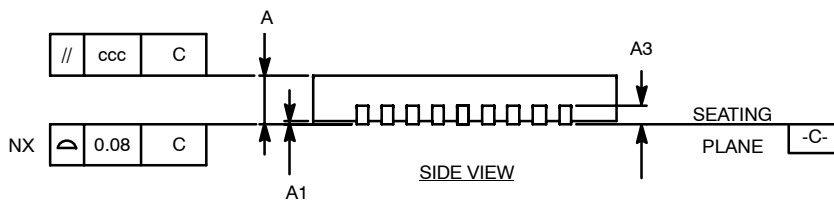
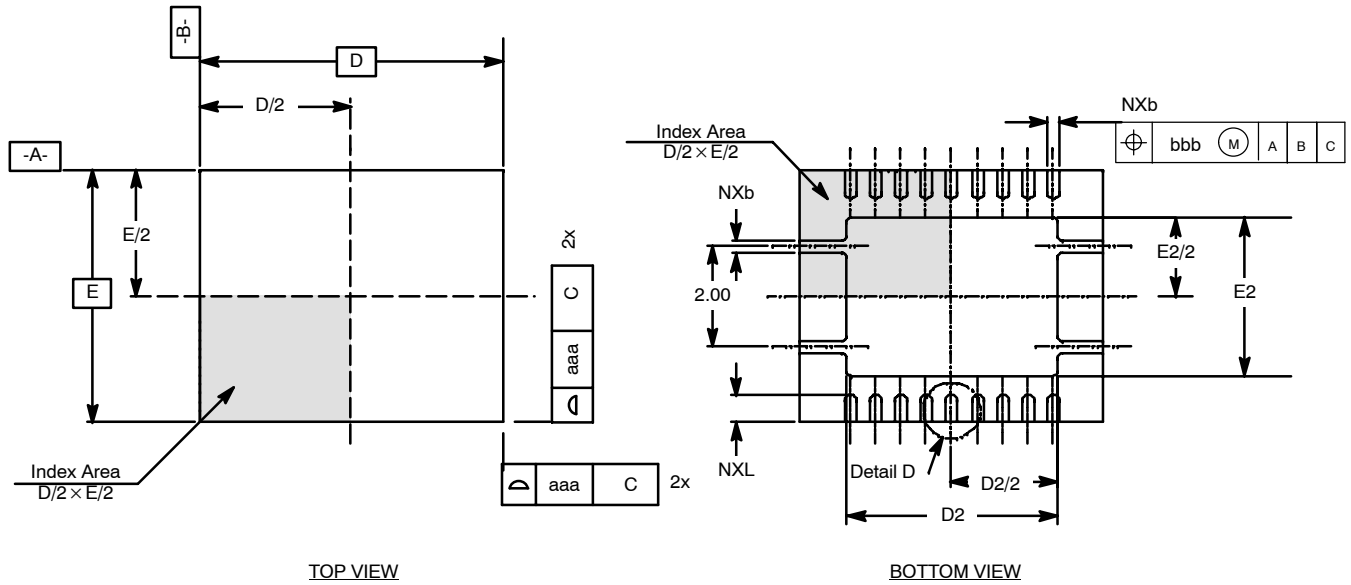


**TSSOP: 20-LEAD (POWER IC ONLY)**





PowerPAK® MLP65-18/20 (POWER IC ONLY)



### PowerPAK MLP65-18/20 (POWER IC ONLY)


**N = 18/20 PITCH: 0.5 mm, BODY SIZE: 6.00 x 5.00**

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.031	0.035	0.039	1, 2
A1	0.00	0.02	0.05	0.000	0.001	0.002	1, 2
A2	0.00	0.65	1.00	0.000	0.003	0.004	1, 2
A3	0.20 REF			0.008 REF			
aaa	–	0.15	–	–	0.006	–	
b	0.18	0.25	0.30	0.007	0.010	0.012	8
bbb	–	0.10	–	–	0.004	–	
C'	–	0.225	–	–	0.009	–	4, 10
ccc	–	0.10	–	–	0.004	–	
D	6.00 BSC			0.236 BSC			1, 2
D2	4.00	4.15	4.25	0.157	1.63	0.167	1, 2
E	5.00 BSC			0.197 BSC			1, 2
E2	3.00	3.15	3.25	0.118	0.124	0.128	1, 2
e	–	0.50	–	–	0.020	–	
L	0.45	0.55	0.65	0.018	0.022	0.026	1, 2
N	18, 20			18, 20			1, 2
ND(18)	9			9			1, 2
NE(18)	0			0			1, 2
ND(20)	10			10			1, 2
NE(20)	0			0			1, 2

\* Use millimeters as the primary measurement.

ECN: S-41946—Rev. A, 18-Oct-04  
DWG: 5939

#### NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angles are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JEDEC publication 95 SSP-022. Details of terminal #1 identifier are optional, but must be located within the zone indicated. A dot can be marked on the top side by pin 1 to indicate orientation.
5.  ND and NE refer to the number of terminals on the D and E side respectively.
6. Depopulation is possible in a symmetrical fashion.
7. NJR refers to NON JEDEC REGISTERED.
8. Dimension "b" applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.
9. Coplanarity applies to the exposed heat slug as well as the terminal.
10. The 45° chamfer dimension C' is located by pin 1 on the bottom side of the package.



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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**