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Vishay Siliconix

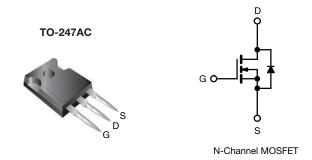
RoHS

COMPLIANT HALOGEN

FREE

EF Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY					
V _{DS} (V) at T _J max.	650				
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V	0.176			
Q _g (Max.) (nC)	84				
Q _{gs} (nC)	14				
Q _{gd} (nC)	24				
Configuration	Single				



FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Low figure-of-merit (FOM): Ron x Qg
- Low input capacitance (Ciss)
- Increased robustness due to low Q_{rr}
- Ultra low gate charge (Q_a)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Telecommunications
 - Server and telecom power supplies
- Lighting
 - High intensity discharge (HID)
 - Light emitting diodes (LEDs)
- Consumer and computing
 - ATX power supplies
- Industrial
 - Welding
 - Battery chargers
- Renewable energy
 - Solar (PV inverters)
- Switch mode power suppliers (SMPS)
- Applications using the following topologies
 - LLC
 - Phase shifted bridge (ZVS)
 - 3-level inverter
 - AC/DC bridge

ORDERING INFORMATION				
Package	TO-247AC			
Lead (Pb)-free and Halogen-free	SiHG21N60EF-GE3			

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage				V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	7 v	
Continuous Drain Current (T _J = 150 °C)		$V_{GS} \text{ at } 10 \text{ V} \qquad \frac{T_C = 2}{T_C = 1}$	T _C = 25 °C	,	21	А
			T _C = 100 °C	I _D	14	
Pulsed Drain Current ^a				I _{DM}	53	
Linear Derating Factor				1.8	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	367	mJ	
Maximum Power Dissipation				P_{D}	227	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C	
Drain-Source Voltage Slope		T _J = 125 °C		-11//-14	70	V/ns
Reverse Diode dV/dt d			dV/dt	50	V/IIS	
Soldering Recommendations (Peak Temperature) c for 10 s			300	°C		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. $V_{DD} = 50 \text{ V}$, starting $T_J = 25 \,^{\circ}\text{C}$, $L = 28.2 \,\text{mH}$, $R_g = 25 \,\Omega$, $I_{AS} = 5.1 \,\text{A}$.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, dI/dt = 900 A/ μ s, starting $T_J = 25$ °C.



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	62	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.55	C/VV	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		•		l	•	•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		600	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.59	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Cata Sauraa Laakaga			V _{GS} = ± 20 V	-	-	± 100	nA
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 30 V	-	-	± 1	μΑ
Zero Gate Voltage Drain Current		V _{DS} =	= 480 V, V _{GS} = 0 V	-	-	1	μА
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 480 \	/, V _{GS} = 0 V, T _J = 125 °C	-	-	500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 11 A	-	0.153	0.176	Ω
Forward Transconductance	9 _{fs}	V _{DS}	= 30 V, I _D = 11 A	-	7	-	S
Dynamic							
Input Capacitance	C _{iss}		$V_{GS} = 0 V$,	-	2030	-	
Output Capacitance	C _{oss}	1	$V_{DS} = 100 V,$	-	105	-	
Reverse Transfer Capacitance	C_{rss}		f = 1 MHz		5	-	
Effective output capacitance, energy related ^a	C _{o(er)}	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V to } 480 \text{ V}$		-	86	-	pF
Effective output capacitance, time related ^b	C _{o(tr)}			-	299	-	
Total Gate Charge	Qg	V _{GS} = 10 V I _D = 11 A, V _{DS} = 480 V		-	56	84	nC
Gate-Source Charge	Q _{gs}			-	14	-	
Gate-Drain Charge	Q _{gd}			-	24	-	
Turn-On Delay Time	t _{d(on)}			-	21	42	
Rise Time	t _r	V _{DD} = 480 V, I _D = 11 A		-	31	62	1
Turn-Off Delay Time	t _{d(off)}	$R_g = 9$	9.1 Ω , $V_{GS} = 10 \text{ V}$	-	59	89	ns
Fall Time	t _f		1		27	54	1
Gate Input Resistance	R_g	f = 1 MHz, open drain		0.2	0.56	1.2	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	Is	MOSFET symbol showing the integral reverse p - n junction diode		-	-	21	
Pulsed Diode Forward Current	I _{SM}			-	-	53	A
Diode Forward Voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 11 \text{A}, V_{GS} = 0 \text{V}$		-	0.9	1.2	V
Reverse Recovery Time	t _{rr}			-	135	270	ns
Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = I_S = 11 \text{A},$		-	0.76	1.52	μC
Reverse Recovery Current	I _{RRM}	dl/dt = 100 A/μs, V _R = 400 V		_	11	_	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

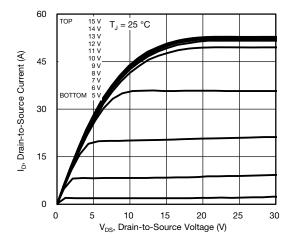


Fig. 1 - Typical Output Characteristics, T_J = 25 °C

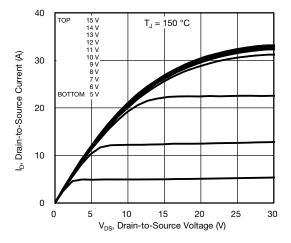


Fig. 2 - Typical Output Characteristics, T_J = 150 °C

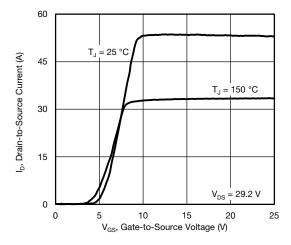


Fig. 3 - Typical Transfer Characteristics

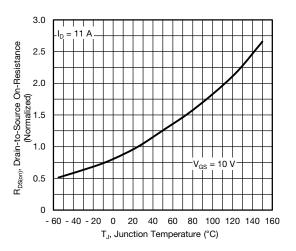


Fig. 4 - Normalized On-Resistance vs. Temperature

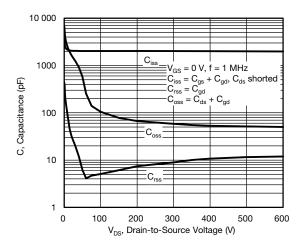


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

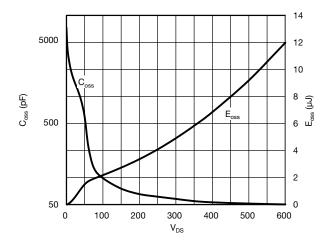


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



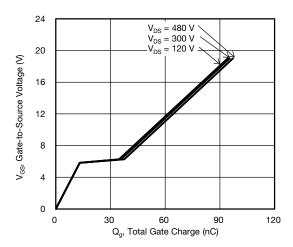


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

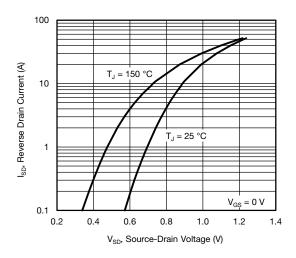


Fig. 8 - Typical Source-Drain Diode Forward Voltage

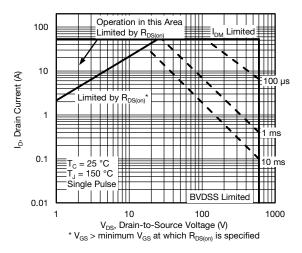


Fig. 9 - Maximum Safe Operating Area

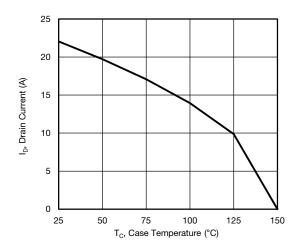


Fig. 10 - Maximum Drain Current vs. Case Temperature

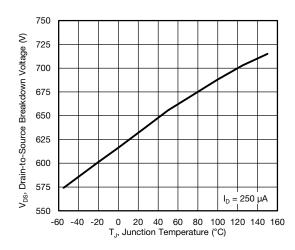


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

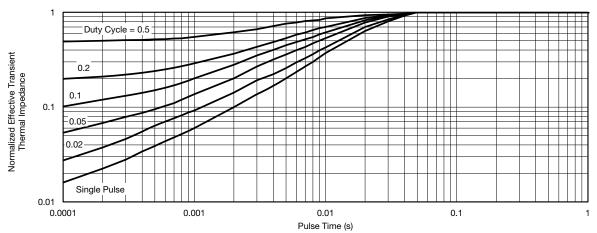


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

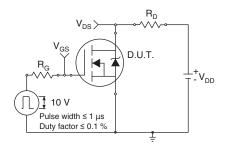


Fig. 13 - Switching Time Test Circuit

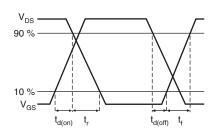


Fig. 14 - Switching Time Waveforms

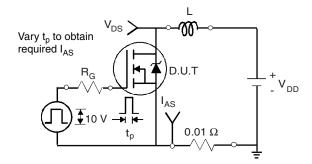


Fig. 15 - Unclamped Inductive Test Circuit

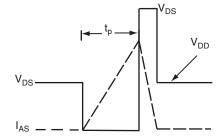


Fig. 16 - Unclamped Inductive Waveforms

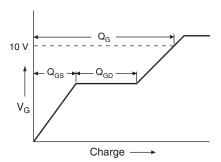


Fig. 17 - Basic Gate Charge Waveform

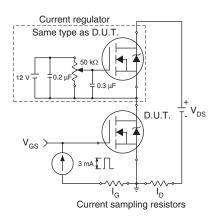
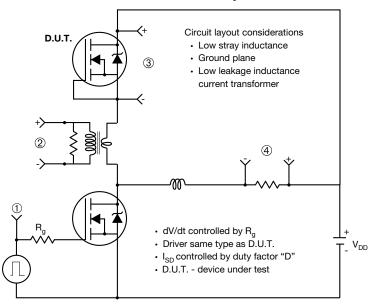


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



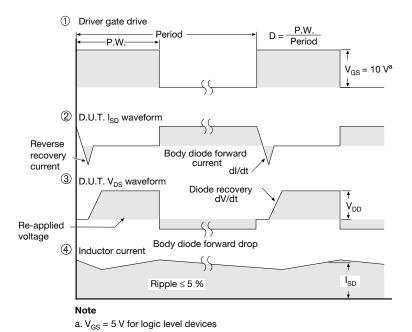
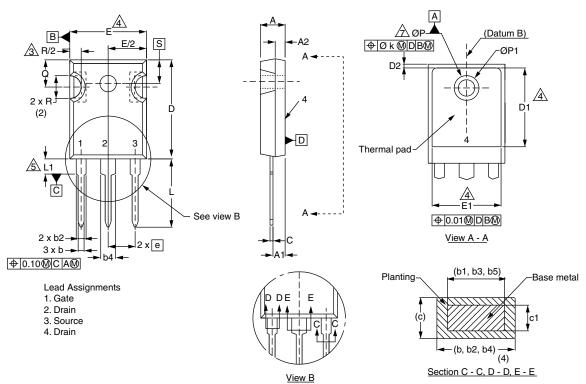


Fig. 19 - For N-Channel

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TO-247AC (High Voltage)



	MILLIN	IETERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
С	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

	MILLIM	IETERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	ı	0.540	ı
е	5.46	BSC	0.215 BSC	
Øk	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62	7.62 BSC		BSC
ØΡ	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	
0.01 200				

ECN: X13-0103-Rev. D, 01-Jul-13

DWG: 5971

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Contour of slot optional.
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- 4. Thermal pad contour optional with dimensions D1 and E1.
 5. Lead finish uncontrolled in L1.
- 6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- 7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
- 8. Xian and Mingxin actually photo.





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