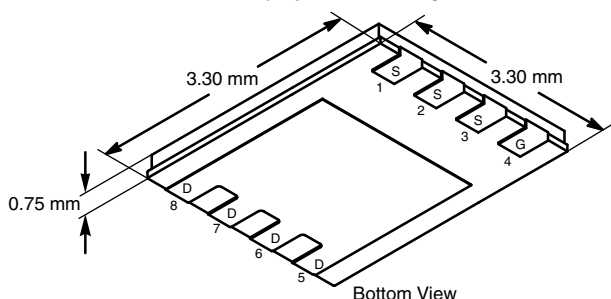


N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^{f, g}	Q _g (Typ.)
20	0.0039 at V _{GS} = 4.5 V	50	22.5 nC
	0.0042 at V _{GS} = 3.7 V	50	
	0.0058 at V _{GS} = 2.5 V	50	

Thin PowerPAK® 1212-8



Ordering Information:

SiS612EDNT-T1-GE3 (Lead (Pb)-free and Halogen-free)

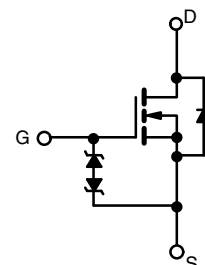
FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Low Thermal Resistance PowerPAK Package with Small Size and 0.75 mm Profile
- Typical ESD performance 3400 V
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Battery Switch / Load Switch
- Power Management for Tablet PCs and Mobile Computing



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	50 ^g
		T _C = 70 °C	50 ^g
		T _A = 25 °C	24.6 ^{a, b}
		T _A = 70 °C	19.7 ^{a, b}
Pulsed Drain Current (t = 100 μs)	I _{DM}	200	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	43.3
		T _A = 25 °C	3.1 ^{a, b}
Single Pulse Avalanche Current	I _{AS}	20	
Single Pulse Avalanche Energy	E _{AS}	20	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	52
		T _C = 70 °C	33
		T _A = 25 °C	3.7 ^{a, b}
		T _A = 70 °C	2.4 ^{a, b}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, e}	R _{thJA}	24	33	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	1.9	2.4	

Notes

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 81 °C/W.
- Based on T_C = 25 °C.
- Package limited.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		18		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 3.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 mA	0.5		1.2	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 10	μA
		V _{DS} = 0 V, V _{GS} = ± 4.5 V			± 1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 14 A		0.0032	0.0039	Ω
		V _{GS} = 3.7 V, I _D = 14 A		0.0035	0.0042	
		V _{GS} = 2.5 V, I _D = 13 A		0.0041	0.0058	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 14 A		50		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		2060		pF
Output Capacitance	C _{oss}			558		
Reverse Transfer Capacitance	C _{rss}			365		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 20 A		46	70	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 20 A		22.5	34	
Gate-Source Charge	Q _{gs}			4.1		
Gate-Drain Charge	Q _{gd}			5.3		
Gate Resistance	R _g	f = 1 MHz	0.2	1	2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		16	24	ns
Rise Time	t _r			65	98	
Turn-Off DelayTime	t _{d(off)}			40	60	
Fall Time	t _f			12	20	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		9	18	
Rise Time	t _r			5	10	
Turn-Off DelayTime	t _{d(off)}			34	51	
Fall Time	t _f			4	8	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			50	A
Pulse Diode Forward Current (t = 100 μs)	I _{SM}				200	
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V		0.75	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		22	44	ns
Body Diode Reverse Recovery Charge	Q _{rr}			10	20	nC
Reverse Recovery Fall Time	t _a			11		ns
Reverse Recovery Rise Time	t _b			11		

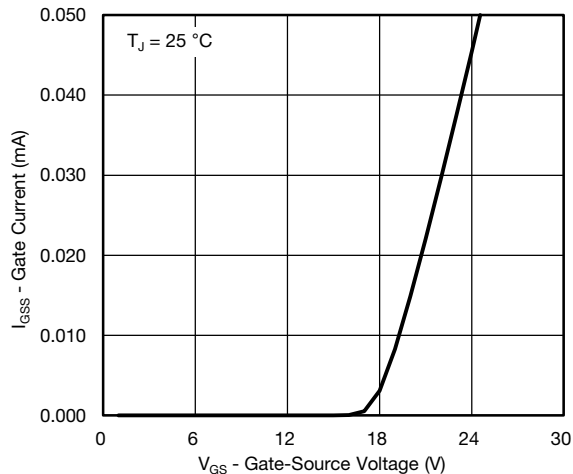
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

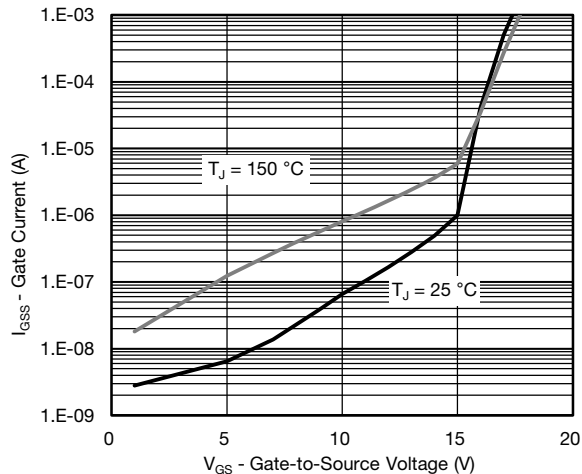
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



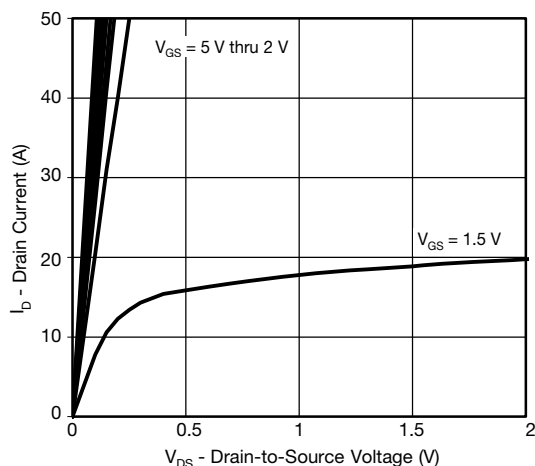
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



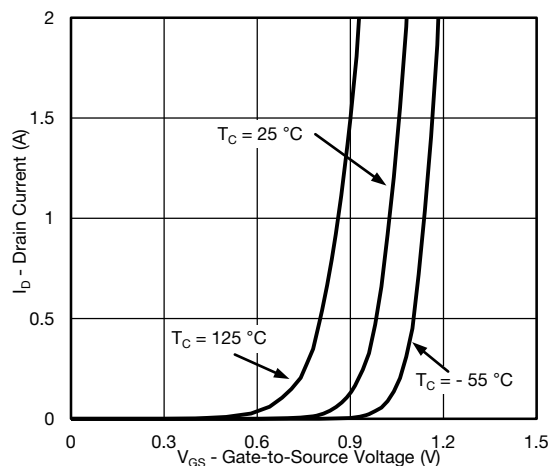
Gate Current vs. Gate-to-Source Voltage



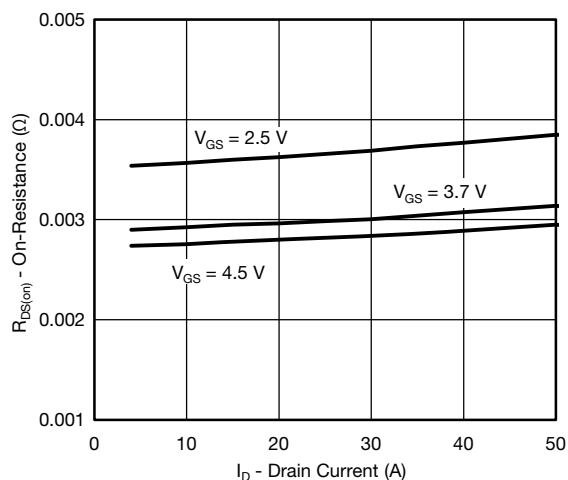
Gate Current vs. Gate-to-Source Voltage



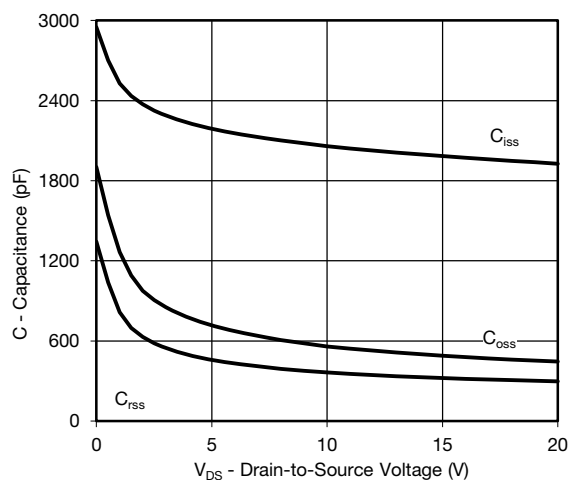
Output Characteristics



Transfer Characteristics



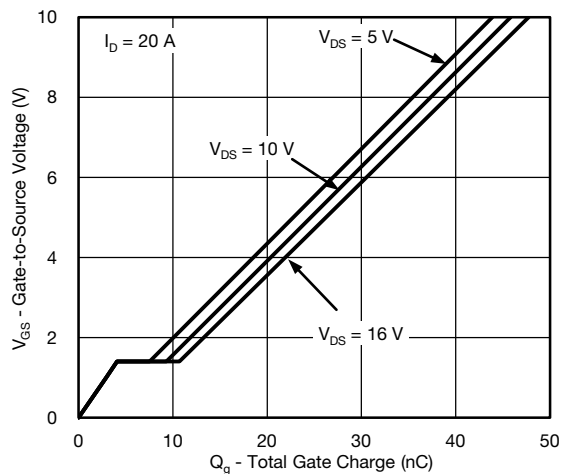
On-Resistance vs. Drain Current and Gate Voltage



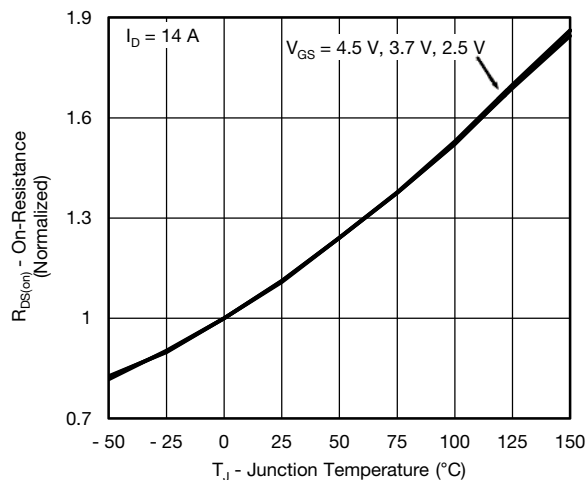
Capacitance



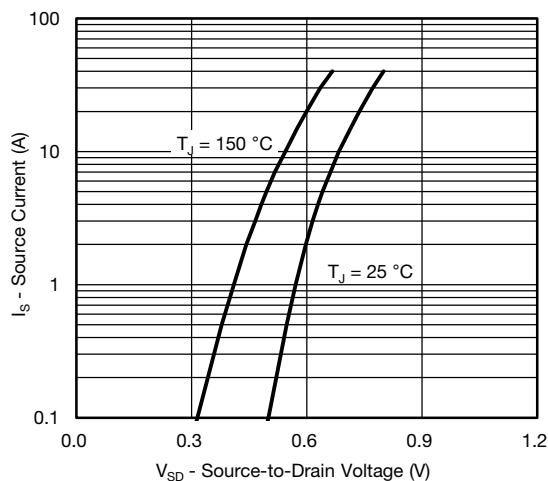
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



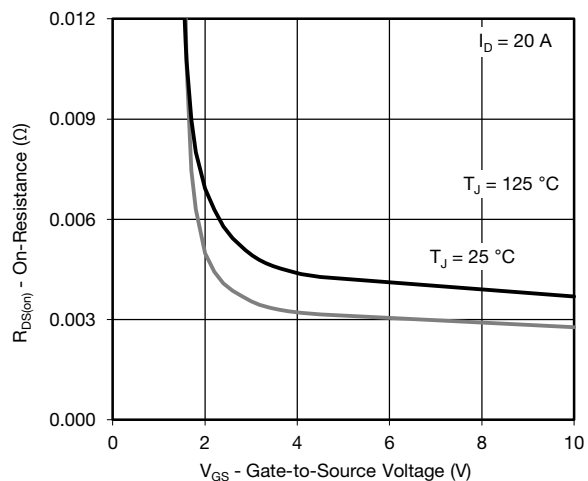
Gate Charge



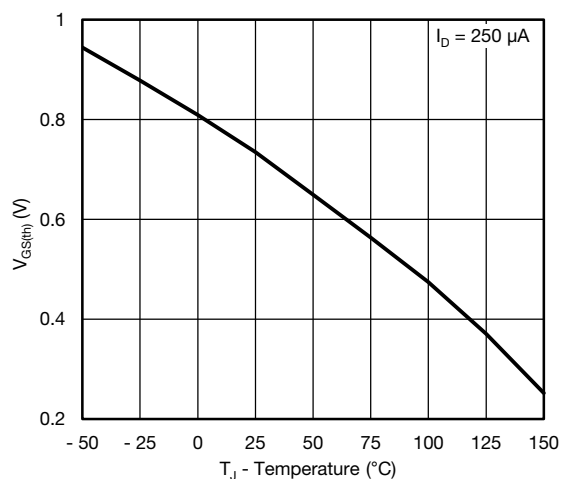
On-Resistance vs. Junction Temperature



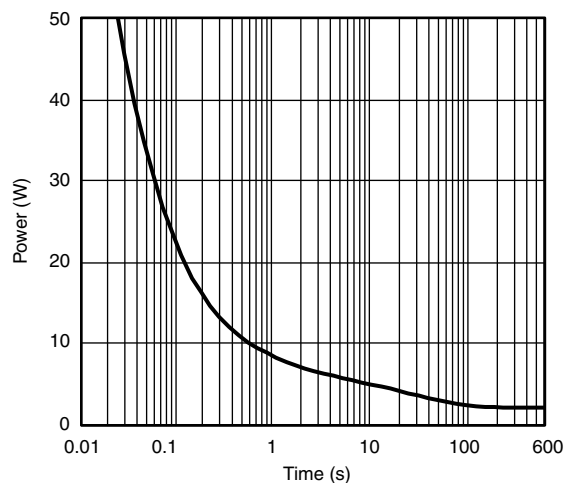
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



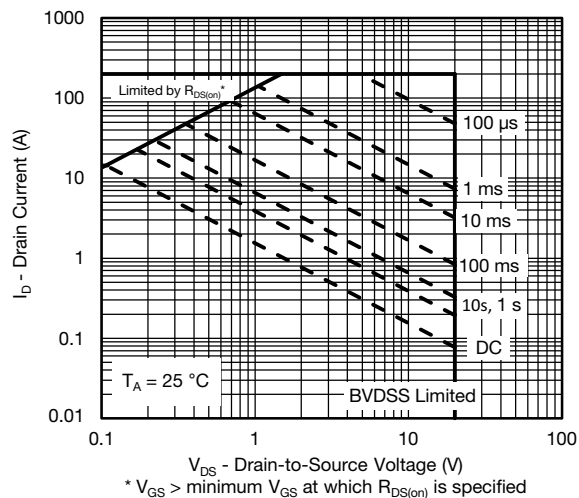
Threshold Voltage



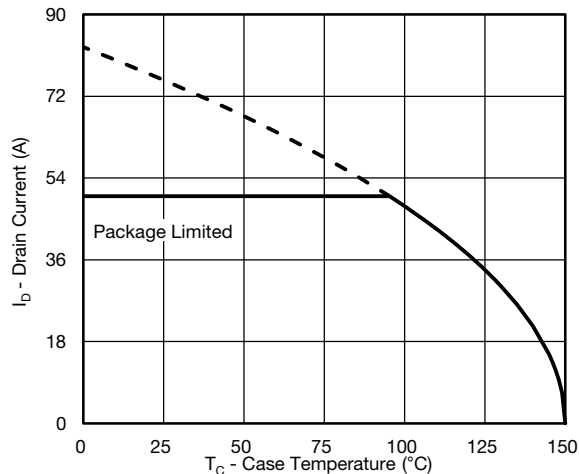
Single Pulse Power, Junction-to-Ambient



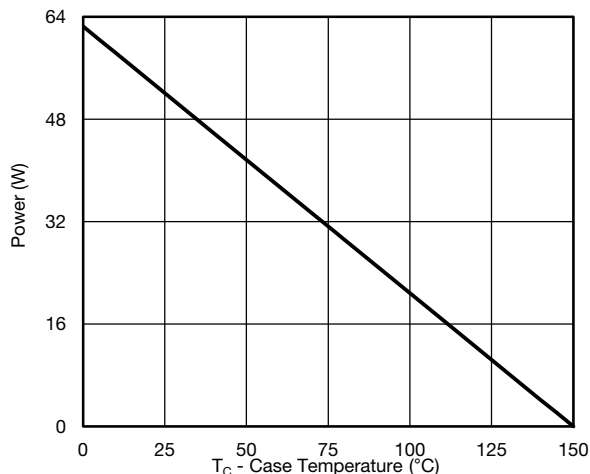
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area



Current Derating*

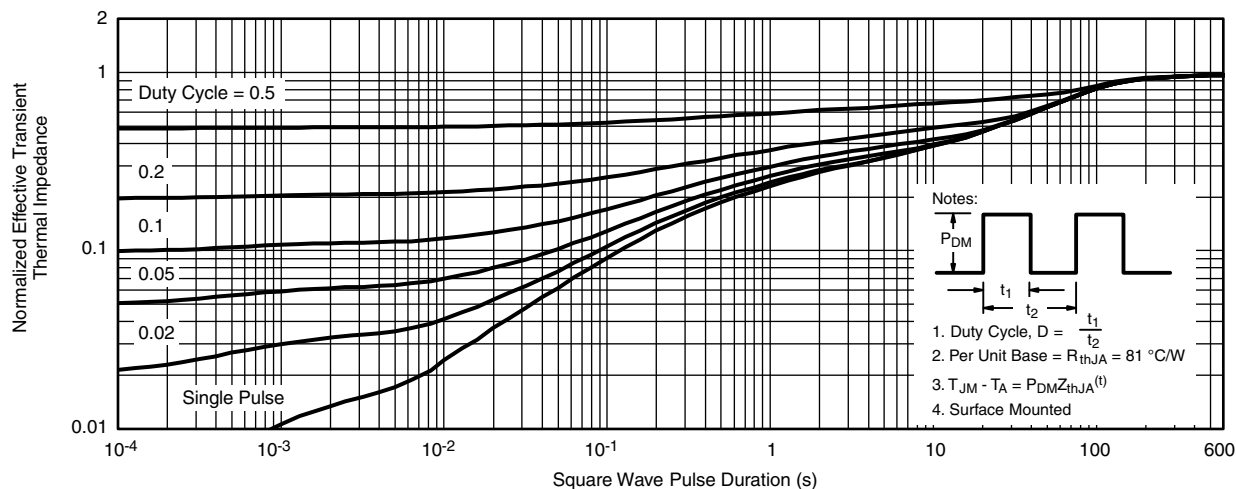


Power, Junction-to-Case

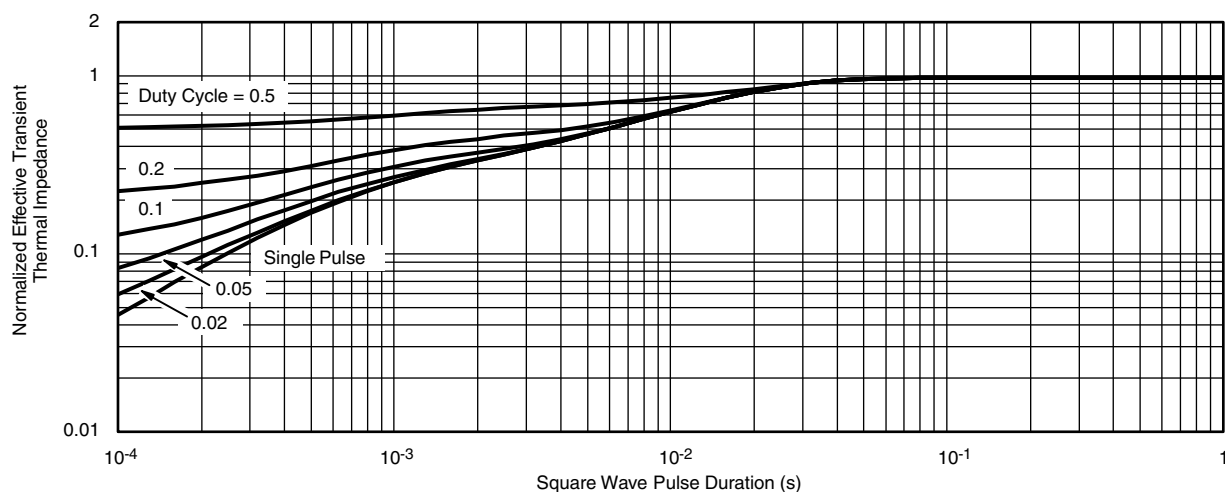
* The power dissipation P_D is based on $T_{J(max.)} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

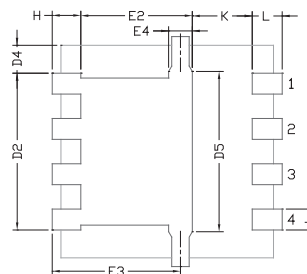
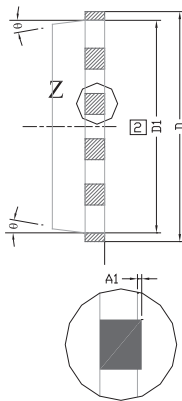
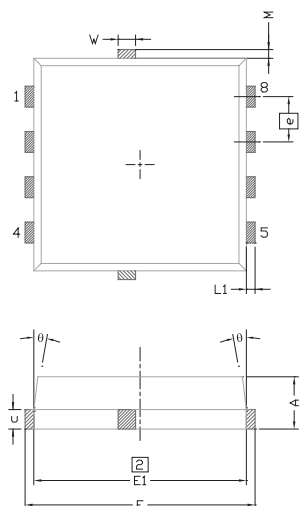


Normalized Thermal Transient Impedance, Junction-to-Case

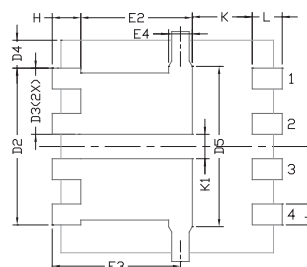
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PowerPAK® 1212-8T



BACKSIDE VIEW OF SINGLE PAD



BACKSIDE VIEW OF DUAL PAD

NOTE:	
1	MILLIMETER WILL GOVERN
2	DIMENSIONS EXCLUSIVE OF MOLD GATE BURRS.
3	DIMENSIONS EXCLUSIVE OF MOLD FLASH AND CUTTING BURRS.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 TYP.			0.0185 TYP.		
D5	2.3 TYP.			0.090 TYP.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 TYP.			0.013 TYP.		
e	0.65 BSC			0.026 BSC		
K	0.86 TYP.			0.034 TYP.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

ECN: T13-0056-Rev. A, 18-Feb-13

DWG: 6012



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