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# MSM7717-01

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## Single Rail CODEC

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### GENERAL DESCRIPTION

The MSM7717 is a single-channel CODEC CMOS IC for voice signals ranging from 300 to 3400 Hz with filters for A/D and D/A conversion.

Designed especially for a single-power supply and low-power applications, the device is optimized for ISDN terminals and telephone terminals in digital wireless systems.

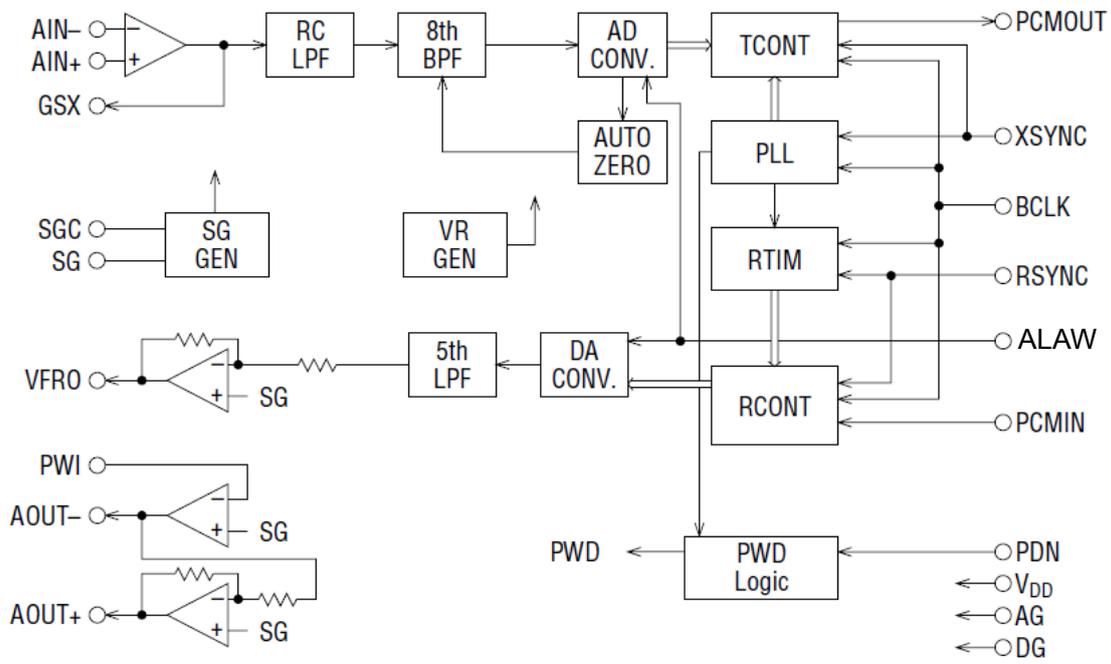
The device uses the same transmission clocks as those used in the MSM7508B and MSM7509B.

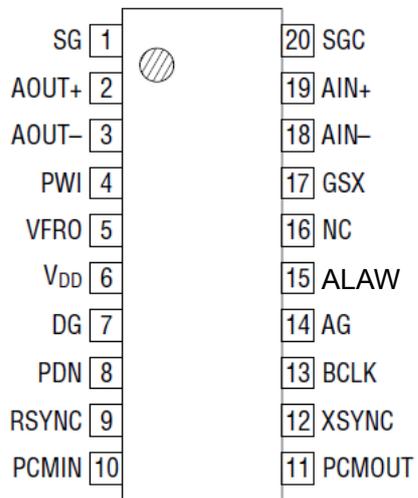
The analog output, which can drive a 1.2 k $\Omega$  load, can directly drive a handset receiver differentially.

### FEATURES

- Single power supply : 2.7 V to 3.8 V
- Low power consumption
  - Operating mode : 20 mW Typ.  $V_{DD}=3V$
  - Power-down mode : 0.03mW Typ.  $V_{DD}=3V$
- Conforms to ITU-T Companding law
  - $\mu/A$ -law pin selectable
- Built-in PLL eliminates a master clock
- Serial data rate : 64/128/256/512/1024 kHz  
96/192/384/768/1536/1544/2048/200 kHz
- Adjustable transmit gain
- Adjustable receive gain
- Built-in reference voltage supply
- Package:
  - 20-pin plastic SSOP (SSOP20-P-250-0.95-K)

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**

NC : No connect pin

**20-Pin Plastic SSOP**

## PIN AND FUNCTIONAL DESCRIPTIONS

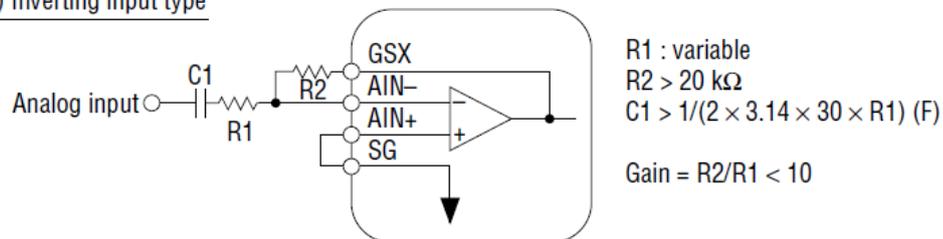
### AIN+, AIN-, GSX

Transmit analog input and transmit level adjustment.

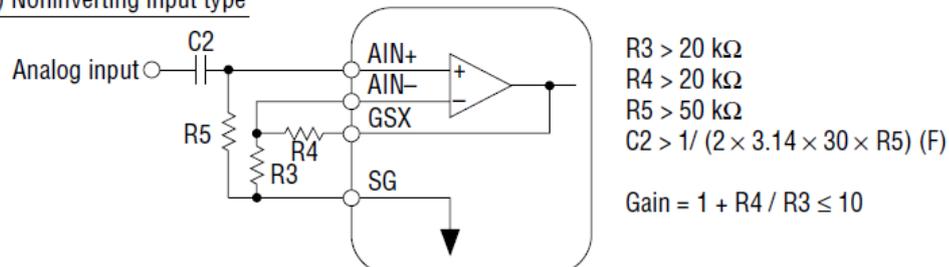
AIN+ is a non-inverting input to the op-amp; AIN- is an inverting input to the op-amp; GSX is connected to the output of the op-amp.

The level adjustment should be performed in any method shown below. When not using AIN- and AIN+, connect AIN- to GSX and AIN+ to SG. During power-saving and power-down modes, the GSX output is at AG voltage.

#### 1) Inverting input type



#### 2) Noninverting input type



### AG

Analog signal ground.

### VFRO

Receive filter output.

The output signal has an amplitude of  $2.0 V_{PP}$  above and below the signal ground voltage (SG) when the digital signal of +3 dBm0 is input to PCMIN and can drive a load of  $20 \text{ k}\Omega$  or more. For driving a load of less than  $20 \text{ k}\Omega$ , connect a resistor of  $20 \text{ k}\Omega$  or more between the pins VFRO and PWL.

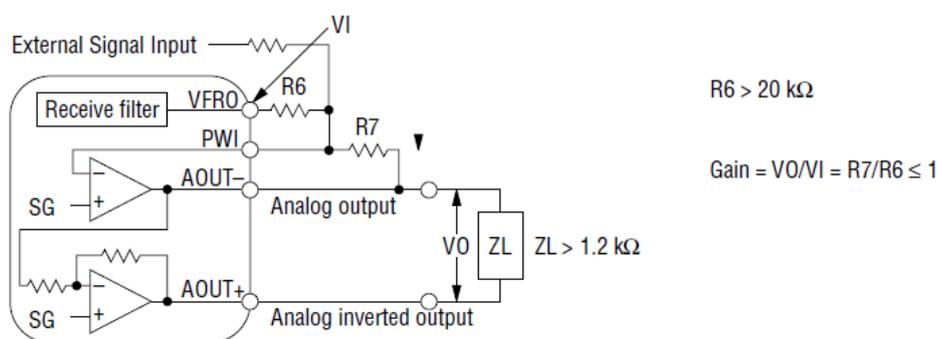
During power-saving mode this output is in a high impedance state, and during power-down mode, the VFRO output is at an SG level.

When adjusting the receive signal on the basis of frequency characteristics, refer to the Frequency Characteristics Adjustment Circuit.

## PWI, AOUT+, AOUT-

PWI is connected to the inverting input of the receive driver.

The receive driver output is connected to the AOUT- pin. Therefore, the receive level can be adjusted with the pins VFRO, PWI, and AOUT-. When the PWI pin is not used, the PWI pin to the AOUT- pin, and leave the pins AOUT- and AOUT+ open. The output of AOUT+ is inverted with respect to the output of AOUT-. Since these outputs provide differential drive of an impedance of 1.2 k $\Omega$ , these outputs can directly be connected to a receiver of handset using a piezoelectric earphone. Refer to the application example. Since the driver amplifiers are being activated during the power-saving mode, the amplifiers can output other external signals from AOUT+ and AOUT- pins. AOUT+ and AOUT- outputs are in a high impedance state during the power-down mode.



## V<sub>DD</sub>

Power supply for 2.7 V to 3.8 V. (Typically 3.0 V)

## PCMIN

PCM data input.

A serial PCM data input to this pin is converted to an analog signal in synchronization with the RSYNC signal and BCLK signal.

The data rate of PCM is equal to the frequency of the BCLK signal.

PCM signal is shifted in at a falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.

The start of the PCM data (MSD) is identified at the rising edge of RSYNC.

## BCLK

Shift clock signal input for the PCMIN and PCMOUT signal.

The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, or 2048 kHz. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

The power-saving state means that the reference voltage generator (VRGEN), PLL, and receive driver amplifiers are in the operating mode and the other circuits are in the non-operating mode.

**RSYNC**

Receive synchronizing signal input.

Eight required bits are selected from serial PCM signals on the PCMIN pin by the receive synchronizing signal.

Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK. The frequency should be  $8\text{ kHz} \pm 50\text{ ppm}$  to guarantee the AC characteristics which are mainly the frequency characteristics of the receive section.

However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of  $8\text{ kHz} \pm 2\text{ kHz}$ , but the electrical characteristics in this specification are not guaranteed.

**XSYNC**

Transmit synchronizing signal input.

The PCM output signal from the PCMOUT pin is output in synchronization with this signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section. This synchronizing signal must be synchronized in phase with BCLK.

The frequency should be  $8\text{ kHz} \pm 50\text{ ppm}$  to guarantee the AC characteristics which are mainly the frequency characteristics of the transmit section.

However, if the frequency characteristic of an applied system is not specified exactly, this device operates in the range of  $8\text{ kHz} \pm 2\text{ kHz}$ , but the electrical characteristics in this specification are not guaranteed.

Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

**DG**

Ground for the digital signal circuits.

This ground is separate from the analog signal ground AG. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground AG.

**PDN**

Power down control signal.

A logic "0" level drives both transmit and receive circuits to a power down state.

**PCMOUT**

PCM signal output.

Synchronizing with the rising edge of the BCLK signal, the PCM output signal is output from MSD in a sequential order.

MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power saving or power down mode.

A pull-up resistor must be connected to this pin because its output is configured as an open drain. This device is compatible with the ITU-T recommendation on coding law and output coding format.

| Input/Output Level | PCMIN/PCMOUT |   |   |   |       |   |   |   |   |   |   |   |   |   |   |   |
|--------------------|--------------|---|---|---|-------|---|---|---|---|---|---|---|---|---|---|---|
|                    | $\mu$ -law   |   |   |   | A-law |   |   |   |   |   |   |   |   |   |   |   |
| +Full scale        | MSD          |   |   |   | MSD   |   |   |   |   |   |   |   |   |   |   |   |
|                    | 1            | 0 | 0 | 0 | 0     | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| +0                 | 1            | 1 | 1 | 1 | 1     | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -0                 | 0            | 1 | 1 | 1 | 1     | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -Full scale        | 0            | 0 | 0 | 0 | 0     | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

**SG**

Signal ground voltage output.

The output voltage is 1/2 of the power supply voltage.

The output drive current capability is  $\pm 200 \mu\text{A}$ .

This pin provides the SG level for CODEC peripherals.

This output voltage level is undefined during power-saving or power-down mode.

**SGC**

Used to generate the signal ground voltage level by connecting a bypass capacitor.

Connect a  $0.1 \mu\text{F}$  capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

**ALAW**

Control signal input of the companding law selection. The CODEC will operate in the  $\mu$ -law when this pin is at a logic "0" level and the CODEC will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the  $\mu$ -law if the pin is left open, since the pin is internally pulled down.

**ABSOLUTE MAXIMUM RATINGS**

| Parameter             | Symbol    | Condition | Rating                 | Unit |
|-----------------------|-----------|-----------|------------------------|------|
| Power Supply Voltage  | $V_{DD}$  | —         | -0.3 to +7             | V    |
| Analog Input Voltage  | $V_{AIN}$ | —         | -0.3 to $V_{DD} + 0.3$ | V    |
| Digital Input Voltage | $V_{DIN}$ | —         | -0.3 to $V_{DD} + 0.3$ | V    |
| Storage Temperature   | $T_{STG}$ | —         | -55 to +150            | °C   |

**RECOMMENDED OPERATING CONDITIONS**

| Parameter                        | Symbol    | Condition                      | Min.  | Typ. | Max.                 | Unit     |
|----------------------------------|-----------|--------------------------------|---|------|----------------------|----------|
| Power Supply Voltage             | $V_{DD}$  | Voltage must be fixed          | 2.7   | 3.0  | 3.8                  | V        |
| Operating Temperature            | $T_a$     | —                              | -30   | +25  | +85                  | °C       |
| Analog Input Voltage             | $V_{AIN}$ | Connect AIN- and GSX           | —   | —    | 1.4                  | $V_{PP}$ |
| High Level Input Voltage         | $V_{IH}$  | XSYNC, RSYNC, BCLK,            | $0.45 \times V_{DD}$  | —    | $V_{DD}$             | V        |
| Low Level Input Voltage          | $V_{IL}$  | PCMIN, PDN, ALAW               | 0   | —    | $0.16 \times V_{DD}$ | V        |
| Clock Frequency                  | $F_C$     | BCLK                           | 64, 128, 256, 512, 1024,<br>2048, 96, 192, 384, 768,<br>1536, 1544, 200 |      |                      | kHz      |
| Sync Pulse Frequency             | $F_S$     | XSYNC, RSYNC                   | 6.0   | 8.0  | 10                   | kHz      |
| Clock Duty Ratio                 | $D_C$     | BCLK                           | 40  | 50   | 60                   | %        |
| Digital Input Rise Time          | $t_{ir}$  | XSYNC, RSYNC, BCLK,            | —   | —    | 50                   | ns       |
| Digital Input Fall Time          | $t_{if}$  | PCMIN, PDN, ALAW               | —   | —    | 50                   | ns       |
| Transmit Sync Pulse Setting Time | $t_{XS}$  | BCLK→XSYNC, See Fig. 1         | 100   | —    | —                    | ns       |
|                                  | $t_{SX}$  | XSYNC→BCLK, See Fig. 1         | 100   | —    | —                    | ns       |
| Receive Sync Pulse Setting Time  | $t_{RS}$  | BCLK→RSYNC, See Fig. 1         | 100   | —    | —                    | ns       |
|                                  | $t_{SR}$  | RSYNC→BCLK, See Fig. 1         | 100   | —    | —                    | ns       |
| High Level Sync Pulse Width      | $t_{WSH}$ | XSYNC, RSYNC, See Fig. 1       | 1 BCLK  | —    | —                    | μs       |
| Low Level Sync Pulse Width       | $t_{WSL}$ | XSYNC, RSYNC, See Fig. 1       | 1 BCLK  | —    | —                    | μs       |
| PCMIN Setup Time                 | $t_{DS}$  | See Timing Diagram             | 100   | —    | —                    | ns       |
| PCMIN Hold Time                  | $t_{DH}$  | See Timing Diagram             | 100   | —    | —                    | ns       |
| Digital Output Load              | $R_{DL}$  | Pull-up resistor               | 0.5   | —    | —                    | kΩ       |
|                                  | $C_{DL}$  | —                              | —   | —    | 100                  | pF       |
| Analog Input Allowable DC Offset | $V_{off}$ | Transmit gain stage, Gain = 1  | -100  | —    | +100                 | mV       |
|                                  |           | Transmit gain stage, Gain = 10 | -10   | —    | +10                  | mV       |
| Allowable Jitter Width           | —         | XSYNC, RSYNC, BCLK             | —   | —    | 1000                 | ns       |

## ELECTRICAL CHARACTERISTICS

### DC and Digital Interface Characteristics

( $V_{DD} = 2.7\text{ V to }3.8\text{ V}$ ,  $T_a = -30^\circ\text{C to }+85^\circ\text{C}$ )

| Parameter                        | Symbol    | Condition  | Min.                    | Typ.  | Max.                 | Unit          |    |
|----------------------------------|-----------|--|-------------------------|-------|----------------------|---------------|----|
| Power Supply Current             | $I_{DD1}$ | Operating mode                                     | $V_{DD} = 3.8\text{ V}$ | —     | 10                   | 14            | mA |
|                                  |           | No signal  | $V_{DD} = 3.0\text{ V}$ | —     | 6.5                  | 10.0          |    |
|                                  | $I_{DD2}$ | Power-saving mode, PDN = 1,<br>BCLK or XSYNC → OFF | —                       | 2.0   | 8.0                  | mA            |    |
|                                  | $I_{DD3}$ | Power-down mode, PDN = 0,<br>BCLK OFF              | —                       | 0.005 | 0.05                 | mA            |    |
| High Level Input Voltage         | $V_{IH}$  | XSYNC, RSYNC, BCLK,<br>PCMIN, PDN, ALAW            | $0.45 \times V_{DD}$    | —     | $V_{DD}$             | V             |    |
| Low Level Input Voltage          | $V_{IL}$  | XSYNC, RSYNC, BCLK,<br>PCMIN, PDN, ALAW            | 0.0                     | —     | $0.16 \times V_{DD}$ | V             |    |
| High Level Input Leakage Current | $I_{IH}$  | —  | —                       | —     | 2.0                  | $\mu\text{A}$ |    |
| Low Level Input Leakage Current  | $I_{IL}$  | —  | —                       | —     | 0.5                  | $\mu\text{A}$ |    |
| Digital Output Low Voltage       | $V_{OL}$  | Pull-up resistor > 500 $\Omega$                    | 0.0                     | 0.2   | 0.4                  | V             |    |
| Digital Output Leakage Current   | $I_O$     | —  | —                       | —     | 10                   | $\mu\text{A}$ |    |
| Input Capacitance                | $C_{IN}$  | —  | —                       | 5     | —                    | pF            |    |

**Transmit Analog Interface Characteristics** $(V_{DD} = 2.7 \text{ V to } 3.8 \text{ V, } T_a = -30^\circ\text{C to } +85^\circ\text{C})$ 

| Parameter               | Symbol     | Condition              | Min. | Typ. | Max. | Unit      |
|-------------------------|------------|------------------------|------|------|------|-----------|
| Input Resistance        | $R_{INX}$  | AIN+, AIN-             | 10   | —    | —    | $M\Omega$ |
| Output Load Resistance  | $R_{LGX}$  | GSX with respect to SG | 20   | —    | —    | $k\Omega$ |
| Output Load Capacitance | $C_{LGX}$  |                        | —    | —    | 30   | pF        |
| Output Amplitude        | $V_{OGX}$  |                        | -0.7 | —    | +0.7 | V         |
| Offset Voltage          | $V_{OSGX}$ | Gain = 1               | -20  | —    | +20  | mV        |

**Receive Analog Interface Characteristics** $(V_{DD} = 2.7 \text{ V to } 3.8 \text{ V, } T_a = -30^\circ\text{C to } +85^\circ\text{C})$ 

| Parameter               | Symbol     | Condition  | Min. | Typ. | Max. | Unit      |
|-------------------------|------------|--|------|------|------|-----------|
| Input Resistance        | $R_{INPW}$ | PWI  | 10   | —    | —    | $M\Omega$ |
| Output Load Resistance  | $R_{LVF}$  | VFRO with respect to SG                                      | 20   | —    | —    | $k\Omega$ |
|                         | $R_{LAO}$  | AOUT+, AOUT- (each) with respect to SG                       | 0.6  | —    | —    | $k\Omega$ |
| Output Load Capacitance | $C_{LVF}$  | VFRO   | —    | —    | 30   | pF        |
|                         | $C_{LAO}$  | AOUT+, AOUT-   | —    | —    | 50   | pF        |
| Output Amplitude        | $V_{OVF}$  | VFRO, $R_L = 20 \text{ k}\Omega$ with respect to SG          | -1.0 | —    | +1.0 | V         |
|                         | $V_{OAO}$  | AOUT+, AOUT-, $R_L = 0.6 \text{ k}\Omega$ with respect to SG | -1.0 | —    | +1.0 | V         |
| Offset Voltage          | $V_{OSVF}$ | VFRO with respect to SG                                      | -100 | —    | +100 | mV        |
|                         | $V_{OSAO}$ | AOUT+, AOUT-, Gain = 1 with respect to SG                    | -100 | —    | +100 | mV        |

## AC Characteristics

(F<sub>S</sub> = 8 kHz, V<sub>DD</sub> = 2.7 V to 3.8 V, T<sub>a</sub> = -30°C to +85°C)

| Parameter                           | Symbol  | Freq. (Hz) | Level (dBm0) | Condition | Min.      | Typ.  | Max.  | Unit |
|-------------------------------------|---------|------------|--------------|-----------|-----------|-------|-------|------|
| Transmit Frequency Response         | Loss T1 | 60         | 0            |           | 20        | 26    | —     | dB   |
|                                     | Loss T2 | 300        |              |           | -0.15     | +0.07 | +0.2  |      |
|                                     | Loss T3 | 1020       |              |           | Reference |       |       |      |
|                                     | Loss T4 | 2020       |              |           | -0.15     | -0.01 | +0.2  |      |
|                                     | Loss T5 | 3000       |              |           | -0.15     | +0.15 | +0.2  |      |
|                                     | Loss T6 | 3400       |              |           | 0         | 0.4   | 0.8   |      |
| Receive Frequency Response          | Loss R1 | 300        | 0            |           | -0.15     | -0.03 | +0.2  | dB   |
|                                     | Loss R2 | 1020       |              |           | Reference |       |       |      |
|                                     | Loss R3 | 2020       |              |           | -0.15     | -0.02 | +0.2  |      |
|                                     | Loss R4 | 3000       |              |           | -0.15     | +0.15 | +0.25 |      |
|                                     | Loss R5 | 3400       |              |           | 0         | 0.56  | 0.8   |      |
| Transmit Signal to Distortion Ratio | SD T1   | 1020       | 3            | *1        | 35        | 43    | —     | dB   |
|                                     | SD T2   |            | 0            |           | 35        | 41    | —     |      |
|                                     | SD T3   |            | -30          |           | 35        | 38    | —     |      |
|                                     | SD T4   |            | -40          |           | 28        | 30    | —     |      |
|                                     | SD T5   |            | -45          |           | 23        | 25    | —     |      |
| Receive Signal to Distortion Ratio  | SD R1   | 1020       | 3            | *1        | 36        | 43    | —     | dB   |
|                                     | SD R2   |            | 0            |           | 36        | 41    | —     |      |
|                                     | SD R3   |            | -30          |           | 36        | 40    | —     |      |
|                                     | SD R4   |            | -40          |           | 30        | 33.5  | —     |      |
|                                     | SD R5   |            | -45          |           | 29        | 32    | —     |      |
| Transmit Gain Tracking              | GT T1   | 1020       | 3            |           | -0.3      | +0.01 | +0.3  | dB   |
|                                     | GT T2   |            | -10          |           | Reference |       |       |      |
|                                     | GT T3   |            | -40          |           | -0.3      | 0     | +0.3  |      |
|                                     | GT T4   |            | -50          |           | -0.6      | -0.03 | +0.6  |      |
|                                     | GT T5   |            | -55          |           | -1.2      | +0.15 | +1.2  |      |
| Receive Gain Tracking               | GT R1   | 1020       | 3            |           | -0.3      | -0.06 | +0.3  | dB   |
|                                     | GT R2   |            | -10          |           | Reference |       |       |      |
|                                     | GT R3   |            | -40          |           | -0.3      | -0.02 | +0.3  |      |
|                                     | GT R4   |            | -50          |           | -0.6      | -0.02 | +0.6  |      |
|                                     | GT R5   |            | -55          |           | -1.2      | -0.27 | +1.2  |      |

\*1 Psophometric filter is used.

\*2 Upper columns are specified for the  $\mu$ -law, lower for the A-law.

## AC Characteristics (Continued)

(F<sub>S</sub> = 8 kHz, V<sub>DD</sub> = 2.7 V to 3.8 V, T<sub>a</sub> = -30°C to +85°C)

| Parameter  | Symbol             | Freq. (Hz) | Level (dBm0) | Condition   | Min.            | Typ.           | Max.  | Unit             |
|--|--------------------|------------|--------------|---|-----------------|----------------|-------|------------------|
| Idle Channel Noise                                     | Nidle T            | —          | —            | A <sub>IN</sub> = SG<br>*1  | — <sup>*2</sup> | -72.5<br>-70.5 | -68   | dBm0p            |
|  | Nidle R            | —          | —            | *1 *3   | —               | -76.5          | -74   |                  |
| Absolute Level (Initial Difference)                    | AV T               | 1020       | 0            | V <sub>DD</sub> = 3.0 V<br>T <sub>a</sub> = 25°C<br>*4                    | 0.338           | 0.35           | 0.362 | V <sub>rms</sub> |
|  | AV R               |            |              |   | 0.483           | 0.5            | 0.518 |                  |
| Absolute Level<br>(Deviation of Temperature and Power) | AV Tt              | 1020       | 0            | V <sub>DD</sub> = 2.7 V<br>to 3.8 V<br>T <sub>a</sub> = -30<br>to 85°C *4 | -0.2            | —              | +0.2  | dB               |
|  | AV Rt              |            |              |   | -0.2            | —              | +0.2  | dB               |
| Absolute Delay   | Td                 | 1020       | 0            | A to A<br>BCLK<br>= 64 kHz  | —               | —              | 0.6   | ms               |
| Transmit Group Delay                                   | t <sub>GD</sub> T1 | 500        | 0            | *5  | —               | 0.19           | 0.75  | ms               |
|  | t <sub>GD</sub> T2 | 600        |              |   | —               | 0.11           | 0.35  |                  |
|  | t <sub>GD</sub> T3 | 1000       |              |   | —               | 0.02           | 0.125 |                  |
|  | t <sub>GD</sub> T4 | 2600       |              |   | —               | 0.05           | 0.125 |                  |
|  | t <sub>GD</sub> T5 | 2800       |              |   | —               | 0.07           | 0.75  |                  |
| Receive Group Delay                                    | t <sub>GD</sub> R1 | 500        | 0            | *5  | —               | 0.00           | 0.75  | ms               |
|  | t <sub>GD</sub> R2 | 600        |              |   | —               | 0.00           | 0.35  |                  |
|  | t <sub>GD</sub> R3 | 1000       |              |   | —               | 0.00           | 0.125 |                  |
|  | t <sub>GD</sub> R4 | 2600       |              |   | —               | 0.09           | 0.125 |                  |
|  | t <sub>GD</sub> R5 | 2800       |              |   | —               | 0.12           | 0.75  |                  |
| Crosstalk Attenuation                                  | CR T               | 1020       | 0            | TRANS → RECV  | 75              | 80             | —     | dB               |
|  | CR R               |            |              | RECV → TRANS  | 70              | 76             | —     |                  |

\*1 Psophometric filter is used.

\*2 Upper column is specified for the μ-law, lower for the A-law.

\*3 Input "0" code to PCMIN.

\*4 AVR is defined at VFRO output.

\*5 With respect to minimum value of the group delay distortion

## AC Characteristics (Continued)

(F<sub>S</sub> = 8 kHz, V<sub>DD</sub> = 2.7 V to 3.8 V, T<sub>a</sub> = -30°C to +85°C)

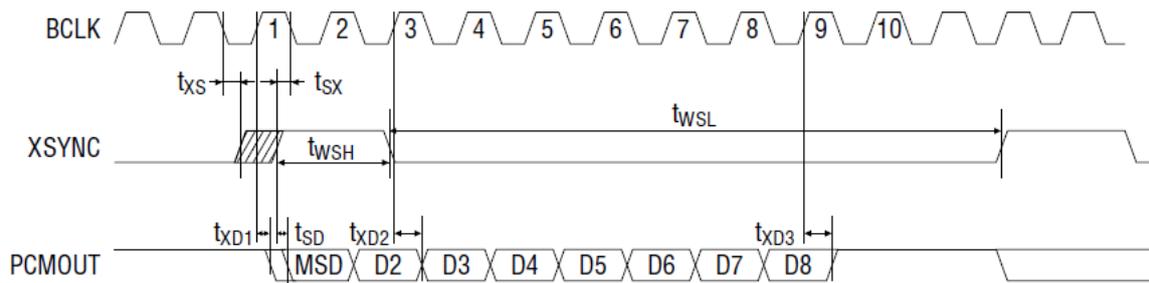
| Parameter                          | Symbol           | Freq. (Hz)                                   | Level (dBm0)        | Condition                        | Min. | Typ.  | Max. | Unit |
|------------------------------------|------------------|--|---------------------|----------------------------------|------|-------|------|------|
| Discrimination                     | DIS              | 4.6 kHz to 72 kHz                            | 0                   | 0 to 4000 Hz                     | 30   | 32    | —    | dB   |
| Out-of-band Spurious               | S                | 300 to 3400                                  | 0                   | 4.6 kHz to 100 kHz               | —    | -37.5 | -35  | dBm0 |
| Intermodulation Distortion         | IMD              | f <sub>a</sub> = 470<br>f <sub>d</sub> = 320 | -4                  | 2f <sub>a</sub> - f <sub>d</sub> | —    | -52   | -35  | dBm0 |
| Power Supply Noise Rejection Ratio | PSR T            | 0 to 50 kHz                                  | 50 mV <sub>PP</sub> | *6                               | —    | 30    | —    | dB   |
|                                    | PSR R            |  |                     |                                  |      |       |      |      |
| Digital Output Delay Time          | t <sub>SD</sub>  | C <sub>L</sub> = 100 pF + 1 LSTTL            |                     |                                  | 20   | —     | 200  | ns   |
|                                    | t <sub>XD1</sub> |  |                     |                                  | 20   | —     | 200  |      |
|                                    | t <sub>XD2</sub> |  |                     |                                  | 20   | —     | 200  |      |
|                                    | t <sub>XD3</sub> |  |                     |                                  | 20   | —     | 200  |      |

\*6 Measured under idle channel noise.

## TIMING DIAGRAM

### PCM Data Input/Output Timing

#### Transmit Timing



When  $t_{XS} \leq 1/2 \cdot F_c$ , the Delay of the MSD bit is defined as  $t_{XD1}$ .  
 When  $t_{SX} \leq 1/2 \cdot F_c$ , the Delay of the MSD bit is defined as  $t_{SD}$ .

#### Receive Timing

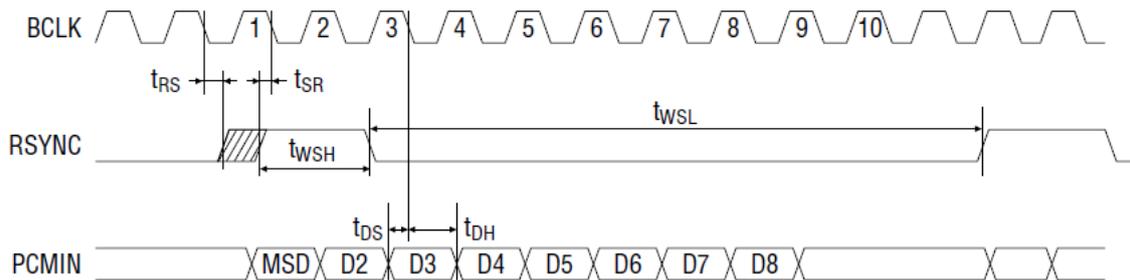
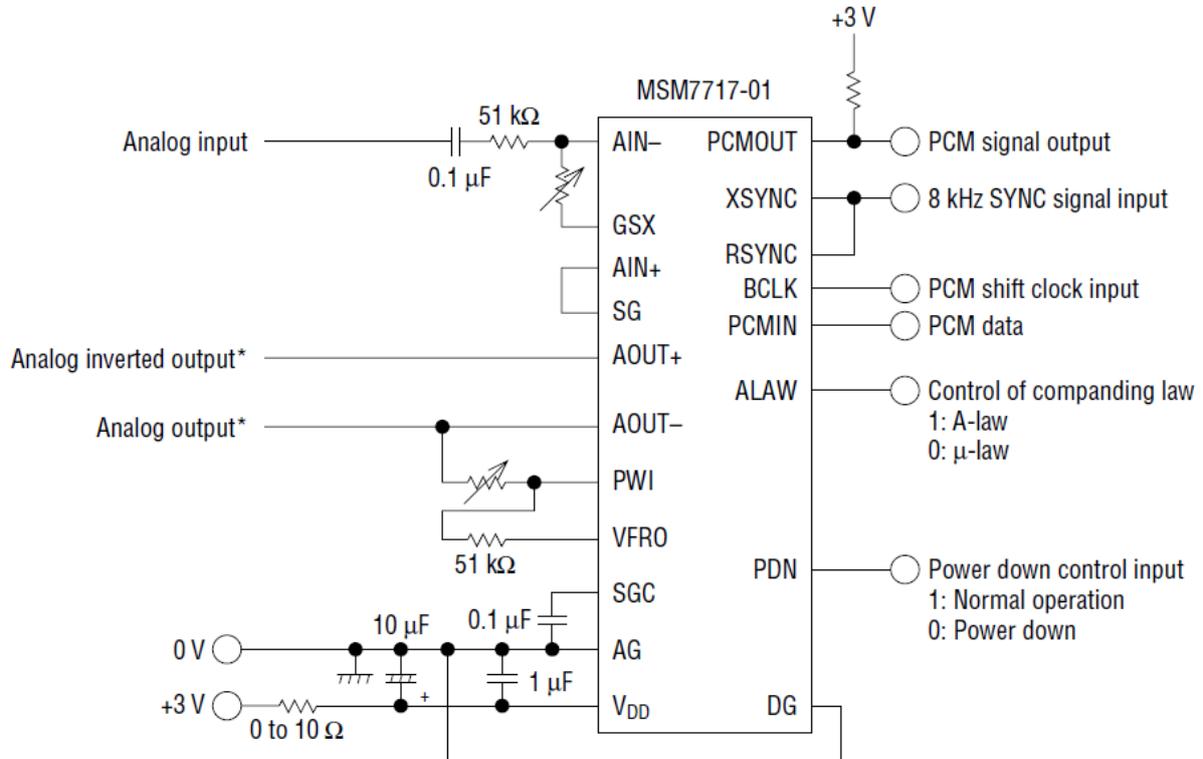


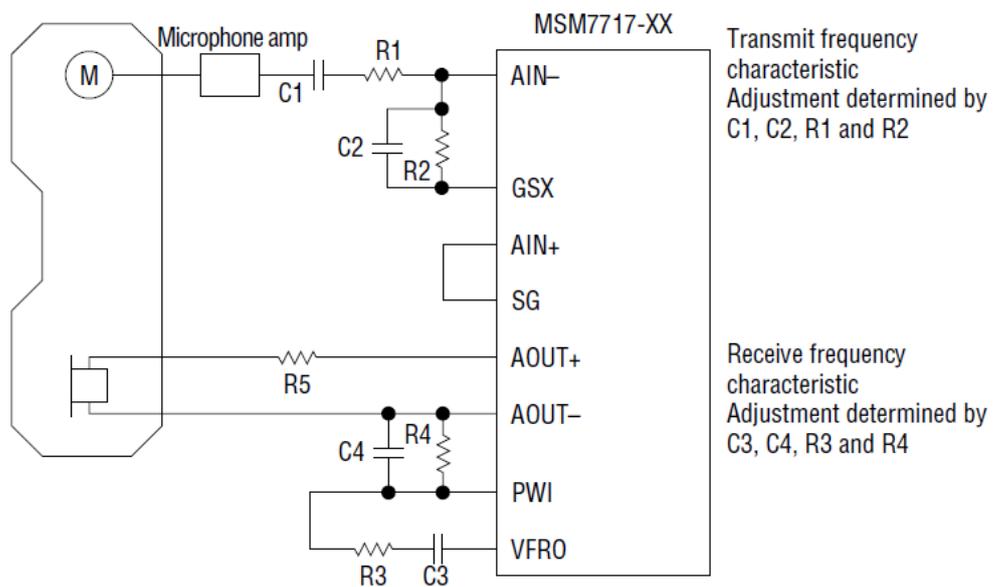
Figure 1 Basic Timing

**APPLICATION CIRCUIT**



\* These output signals have amplitudes above and below the offset level of  $V_{DD}/2$ .

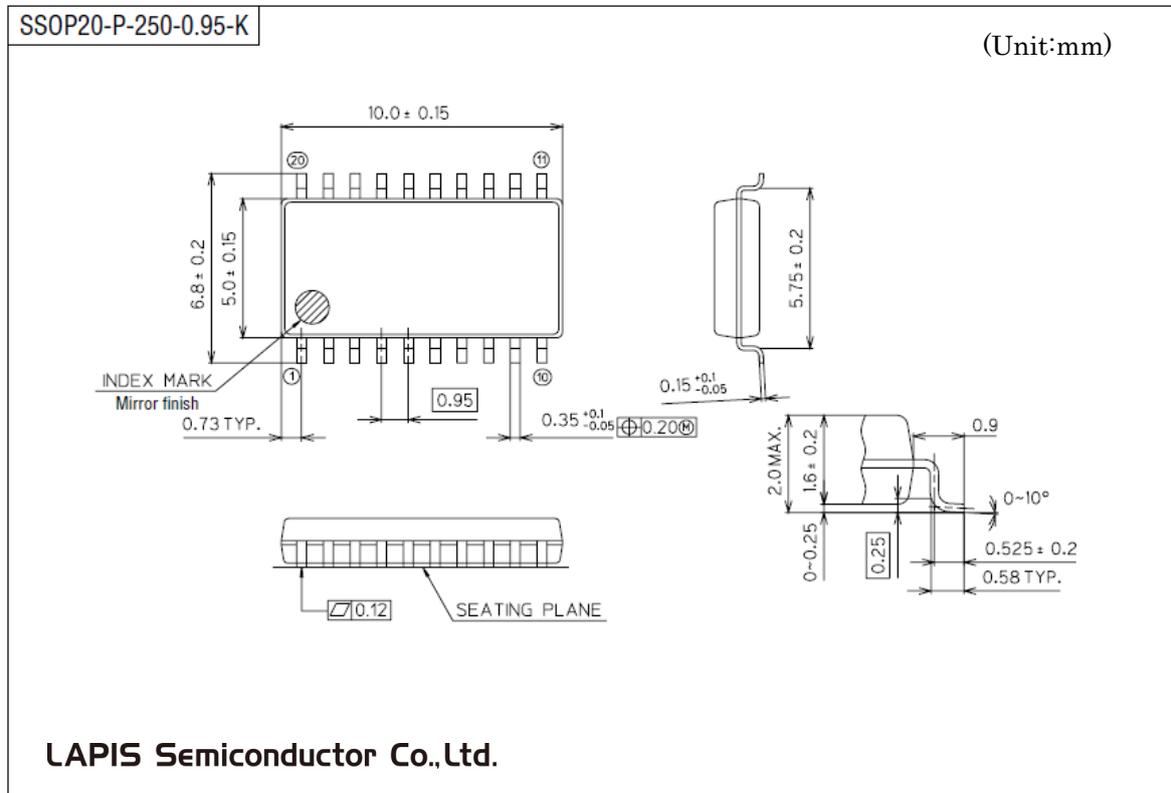
**FREQUENCY CHARACTERISTICS ADJUSTMENT CIRCUIT**



## NOTES ON USE

- To ensure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If the use of IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave sources such as power supply transformers surround the device.
- Keep the voltage on the  $V_{DD}$  pin not lower than  $-0.3$  V even instantaneously to avoid latch-up that may otherwise occur when power is turned on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

## PACKAGE DIMENSIONS



## Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

| Document No.   | Date          | Page             |                 | Description   |
|----------------|---------------|------------------|-----------------|---------------|
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