SM802149

156.25MHz/312.5MHz and 78.125MHz/156.25MHz LVDS Clock Synthesizer

ClockWorks™ Flex

General Description

The SM802149 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution. It is based on a unique patented ClockWorks Flex architecture that provides very low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes eight differential LVDS clocks, four at 156.25MHz and four at 3125MHz, or four at 78.125MHz and four at 156.25MHz.

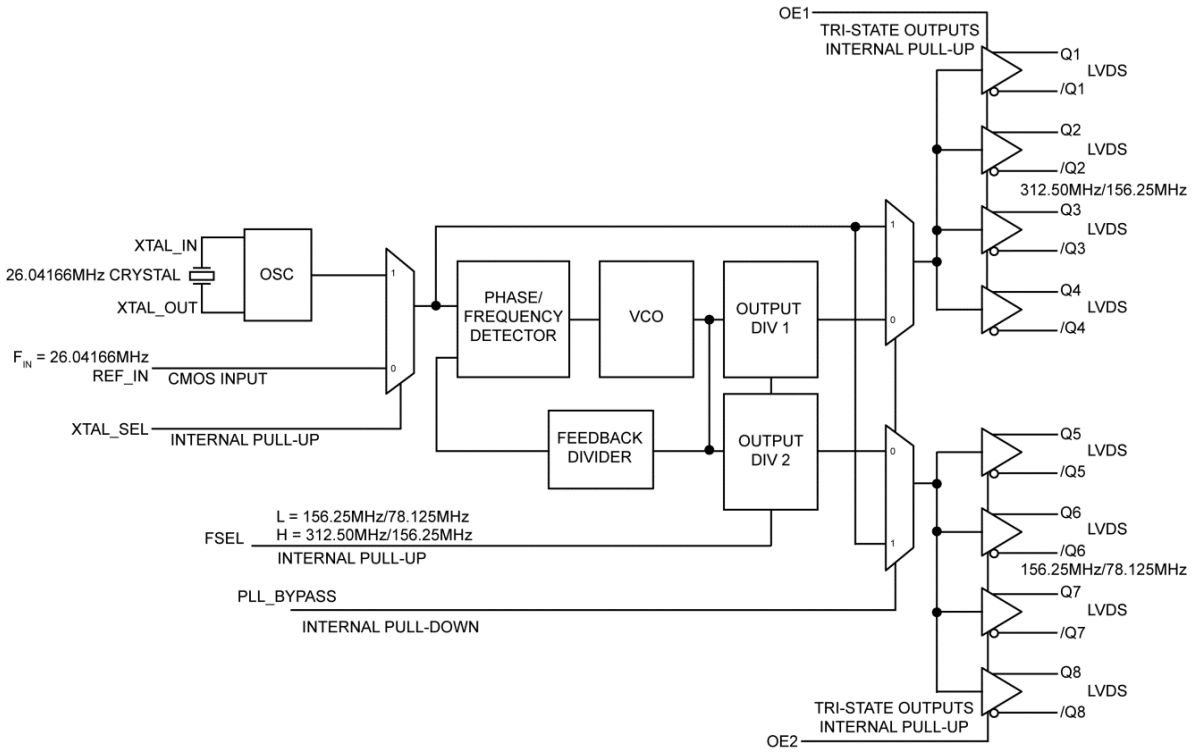
The SM802149 accepts a 26.04166MHz crystal or external LVCMOS input.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- Generates eight differential LVDS clocks: either four at 156.25MHz and four at 312.5MHz, or four at 78.125MHz and four at 156.25MHz
- 2.5V or 3.3V operating range
- Typical phase jitter (1.875MHz to 20MHz): 99fs
- Industrial temperature range
- Green, RoHS, and PFOS compliant
- Available in 44-pin 7mm × 7mm QFN package

Typical Application



ClockWorks is a trademark of Micrel, Inc.

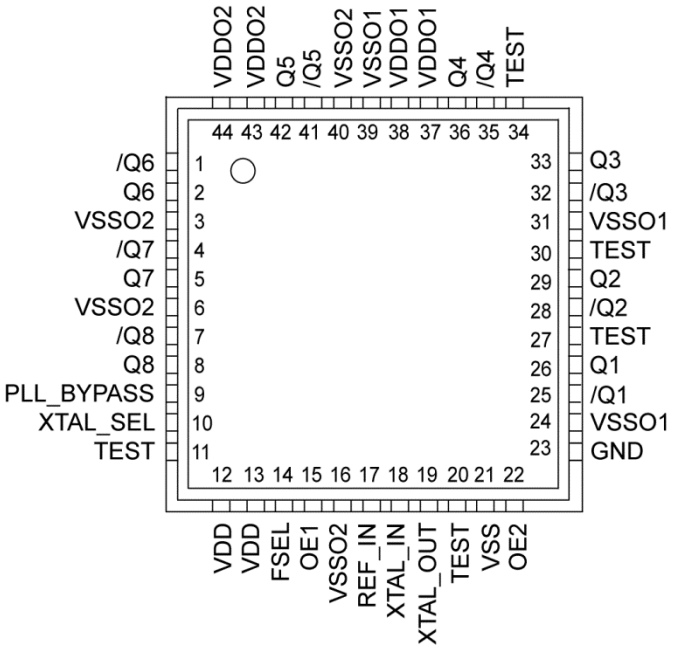
Ordering Information[1]

Part Number	Marking	Shipping	Temperature Range	Package
SM802149UMG	802149	Tray	–40°C to +85°C	44-Pin QFN
SM802149UMGR	802149	Tape and Reel	–40°C to +85°C	44-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



44-Pin QFN
7mmx7mm
(Top View)

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Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
25, 26 28, 29 32, 33 35, 36	/Q1, Q1 /Q2, Q2 /Q3, Q3 /Q4, Q4	O, (DIF)	LVDS	Differential Clock Outputs from Bank 1 312.50MHz/156.25MHz
41, 42 1, 2 4, 5 7, 8	/Q5, Q5 /Q6, Q6 /Q7, Q7 /Q8, Q8	O, (DIF)	LVDS	Differential Clock Outputs from Bank 2 156.25MHz/78.125MHz
31, 37, 38	VDDO1	PWR		Power Supply for the Outputs on Bank 1
43, 44, 16	VDDO2	PWR		Power Supply for the Outputs on Bank 2
24, 39	VSSO1	PWR		Power Supply Ground for the Outputs on Bank 1
3, 6, 40	VSSO2	PWR		Power Supply Ground for the Outputs on Bank 2
23	GND	I, (SE)		This pin is not a Power Supply Ground, but MUST be tied to VSS
10	XTAL_SEL	I, (SE)	LVCMOS	Selects PLL Input Reference Source 0 = REF_IN 1 = XTAL 45kΩ pull-up
11, 20, 27, 30, 34	TEST			Factory Test Pins. Do not connect anything to these pins.
12, 13	VDD	PWR		Core Power Supply
21	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
9	PLL_BYPASS	I, (SE)	LVCMOS	PLL Bypass is a dual-function input. Normal operation selects output source. 0 = Normal PLL operation 1 = Output from crystal oscillator 45kΩ pull-down
18	XTAL_IN	I, (SE)	10pF crystal	Crystal Reference Input. No load caps needed. See Figure 5.
19	XTAL_OUT	O, (SE)	10pF crystal	Crystal Reference Output. No load caps needed. See Figure 5.
17	REF_IN	I, (SE)	LVCMOS	26.04166MHz Reference Clock Input
14	FSEL	I, (SE)	LVCMOS	Frequency Select. 1 = 312.5MHz/156.25 MHz 0 = 156.25MHz/78.125MHz. Internal 45kΩ pull-up
15	OE1	I, (SE)	LVCMOS	Output Enable. Q1–Q4 disables to tri-state. 0 = Disabled 1 = Enabled 45kΩ pull-up
22	OE2	I, (SE)	LVCMOS	Output Enable. Q5–Q8 disables to tri-state. 0 = Disabled 1 = Enabled 45kΩ pull-up

Truth Tables

PLL_BYPASS	XTAL_SEL	OE1	OE2	INPUT	OUTPUT
0		1	1		PLL
1		1	1		XTAL/REF_IN
	0	1	1	REF_IN	
	1	1	1	XTAL	
		0	1		Q1–4 Tri-State
		1	0		Q5–8 Tri-State

FSEL	Output Frequency (MHz)
0	156.25/78.125
1	312.50/156.25

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Absolute Maximum Ratings[2]

Supply Voltage (V_{DD}, V_{DDOX}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD}+0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (Ts) ..... –65°C to +150°C

Operating Ratings[3]

Supply Voltage ($V_{DD,}$ V_{DDOX}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[4]
QFN (θ_{JA})
Still-Air ..... 24°C/W
QFN (ψ_{JB})
Junction to Board ..... 8°C/W

DC Electrical Characteristics[5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%, V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD,}$ $V_{DDO1/2}$	3.3V Operating Voltage	V_{DDO1} = V_{DDO2}	3.135	3.3	3.465	V
	2.5V Operating Voltage	V_{DDO1} = V_{DDO2}	2.375	2.5	2.625	V
		Outputs loaded 156.25MHz		181	235	mA
		Outputs loaded 312.5MHz		216	280	

LVCMOS Input (OE1, OE2, PLL_BYPASS) DC Electrical Characteristics[5]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

REF_IN DC Electrical Characteristics[5]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	–5		5	µA

Notes:

2. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
5. The circuit is designed to meet the AC and DC specifications shown in the above tables after thermal equilibrium has been established.

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF load		Fundamental, Parallel Resonant		
Frequency			26.04166		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			1	5	pF
Correlation Drive Level			10	100	µW

LVDS OUTPUT DC Electrical Characteristics[5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%, V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C.
R_L = 100Ω across Q and /Q.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage	Figure 1, Figure 4	275	350	475	mV
ΔV_{OD}	V_{OD} Magnitude Change				40	mV
V_{OS}	Offset Voltage		1.15	1.25	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics[5, 6]

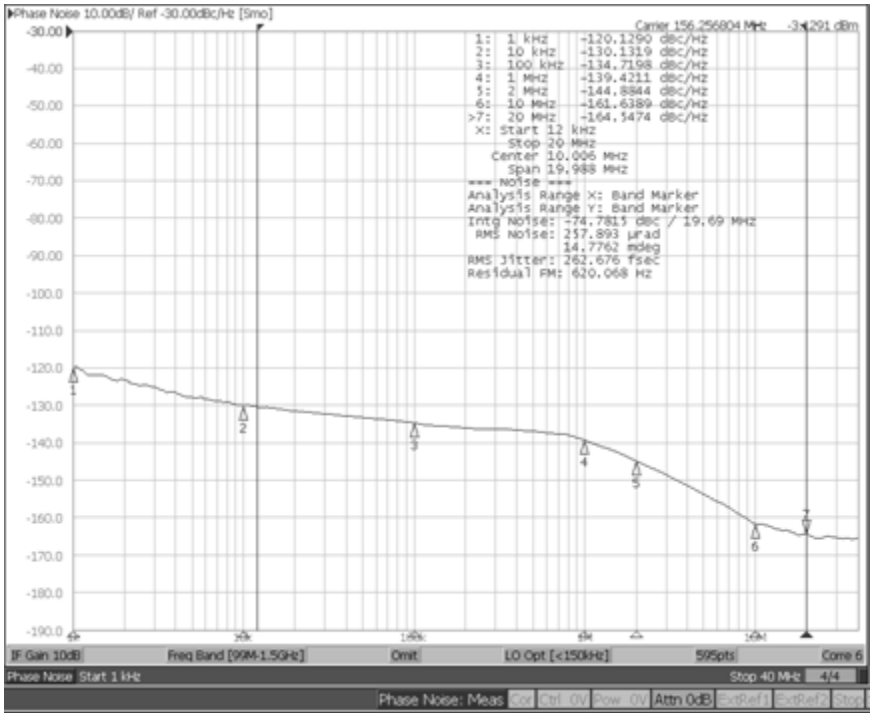
V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%, V_{DD} = 3.3V ±5%, $V_{DDOX1/2}$= 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency 1	FSEL = 1, Q1–Q4		312.5		MHz
	Output Frequency 2	FSEL = 1, Q5–Q8		156.25		MHz
F_{OUT}	Output Frequency 1	FSEL = 0, Q1–Q4		156.25		MHz
	Output Frequency 2	FSEL = 0, Q5–Q8		78.125		MHz
T_R/T_F	Output Rise/Fall Time	20%–80%, Figure 2, Figure 4	100	220	400	ps
T_{SKEW}	Output-to-Output Skew	Within bank. Note 7			45	ps
ODC	Output Duty Cycle	LVDS outputs	48	50	52	%
T_{LOCK}	PLL Lock Time				20	ms
	RMS Phase Jitter[8] (Output = 156.25MHz)	Integration range: 12kHz–20MHz		260		fs
		Integration range: 1.875MHZ–20MHz		105		fs
	RMS Phase Jitter[8] (Output = 312.5MHz)	Integration range: 12kHz–20MHz		250		fs
		Integration range: 1.875MHz–20MHz		99		fs

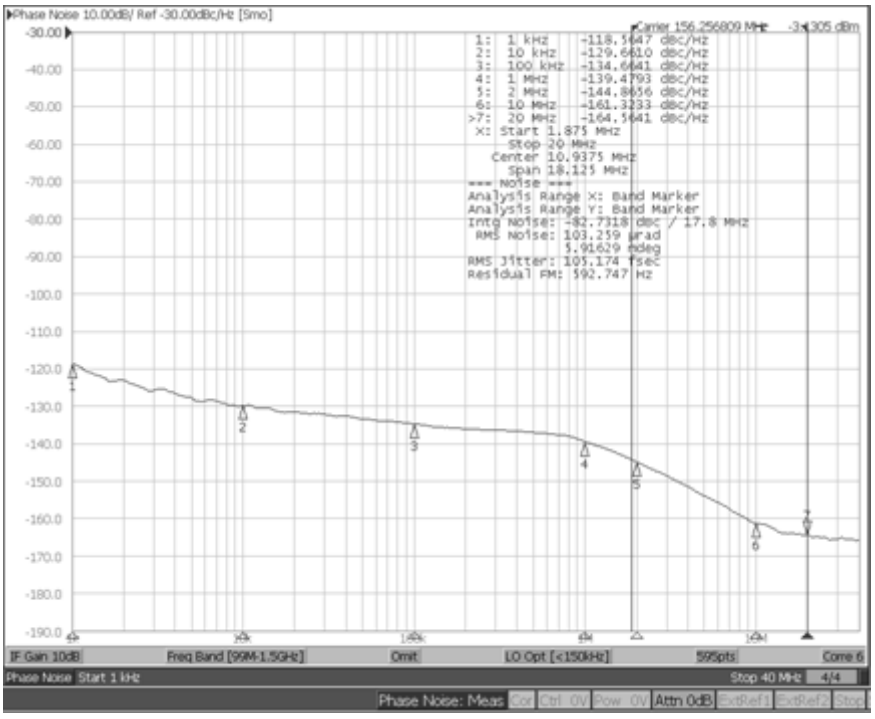
Notes:

6. All phase noise measurements were taken with an Agilent 5052B phase noise system.
7. Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.
8. Measured using a 26.04166 MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Phase Noise Plots



156.25MHz LVDS Integrated Jitter 12kHz–20MHz = 262fs



156.25MHz LVDS Integrated Jitter 1.875MHz–20MHz = 105fs

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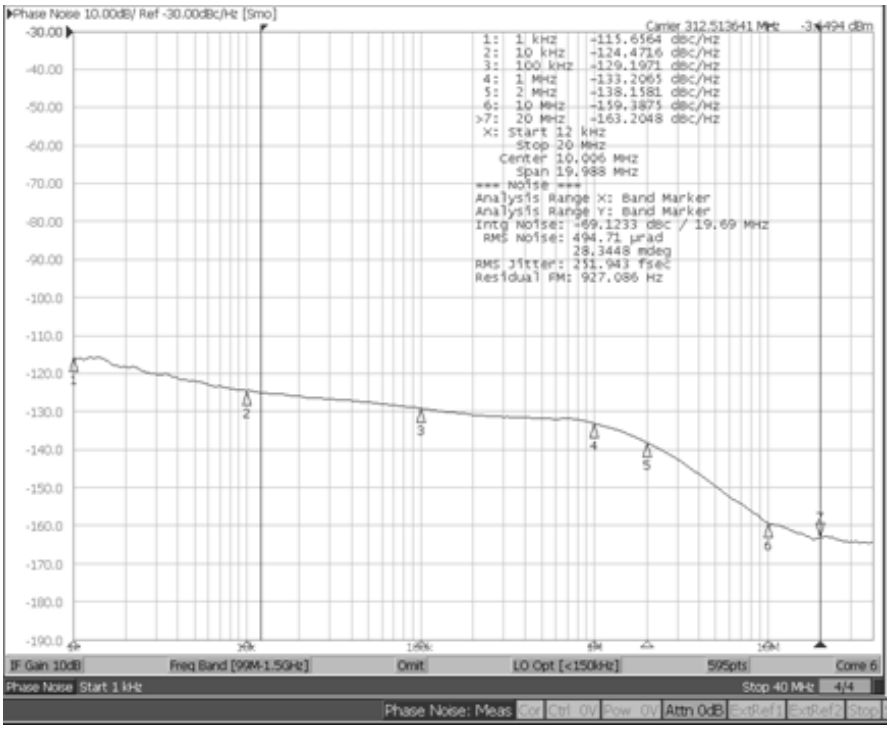
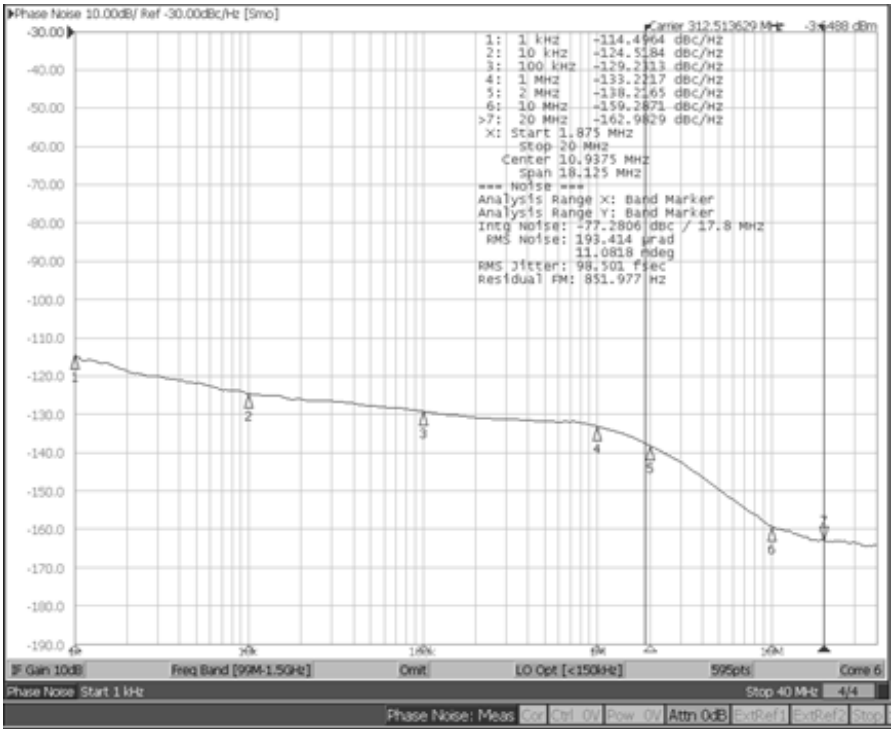
Phase Noise Plots (Continued)



312.5MHz LVDS Integrated Jitter 12kHz–20MHz = 252fs



312.5MHz LVDS Integrated Jitter 1.875MHz–20MHz = 99fs

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Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz Crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

Contact Micrel's HBW applications group if you need assistance to select a suitable crystal for your application at hbwhelp@micrel.com

LVDS Outputs

Terminate LVDS outputs with 100Ω across Q and /Q. For best performance, load all outputs. Outputs can be DC or AC-coupled.

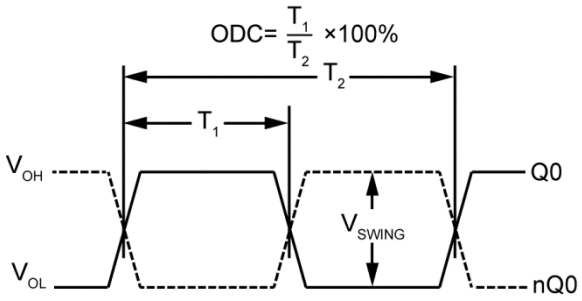


Figure 1. Duty Cycle Timing

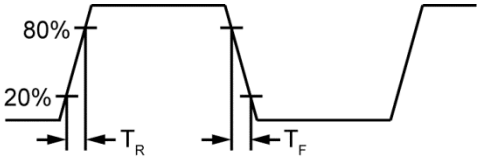


Figure 2. All Outputs Rise/Fall Time

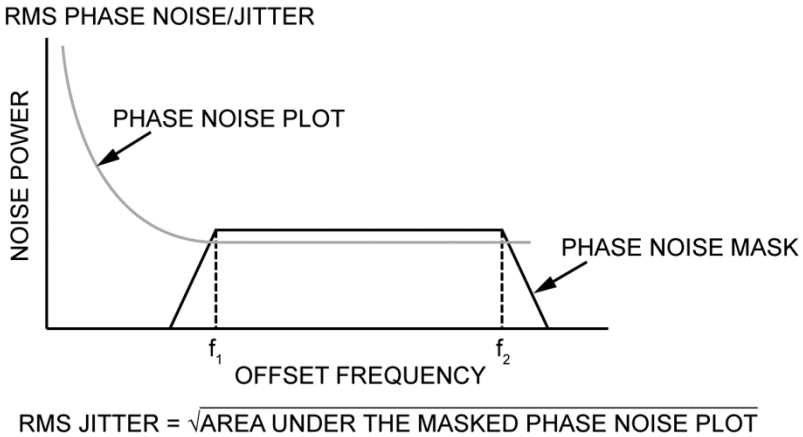


Figure 3. RMS Phase/Noise/Jitter

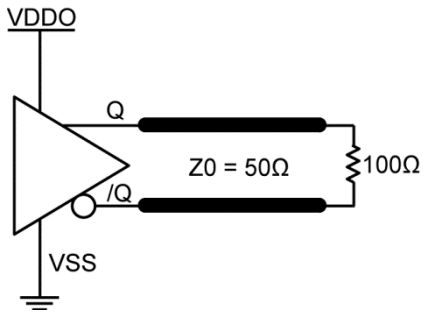


Figure 4. LVDS Output Load

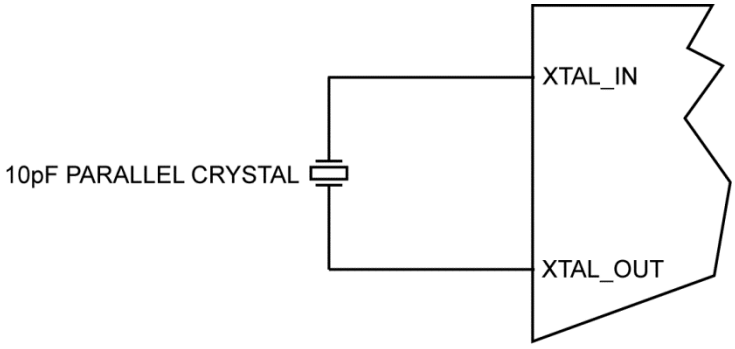
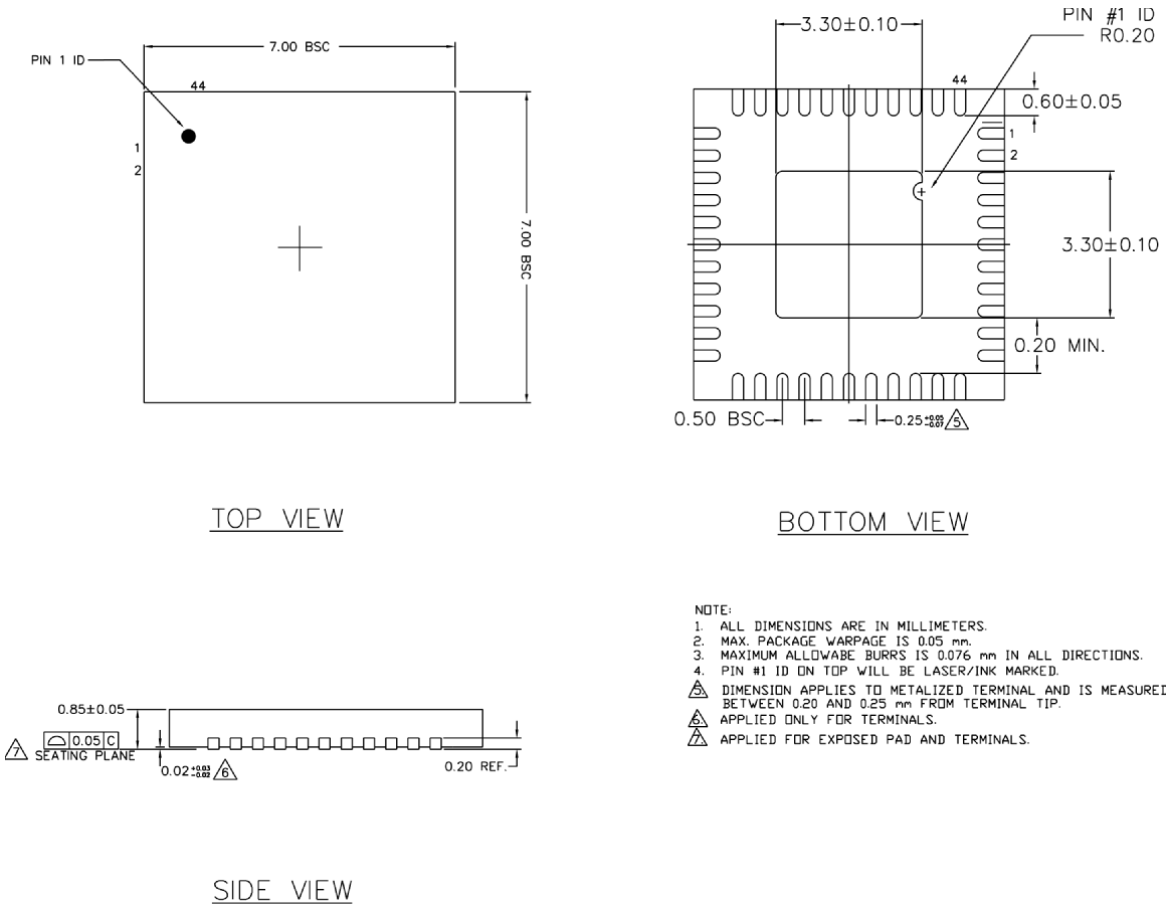


Figure 5. Crystal Input Interface

Package Information[9]



44-pin 7mm × 7mm QFN package

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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