CY3280-SmartSense™ CapSense® Auto-Tuning Kit Guide

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Contents

1. Introduction

1.1 Overview

Thank you for your interest in the CY3280-SmartSense™ CapSense® Auto-Tuning Kit. This kit is designed to showcase the abilities of the patented SmartSense algorithm, which does automatic tuning of capacitive sensor designs over the conventional manual-tuning approach.

1.2 Kit Contents

- CY3280-SmartSense Kit
- Two AAA batteries
- Overlay - Clear acrylic overlays with matt finish on one side in 1 mm, 2 mm, 3 mm thickness. 2 mm thick overlay is stuck to the board
- Axial capacitors 10 pF, 22 pF, 33 pF, 68 pF
- Printed documentation
- Quick Start Guide
  - CY3280-SmartSense schematic

1.3 Installation

Everything you need to use the CY3280-SmartSense kit is included; install the software to load and run the example projects on the board.

1.3.1 Before You Begin

All Cypress software installations require administrator privileges, but this is not required to run the installed software.

- Shut down any Cypress software that is currently running.
- Disconnect any ICE Cube or MiniProg devices from your computer.

1.3.2 Prerequisites

PSoC Designer™ uses the Microsoft .NET Framework, Adobe Acrobat Reader, and a Windows Installer. If .NET Framework and Windows Installer are not on your computer, the installation automatically installs it. If you do not have Adobe Acrobat Reader, download and install it from the Adobe website.

Download the kit specific software CD ISO from http://www.cypress.com/go/CY3280-SmartSense.

1.3.3 PSoC Designer Installation Procedure

1. If PSoC Designer 5.0 or earlier is currently installed, uninstall it.
   Click **Start** > **Control Panel** > **Add or Remove Programs**
2. Insert the software CD; using the menu, select **Install PSoC Designer 5.1**.
   Note Create the software CD by burning the downloaded CD ISO.

After installation, user guides and key documents are available in the \Documentation subdirectory of the PSoC Designer installation directory.

The default location is: `C:\Program Files\Cypress\CY3280-SmartSense\1.0\CY3280-SmartSense\Documentation`.

1.3.4 Factory Default Configuration

When shipped, the CY3280-SmartSense kit is loaded to run the SmartSense example project. The LED is expected to toggle when the corresponding button is touched.

For a demonstration of the self-tuning capability of SmartSense algorithm, refer 3.2.5 Self Tuning Demonstration on page 22.

1.4 Reference Documents

1.4.1 Application Notes

- AN57316 - CapSense SmartSense Basics
- AN2394 - CapSense Best Practices
- AN47456 - CapSense Buttons with CSD
- AN2292 - Capacitive Sensing - Layout Guidelines for PSoC CapSense

1.4.2 Example Projects

- CapSense Buttons using SmartSense CSDAUTO on CY8C20xx6A
- CapSense Buttons and Slider using SmartSense CSDAUTO on CY8C20xx66A
- CapSense Matrix Buttons using SmartSense CSDAUTO on CY8C20xx66A

1.4.3 Data Sheets

- CY8C20x36A/46A/66A/96A

1.4.4 Technical Reference Manual

- PSoC® CY8C20x66, CY8C20x66A, CY8C20x46/96, CY8C20x46A/96A, CY8C20x36, CY8C20x36A

1.5 Document Revision History

Table 1-1. Revision History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	11/25/10	KPOL	New kit guide.
*A	01/04/11	BVI	Fixed hyperlink in section 2.1.4. Modified the installation location in section 1.3.3

1.6 Documentation Conventions

Table 1-2. Document Conventions for Guides

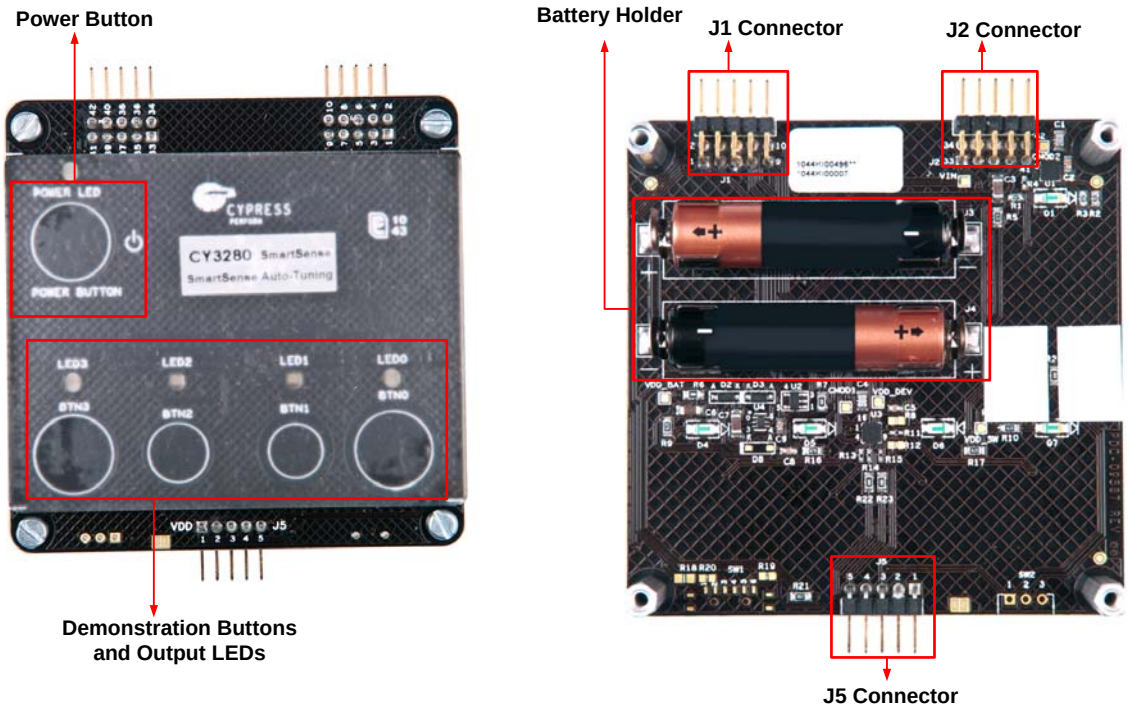
Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes Cautions or unique functionality of the product.

2. Kit Operation

The CY3280-SmartSense kit is designed to demonstrate four CapSense buttons and a CapSense based power button. Figure 2-1 illustrates these buttons: demonstration buttons (BTN0 to BTN3) and a CapSense power button (POWER BUTTON). In its default configuration, the kit is powered from two AAA on-board batteries, which are placed below the kit in the battery holder. The board has three connectors. Connector J5 is used for ISSP programming and to demonstrate self tuning capability of SmartSense algorithm. Connectors J1 and J2 are used to expand controller I/O pins.

Touch the Power Button first and ensure the power LED is turned on. Each CapSense button is mapped to an LED (LED 0 to LED3) such that activation of each button can be verified visually by monitoring the LED status.

Figure 2-1. Top and Bottom View of Kit



2.1 CY3280-SmartSense Kit Board

2.1.1 Board Features

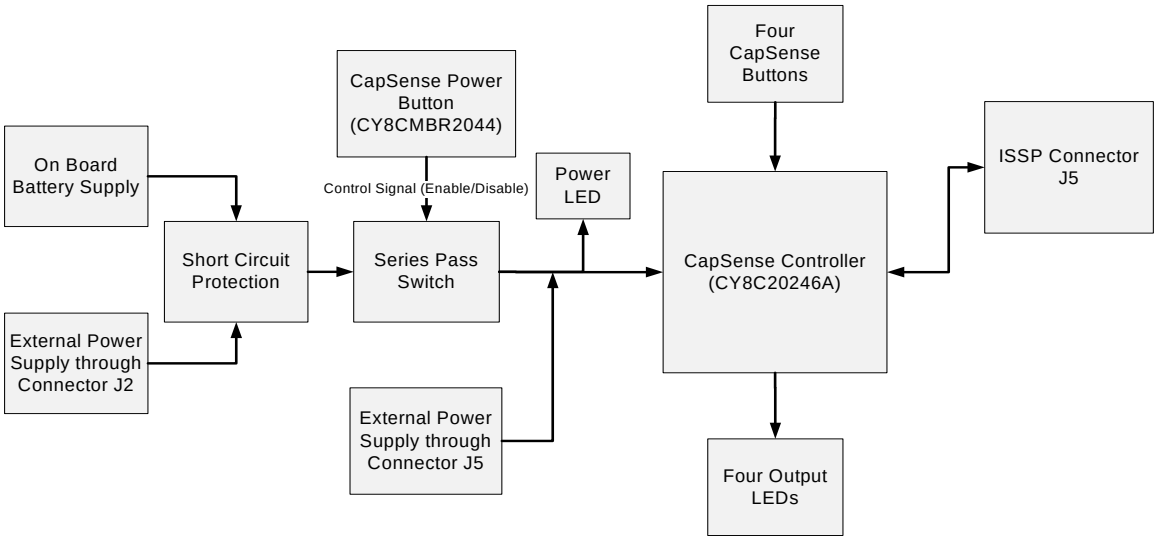
- Four CapSense buttons of different dimensions
- Four LEDs connected to general purpose output pins
- CapSense based power button and power LED
- Operates from external power supply and battery
- Expansion slots, allowing I/O to expand to external boards

2.1.2 System Block Diagram

Figure 2-2 shows the block diagram of the CY3280-SmartSense kit.

The kit can be powered from three different sources. Internal supply from on-board battery and external supply through J2 connector are gated using a series pass switch controlled by the CapSense based power button. Protection diodes are placed to avoid accidental short between the two power sources. External supply through J5 connector is directly fed to CapSense controller. Four CapSense buttons and LEDs are connected to the CapSense controller and are used for demonstration purpose. Unused I/Os from CapSense controller are routed to expansion headers J1 and J2 for debugging and development purpose.

Figure 2-2. Block Diagram of CY3280-SmartSense kit



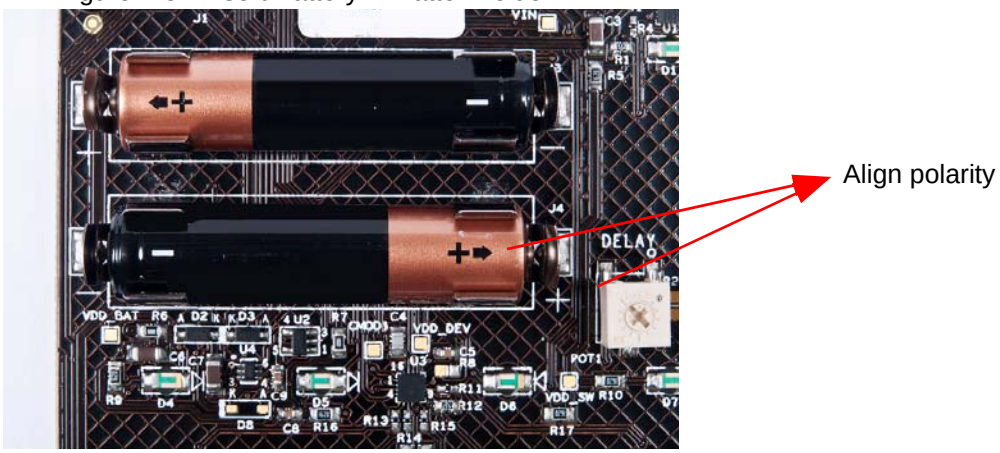
2.1.3 Power Sources

The board supports three power sources:

- Internal supply (supplied AAA batteries to be placed in the battery holder)
- External supply (pin#41, Header J2)
- External supply (pin#1, Header J5)

Note To power the kit, at least one of the above sources should be active. The first two sources are gated to capacitive touch controller by the Power button. The CapSense controller is powered 200 mV less than what is supplied to the board due to voltage drop across the power button switch circuitry. External supply should be greater than 2.0 V and less than 3.8 V to get 1.71 V to 3.6 V supply on the CapSense controller.

Figure 2-3. Insert Battery in Batter Holder



2.1.4 Controller Pin Assignment

Pin assignment of the CapSense controller is shown in the following table. To learn how to assign pins for your design, refer to the CY8C20246A data sheet.

Type	Pin	Description
BTN0	P1[3]	CapSense Button 0
BTN1	P1[1]	CapSense Button 1
BTN2	P1[0]	CapSense Button 2
BTN3	P1[4]	CapSense Button 3
LED0	P2[3]	Active Low LED 0
LED1	P2[5]	Active Low LED 1
LED2	P0[1]	Active Low LED 2
LED3	P0[7]	Active Low LED 3
CMOD	P0[3]	CSD Modulation Capacitor
ISSP-SDA	P1[0]	ISSP - Data Line
ISSP-SCL	P1[1]	ISSP - Clock Line

2.1.5 Connector Details

Table 2-1. CY3280-SmartSense Kit Connector Details

ISSP Header	
Connector J5 (ISSP Header)	
J5 - 1	VDD (External)
J5 - 2	GND
J5 - 3	XRES
J5 - 4	P1[1] (ISSP SCL)
J5 - 5	P1[0] (ISSP SDA)
Expansion Connector J1	
J1 - 1	P0[4]
J1 - 2	XRES
J1 - 3	P1[5]
J1 - 4	P1[7]
J1 - 5	GND
J1 - 6	GND
J1 - 7	P2[3]
J1 - 8	P2[5]
J1 - 9	P0[1]
J1 - 10	P0[7]
Expansion Connector J2	
J2-33	P1[2]
J2-34	NC
J2-35	GND
J2-36	GND
J2-37	NC
J2-38	NC
J2-39	GND
J2-40	GND
J2-41	VDD (External – Gated by ‘POWER BUTTON’)
J2-42	NC

3. Load CapSense Example Projects

This section walks you through the high level design process to open, build, program, and run example projects using this kit. To access the example projects, go to the following location: `C:\Program Files\Cypress\CY3280-SmartSense\1.0\CY3280-SmartSense\Firmware`.

Before beginning, follow each of these steps to make certain that your software and hardware environments are properly configured and ready for these projects:

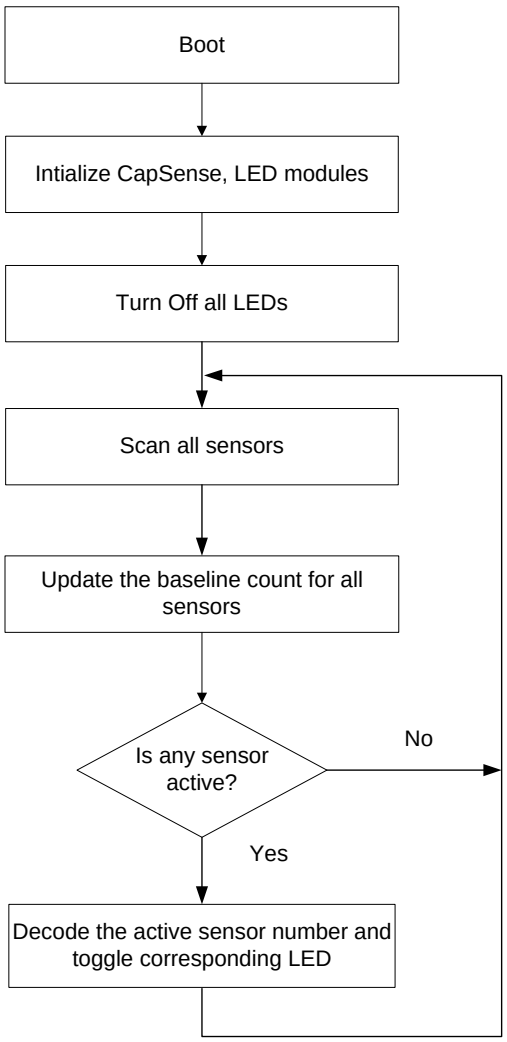
1. Install PSoC Designer following the steps in 1.3.3 PSoC Designer Installation Procedure on page 6.
2. Connect the MiniProg3 into your PC using mini USB connector. You can purchase the programmer from http://www.cypress.com/?rID=38154.
3. Insert the MiniProg3 to ISSP header J5 of the kit as shown in the following figure.
4. Close any open PSoC Designer applications and projects.

Figure 3-1. MiniProg3 Connected to Kit

3.1 CapSense Project: CSD + Manual Tuning

This section outlines the conventional method of tuning a project - CSD with manual tuning. The example project demonstrates four CapSense buttons controlled by the CSD user module to detect the button press. Any button press detected is indicated by toggling the corresponding LED. Figure 3-2 illustrates the code flow.

Figure 3-2. Conventional Method Flowchart

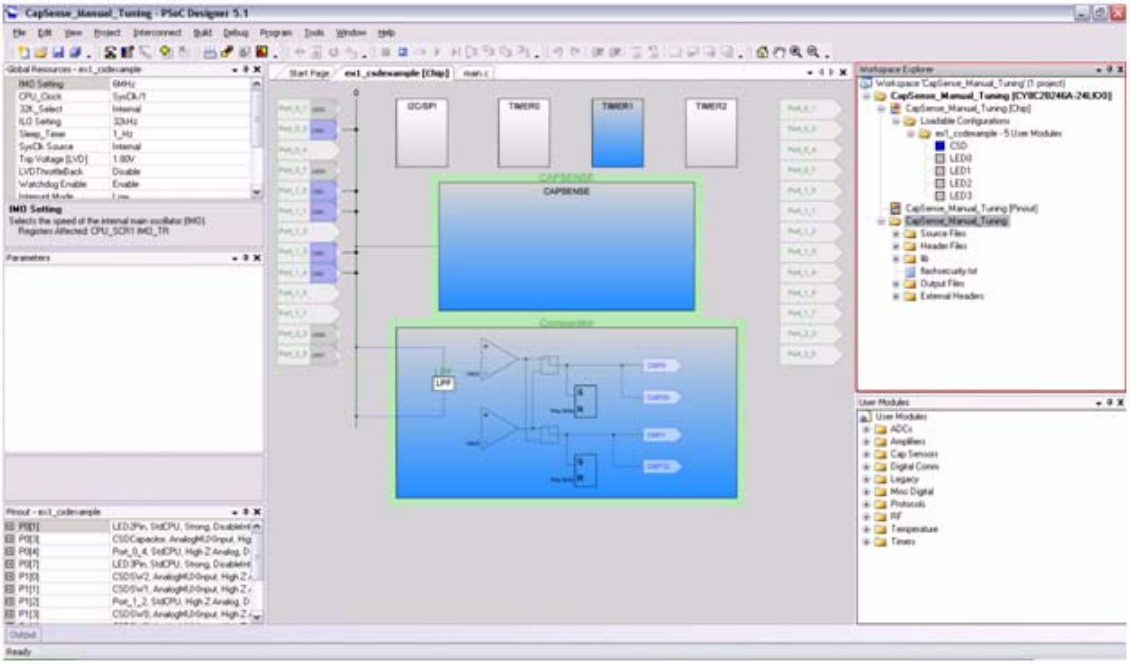


3.1.1 Load Project

1. Open PSoC Designer
2. Click **File** > **Open Project/Workspace**
3. Locate the project directory
4. Open the **CapSense_Manual_Tuning** folder
5. Double-click *CapSense_Manual_Tuning.app*

The project opens in the chip editor view. All the project files are in workspace explorer.

Figure 3-3. Chip Editor View



3.1.2 Build Project

To build a project, select **Build** > **Generate/Build**.

PSoC Designer builds the project and displays comments in the Output window. When you see the message that the project is built with 0 errors and 0 warnings, you are ready to program the device.

Figure 3-4. Build Project

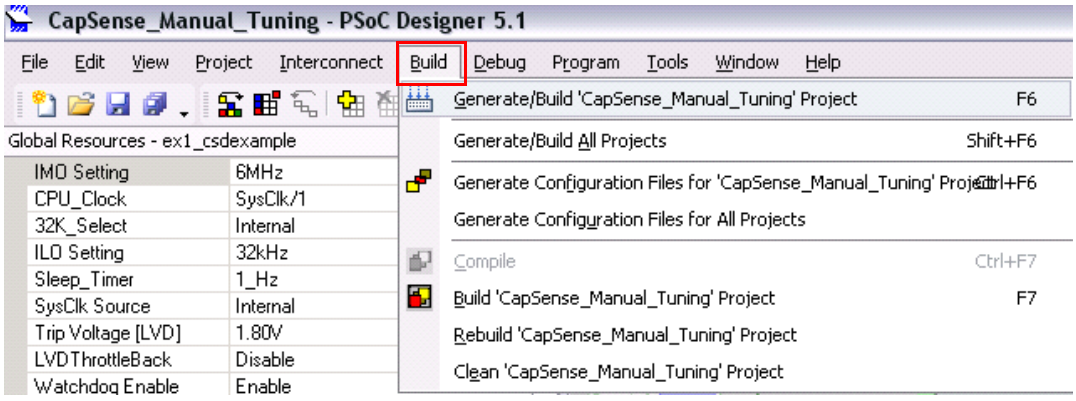
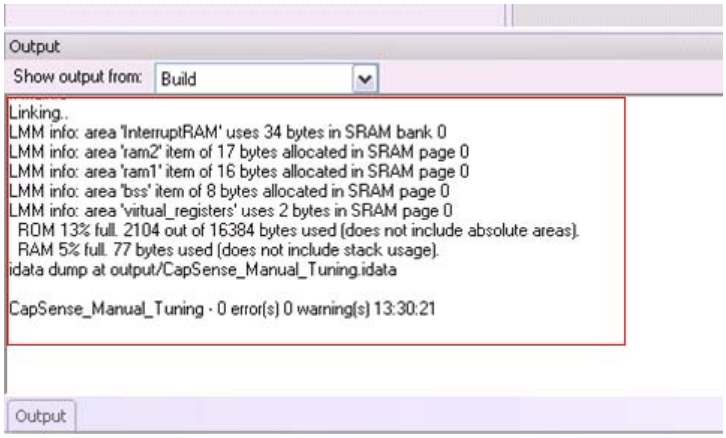


Figure 3-5. Output Window



3.1.3 Program Project

1. Open **Program Part** in PSoC Designer by selecting **Program** > **Program Part**
2. In the **Program Part** window
   a. Select **MiniProg3** in the **PortSelection** box
   b. Set **Acquire Mode** to **Power Cycle**. If the board is already powered from AAA batteries or from external supply through J2, set **Acquire Mode** to **Reset**
   c. Set **Verification** to **ON**. This ensures that downloaded checksum matches actual checksum
   d. Set **Power Settings** to **5V**
   e. Click program arrow to program the device
3. Wait until programming is complete
4. Disconnect MiniProg3 from kit

3.1.4 Run Project

Power the board using any one of the sources listed in 2.1.3 Power Sources on page 11. Touch a CapSense button on the board to see the corresponding LEDs toggle, as shown in . Figure 3-6.

Figure 3-6. Toggle Feature Test Sequence

1. Touch a button; LED turns on

2. Release the button; LED remains on

3. Touch the same button again; LED turns off

4. Release the button; LED remains off

5. Touch the same button again; LED turns on

6. Release the button; LED remains on

3.1.5 Manual Tuning Limitations Demonstration

1. Power the board using one of the sources listed in 2.1.3 Power Sources on page 11
2. Touch **BTN2**; the corresponding LED2 toggles
3. Connect the supplied axial capacitor of 10 pF value between J5.5 and J5.2 (this adds to the parasitic capacitance of BTN2); see Figure 3-7
4. Toggle the board power
5. Touch **BTN2**; the BTN2-LED2 link is broken. This failure occurs due to manual tuning, see Figure 3-8
6. Repeat step 2, 3, and 4 with 22 pF, 33 pF, and 68 pF axial capacitors

This experiment demonstrates that sensors need to be tuned to work every time its parasitic capacitor value changes.

Figure 3-7. Connect Axial Capacitor to Connector J5 (picture to be updated)

Figure 3-8. Broken Link in BTN2-LED2

1. Touch BTN2; LED2 remains off

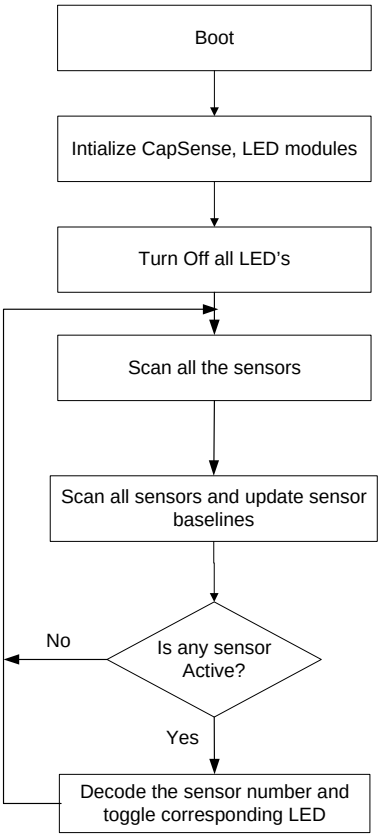
2. Release BTN2; LED2 continues to remain off

3. Touch BTN2 again; LED2 remains off

3.2 CapSense Project: SmartSense + Auto Tuning

This section outlines the SmartSense method of tuning a project - SmartSense with auto tuning. The example project demonstrates four CapSense buttons controlled by SmartSense user module to detect the button press. Any button press detected is indicated by toggling the corresponding LED. Figure 3-9 illustrates the code flow.

Figure 3-9. SmartSense Method Flowchart

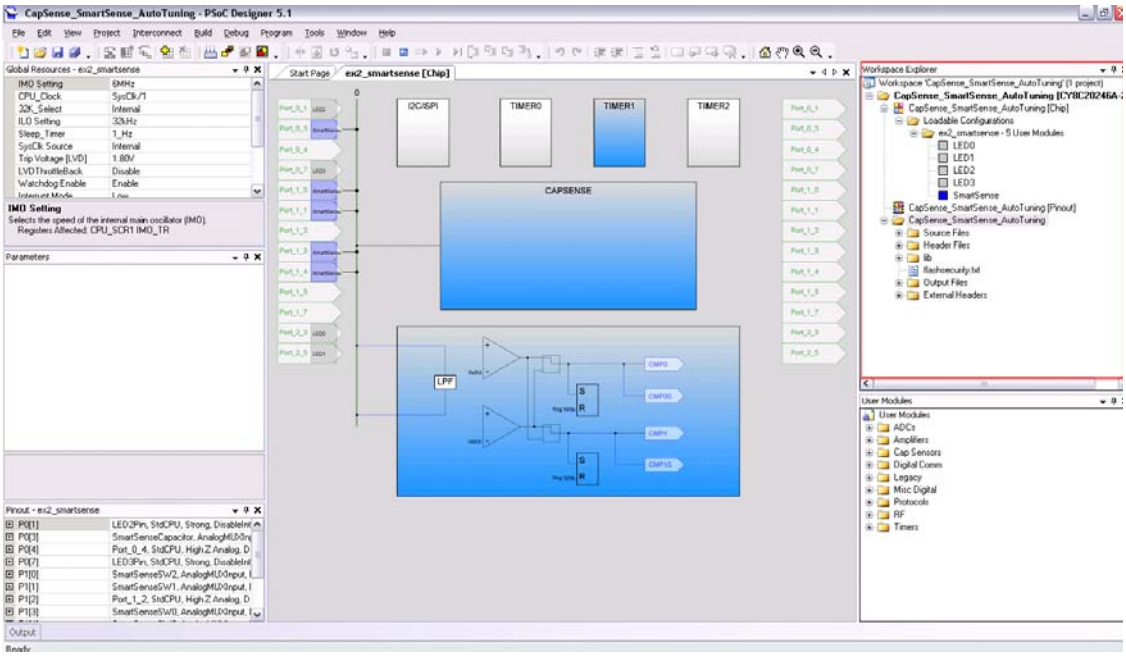


3.2.1 Load Project

1. Open PSoC Designer
2. Click **File** > **Open Project/Workspace**
3. Locate the project directory
4. Open the **CapSense_SmartSense_AutoTuning** folder
5. Double-click *CapSense_SmartSense_AutoTuning.app*

The project opens in the Chip Editor view. All the project files are in workspace explorer.

Figure 3-10. Chip Editor View



3.2.2 Build Project

To build a project, select **Build** > **Generate/Build.**

PSoC Designer builds the project and displays comments in the Output window. When you see the message that the project built with 0 errors and 0 warnings, you are ready to program the device.

Figure 3-11. Build Project

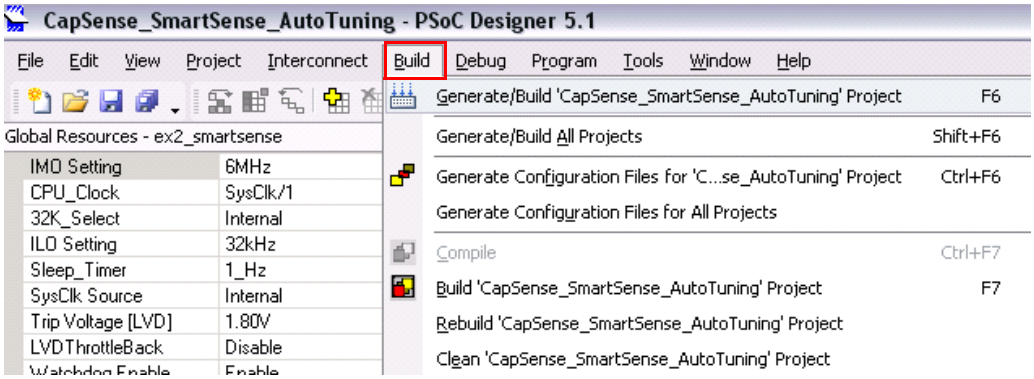
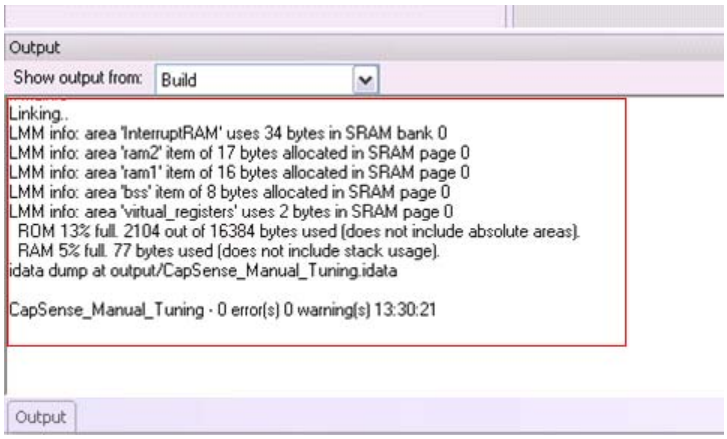


Figure 3-12. Output Window



3.2.3 Program Project

1. Open **Program Part** in PSoC Designer by selecting **Program** > **Program Part**
2. In the **Program Part** window
   a. Select **MiniProg3** in the **PortSelection** box
   b. Set **Acquire Mode** to **Power Cycle**. If the board is already powered from AAA batteries or from external supply through J2, set **Acquire Mode** to **Reset**
   c. Set **Verification** to **ON**. This ensures that downloaded checksum matches actual checksum
   d. Set **Power Settings** to **5V**
   e. Click program arrow to program the device
3. Wait until programming is completed to continue
4. Disconnect MiniProg3 from the kit

3.2.4 Run Project

Power the board using one of the sources listed in 2.1.3 Power Sources on page 11. Touch a CapSense button on the board to see the corresponding LEDs toggle. See Figure 3-6.

3.2.5 Self Tuning Demonstration

1. Power the board using one of the sources listed in 2.1.3 Power Sources on page 11
2. Touch **BTN2**; the corresponding LED2 toggles
3. Connect the supplied axial capacitor of value 10 pF between J5.5 and J5.2 (this adds to the parasitic capacitance of BTN2); see Figure 3-7
4. Toggle the board power
5. Touch **BTN2**; LED2 toggles again, as shown in Figure 3-6
6. Repeat step 2, 3, and 4 with 22 pF, 33 pF, and 68 pF axial capacitors

This demonstration shows that irrespective of variation in button parasitic capacitance, system works the way it is indented to (LED toggles when the corresponding button is touched) due to the self tuning capability of the SmartSense algorithm.

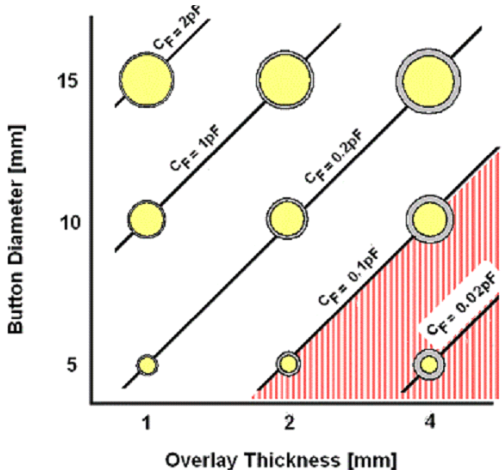
Note SmartSense user module works with sensor parasitic capacitance (Cp) as high as 45 pF. Sensors with Cp greater than 45 pF are not guaranteed to work.

3.2.6 Tuning For Overlay

1. Stick overlay of required thickness on top of CapSense buttons
2. Follow steps in 3.2.1 Load Project on page 20 to load the SmartSense example project
3. Decide the required SmartSense 'Sensor Sensitivity' parameter value

   Sensor sensitivity sets the capacitance signal change (sensor response) in pF needed to activate a button sensor. The available settings are 0.1, 0.2, 0.3, and 0.4 pF. The default setting is 0.1 pF. Figure 3-13 shows the relationship between the button size, overlay thickness (acrylic plastic), and sensor response (C_F), and can be used as a guide to set sensor sensitivity. The sensor sensitivity should always be set at or below the sensor response indicated in Figure 3-13. This ensures robust operation. Note that the area shaded in red must be avoided, because the sensor response is below the minimum 0.1 pF that can be detected by SmartSense.

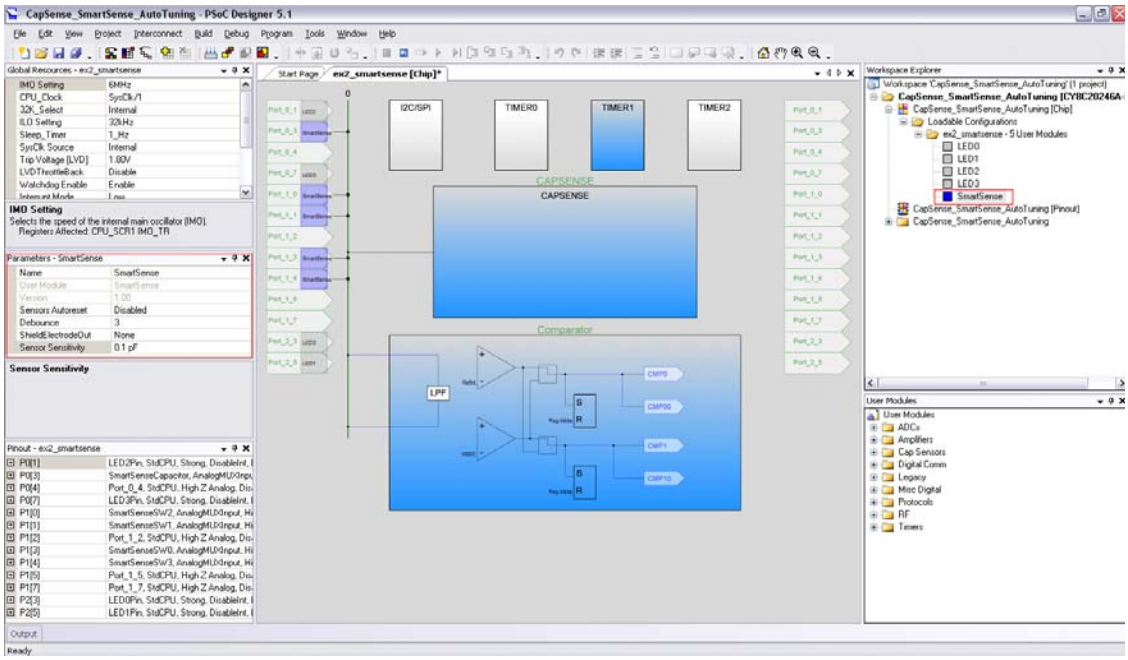
Figure 3-13. Relationship between Button Size, Overlay Thickness, and Sensor Response in pF



Note For overlay materials other than acrylic, X-axis (overlay thickness) of the figure should be scaled accordingly. Scaling factor is the ratio of dielectric constant of 'Overlay Material' to that of 'Acrylic'.

4. After deciding 'Sensor Sensitivity' value, go to the SmartSense user module Property window and associate the value with the Sensor Sensitivity parameter. By default, SmartSense user module associates a value of 0.1 pF with this parameter.

Figure 3-14. SmartSense Property Window

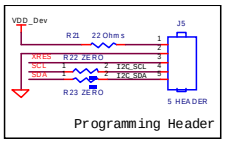


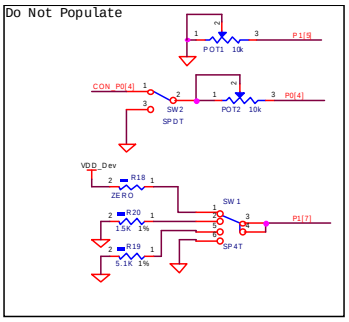
5. Follow steps in 3.2.2 Build Project, 3.2.3 Program Project, and 3.2.4 Run Project to build, program, and run the modified example project.

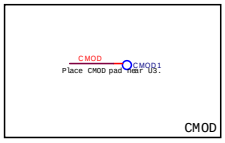
A. Appendix

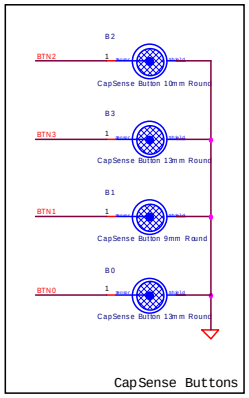
A.1 Schematics

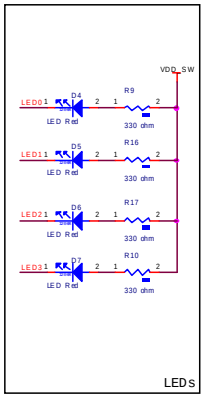
A.1.1 CapSense Controller, Buttons, I/O Interfaces

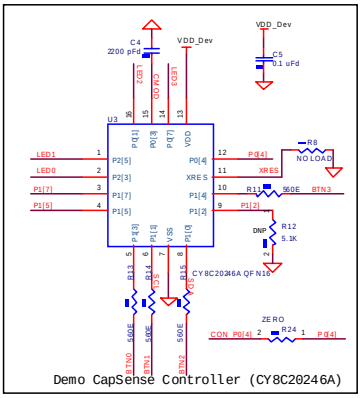


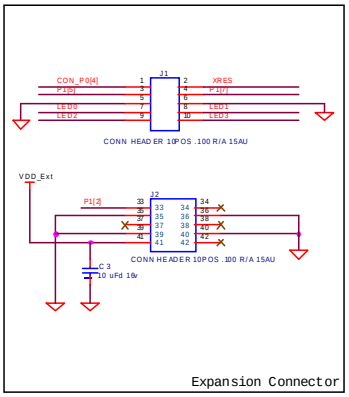




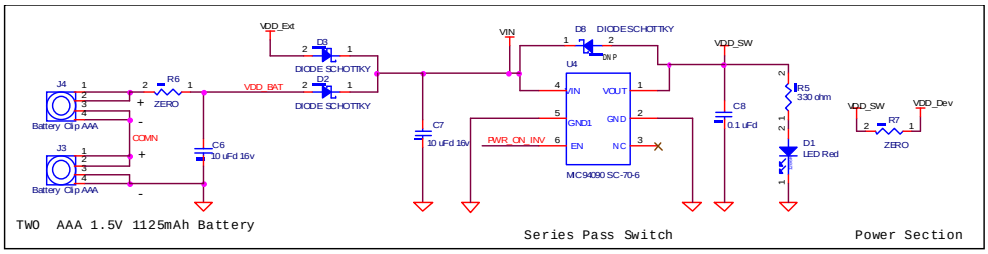


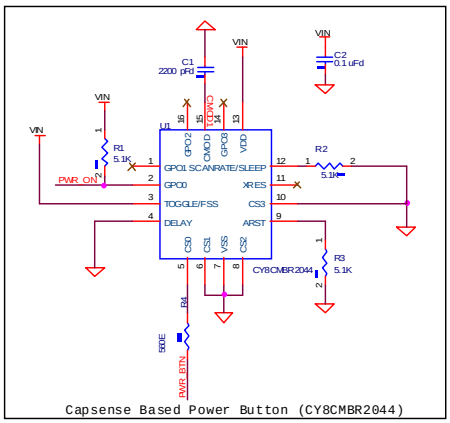


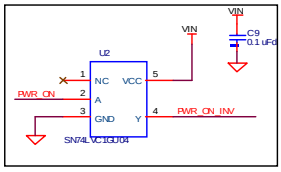


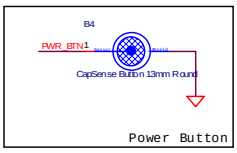


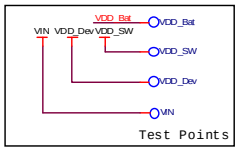
A.1.2 Power Supply

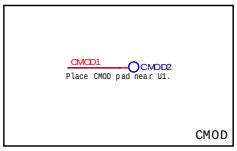










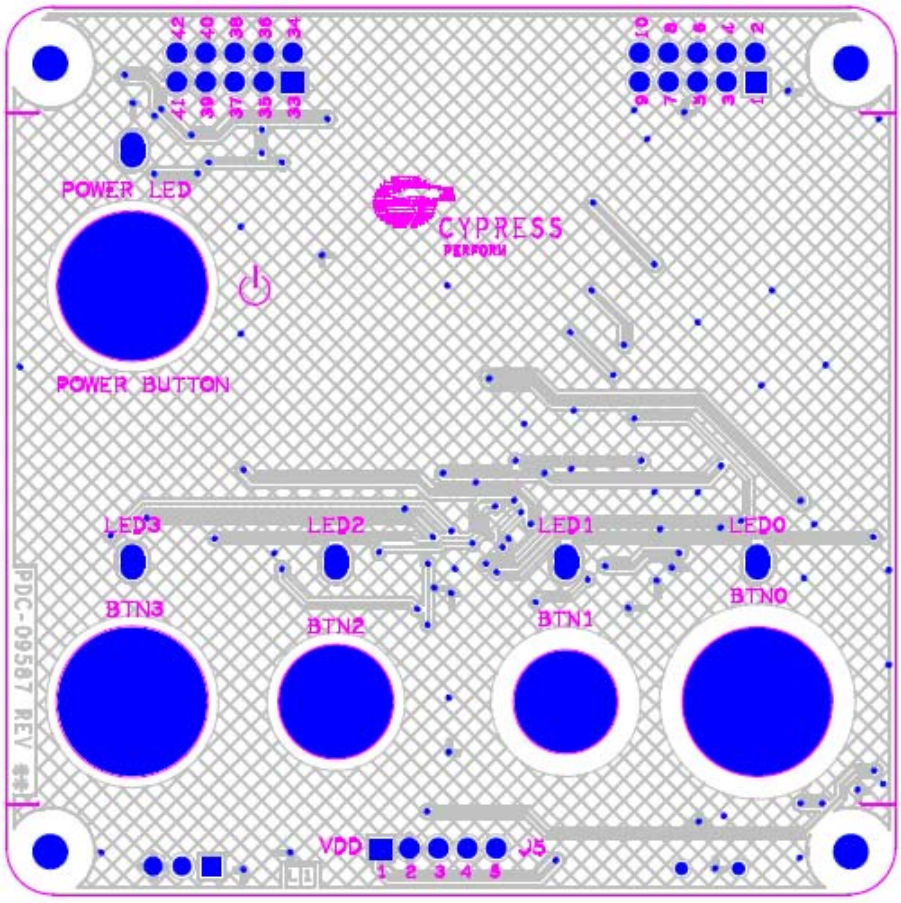


In the schematic:

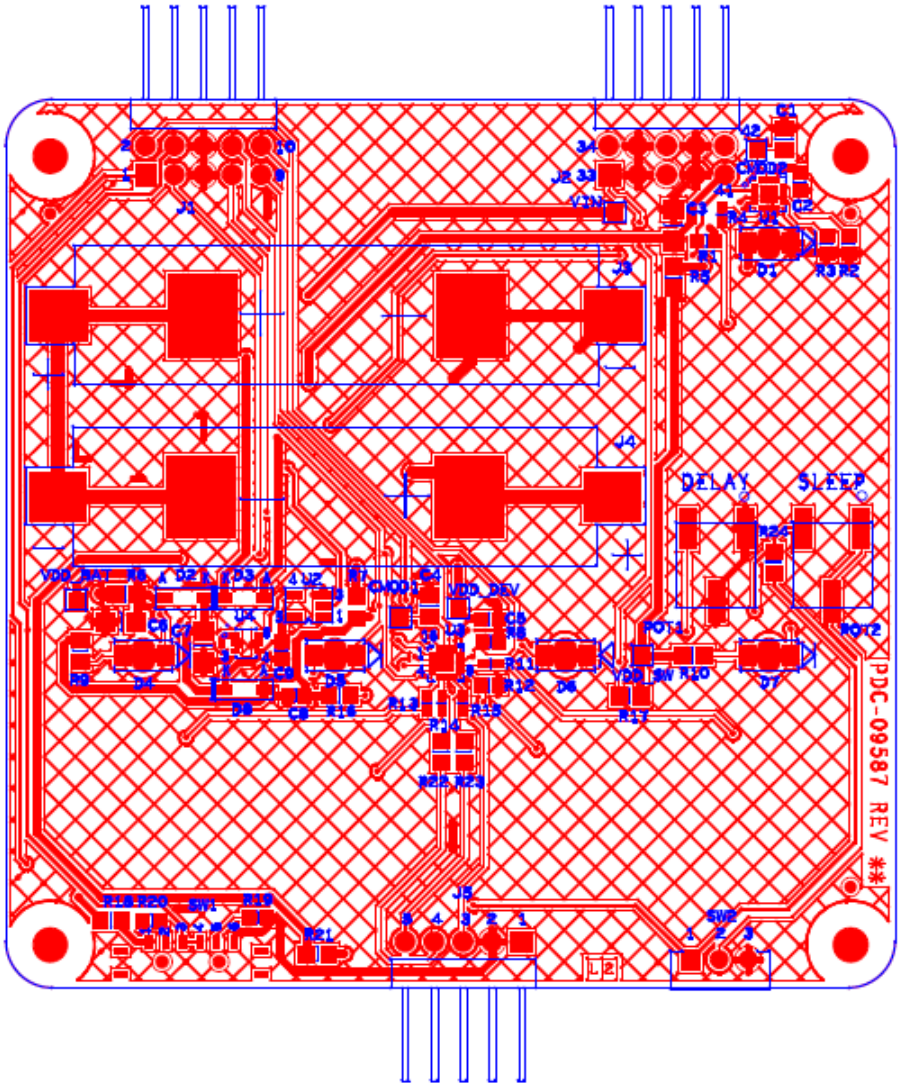
- CapSense controller CY8C20246A is used to detect finger touch on sensors BTN0-BTN3. It drives active low LEDs (LED0-LED3) based on detected touch on sensors.
- CY8C20246A controller can be powered either from on-board AAA batteries or from external sources (VDD_EXT / VDD_DEV).
- Supply from battery and VDD_EXT are gated by the Power button, but VDD_DEV is not.
- CapSense controller CY8CMBR2044 is used to detect finger touch on the Power button. It turns on/off series pass switch based on detected status. CY8CMBR2044 is configured to operate for a period of 1 year on battery power.
- Power LED turns on when any of the three power sources are activated.
- Connectors J1 and J2 are expansion connectors. Unused I/Os of controller CY8C20246A are routed to these connectors.
- Connector J5 is used for ISSP programming of CY8C20246A. ISSP pins P1[0] and P1[1] are routed to this connector.
- If required, connector J5 can be reused as an I^2C header. For this, configure P1[0] and P1[1] as I^2C pins in the PSoC Designer project. However, CapSense buttons, BTN1 and BTN2, cannot be used. An alternative option is to configure P1[5] and P1[7] as I2C pins; both are mapped to J5.
- It is not recommended to configure ISSP pins P1[0] and P1[1] as CapSense sensors. However these pins are used as sensors in this kit only to demonstrate SmartSense self tuning capability.
- SmartSense requires an external modulation capacitor Cmod, connected from VSS to one of two dedicated PSoC pins P0[1] or P0[3]. The CY3280-SmartSense kit uses P0[3] as the Cmod (C4) pin. The recommended value for the external modulation capacitor is 2.2 nF. A ceramic capacitor must be used. The temperature capacitance coefficient is not important.
- Cypress strongly recommends using a 560-Ω series resistor on all CapSense sensor traces to suppress RF interference. This resistor must be placed as close to the CapSense controller as possible.

A.2 Board Layouts

A.2.1 PDC-09587 Top



A.2.2 PDC-09587 Bottom



A.3 Bill of Materials

Item	Qty	Reference	Value	Description	Manufacturer	Mfr Part Number
1				PCB	Cypress	PDC-09587 Rev04
2	2	C1,C4	2200 pFd	CAP CER 2200PF 50V 5% C0G 0805	Murata Electronics	GRM2165C1H222JA01D
3	4	C2,C5,C8,C9	0.1 uFd	CAP .10UF 10V CERAMIC X7R 0603	Kemet	C0603C104K8RACTU
4	3	C3,C6,C7	10 uFd 16v	CAP CERAMIC 10.0UF 16V X5R 1206	Kemet	C1206C106K4PACTU
5	5	D1,D4,D5,D6,D7	LED Red	LED Red CLEAR 1206 REAR MNT SMD	Stanley Electric Co	BR1111R-TR
6	2	D2,D3	DIODE SCHOTTKY	DIODE SCHOTTKY 0.5A 20V SOD-123	Fairchild Semiconductor	MBR0520L
7	2	J1,J2	CONN HEADER 10POS .100 R/A 15AU	CONN HEADER 10POS .100 R/A 15AU	FCI	68021-210HLF
8	4	J3,J4	Battery Clip AAA	CLIP BATTERY AAA/N .375X.460" SS	Keystone Electronics	55TR
9	1	J5	5 HEADER	CONN MALE 5POS .100" R/A GOLD	3M	961105-5604-AR
11	3	R1,R2,R3	5.1K	RES 5.1K OHM 1/16W 1% 0603 SMD	Yageo Corporation	RC0603FR-075K1L
11	5	R4,R11,R13,R14,R15	560E	RES 560 OHM 1/16W 5% 0402 SMD	Yageo Corporation	RC0402JR-07560RL
12	5	R5,R9,R10,R16,R17	330 ohm	RES 330 OHM 1/8W 1% 0805 SMD	Panasonic-ECG	ERJ-6ENF3300V
13	5	R6,R7,R22,R23,R24	ZERO	RES 0.0 OHM 1/10W 5% 0805 SMD	Panasonic-ECG	ERJ-6GEY0R00V
14	1	U3	CY8C20246A	CY8C20246A	Cypress	CY8C20246A
15	1	U1	CY8CMBR2044	CY8CMBR2044	Cypress	CY8CMBR2044
16	1	U4	MIC94090 SC-70-6	IC LOAD SW HGH SIDE 1.2A SC70-6	Micrel Inc	MIC94090YC6 TR
17	1	U2	SN74LVC1GU04	IC SINGLE INVERTER GATE SOT-23-5	Texas Instruments	SN74LVC1GU04DBVR
22	1	R21	ERJ-6GEYJ220V	RES 22 OHM 1/8W 5% 0805 SMD	Panasonic-ECG	ERJ-6GEYJ220V
No Load Components						
18	1	B0	CapSense Button 13mm Round			
19	1	B1	CapSense Button 9mm Round			
20	1	B2	CapSense Button 10mm Round			
21	2	B3,B4	CapSense Button 13mm Round			
22	6	CMOD1,CMOD2,VIN,VDD_Dev,VDD_Bat,VDD	T POINT R			
23	1	R8	NO LOAD			
24	2	R19,R12	5.1K	RES 5.1K OHM 1/16W 1% 0603 SMD	Yageo Corporation	RC0603FR-075K1L
25	1	R20	1.5K	RES 1.50K OHM 1/16W 1% 0603 SMD	Yageo Corporation	RC0603FR-071K5L
26	2	POT1,POT2	10k	TRIMPOT 10K OHM 6MM SQ SMD	Bourns Inc.	3361P-1-103GLF

Item	Qty	Reference	Value	Description	Manufacturer	Mfr Part Number
27	1	SW1	SP4T	SWITCH SLIDE SP4T LOW PROF SMD	Copal Electronics Inc	CUS-14TB
28	1	SW2	SPDT	SWITCH SLIDE SPDT .3A RT ANGLE	E-Switches	EG1270
29	1	R18	ZERO	RES 0.0 OHM 1/10W 5% 0805 SMD	Panasonic-ECG	ERJ-6GEY0R00V
30	1	D8	DIODE SCHOTTKY	DIODE SCHOTTKY 0.5A 20V SOD-123	Fairchild Semiconductor	MBR0520L

Mouser Electronics

Authorized Distributor

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Cypress Semiconductor:
CY3280-SMARTSENSE