



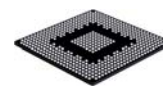
## MPC5674F

## MPC5674F Microcontroller Data Sheet

Covers: MPC5674F and MPC5673F



TEPBGA-416  
27mm x 27mm



TEPBGA-516  
27mm x 27mm



TEPBGA-324  
23mm x 23mm

- Dual issue, 32-bit CPU core complex (e200z7)
  - Compliant with the Power Architecture<sup>®</sup> embedded category
  - 16 KB I-Cache and 16 KB D-Cache
  - Includes an instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - Includes signal processing extension (SPE2) instruction support for digital signal processing (DSP) and single-precision floating point operations
- 4 MB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 256 KB on-chip general-purpose SRAM including 32 KB of standby RAM
- Two direct memory access controller (eDMA2) blocks
  - One supporting 64 channels
  - One supporting 32 channels
- Interrupt controller (INTC)
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- External bus interface (EBI) for calibration and application development (not available on all packages)
- System integration unit (SIU)
- Error correction status module (ECSM)
- Boot assist module (BAM) supports serial bootstrap via CAN or SCI
- Two second-generation enhanced time processor units (eTPU2) that share code and data RAM.
  - 32 standard channels per eTPU2
  - 24 KB code RAM
  - 6 KB parameter (data) RAM
- Enhanced modular input output system supporting 32 unified channels (eMIOS) with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Four enhanced queued analog-to-digital converters (eQADC)
  - Support for 64 analog channels
  - Includes one absolute reference ADC channel
  - Includes eight decimation filters
- Four deserial serial peripheral interface (DSPI) modules
- Three enhanced serial communication interface (eSCI) modules
- Four controller area network (FlexCAN) modules
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003/5001-2008 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller regulates supply voltage down to 1.2 V for core logic

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# 1 Ordering Information

## 1.1 Orderable Parts

Figure 1 and Table 1 describe and list the orderable part numbers for the MPC5674F.

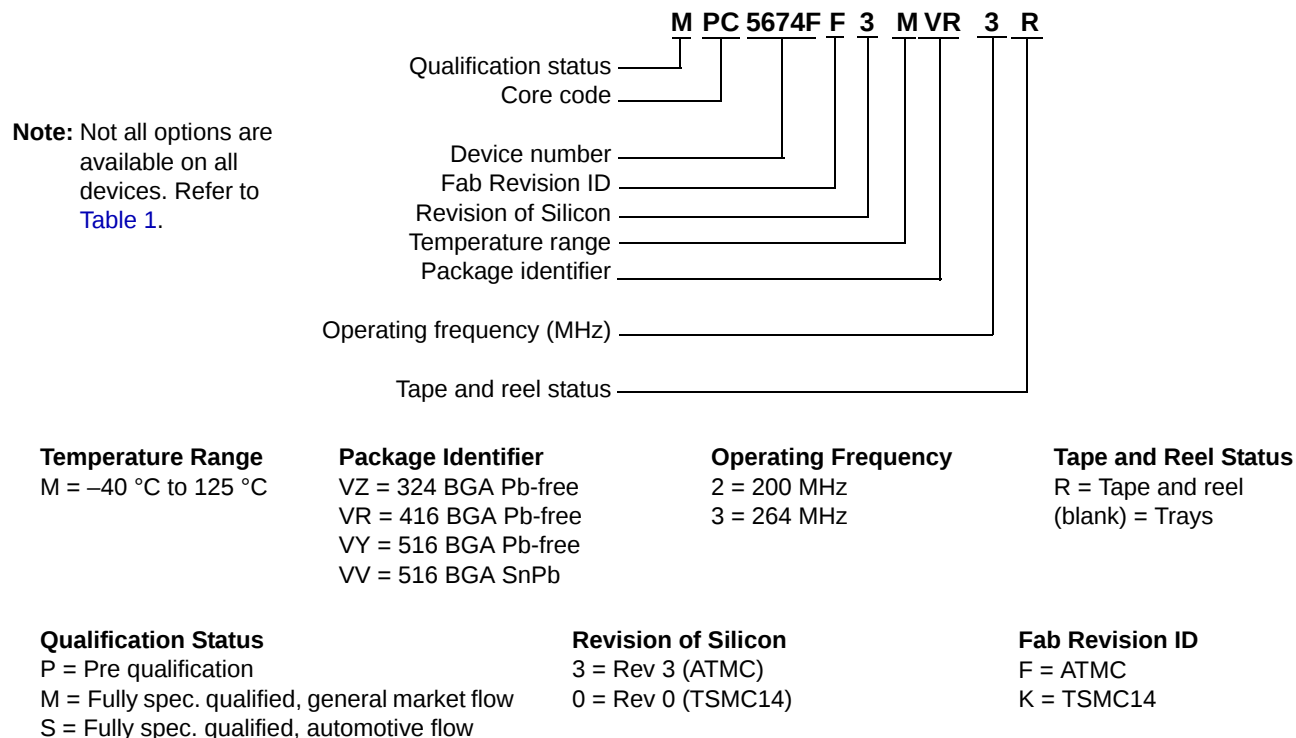


Figure 1. MPC5674F Orderable Part Number Description

Table 1. Orderable Part Numbers

| Freescale Part Number | Package Description       | Speed (MHz) <sup>1</sup> |                                      | Operating Temperature <sup>2</sup> |                       |
|-----------------------|---------------------------|--------------------------|--------------------------------------|------------------------------------|-----------------------|
|                       |                           | Nominal                  | Max <sup>3</sup> (f <sub>MAX</sub> ) | Min (T <sub>L</sub> )              | Max (T <sub>H</sub> ) |
| SPC5674FK0MVR3        | 416 PBGA, no EBI, Pb-free | 264                      | 270                                  | -40 °C                             | 125 °C                |
| SPC5674FK0MVY3        | 516 PBGA, w/EBI, Pb-free  | 264                      | 270                                  | -40 °C                             | 125 °C                |
| SPC5674FK0MVR3R       | 516 PBGA, w/EBI, SnPb     | 264                      | 270                                  | -40 °C                             | 125 °C                |
| SPC5674FK0MVR3        | 516 PBGA, w/EBI, SnPb     | 264                      | 200                                  | -40 °C                             | 125 °C                |
| SPC5674FK0MVY3R       | 516 PBGA, w/EBI, Pb-free  | 264                      | 270                                  | -40 °C                             | 125 °C                |
| SPC5674FK0MVY3        | 516 PBGA, w/EBI, Pb-free  | 264                      | 270                                  | -40 °C                             | 125 °C                |
| SPC5673FK0MVR2R       | 416 PBGA, no EBI, Pb-free | 200                      | 200                                  | -40 °C                             | 125 °C                |
| SPC5673FK0MVR2        | 416 PBGA, no EBI, Pb-free | 200                      | 200                                  | -40 °C                             | 125 °C                |
| SPC5673FK0MVR2R       | 324 PBGA, no EBI, Pb-free | 200                      | 200                                  | -40 °C                             | 125 °C                |
| SPC5673FK0MVR2        | 324 PBGA, no EBI, Pb-free | 200                      | 200                                  | -40 °C                             | 125 °C                |

<sup>1</sup> For the operating mode frequency of various blocks on the device, see Table 28.

## Ordering Information

- <sup>2</sup> The lowest ambient operating temperature is referenced by  $T_L$ ; the highest ambient operating temperature is referenced by  $T_H$ .
- <sup>3</sup> Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

## 1.2 MPC567xF Family Differences

Table 2 lists the differences between the MPC567xF devices. Refer to the *MPC5674F Reference Manual* for a full feature list and comparison.

**Table 2. MPC567xF Family Differences**

| Feature      | MPC5674F                 | MPC5674F                  | MPC5673F                 | MPC5673F                  |
|--------------|--------------------------|---------------------------|--------------------------|---------------------------|
| Package      | 416 BGA<br>516 BGA       | 324 BGA                   | 416 BGA<br>516 BGA       | 324 BGA                   |
| Flash        | 4 MB                     | 4 MB                      | 3 MB                     | 3 MB                      |
| SRAM         | 256 KB                   | 256 KB                    | 192 KB                   | 192 KB                    |
| External bus | Yes<br>(516 BGA only)    | No                        | Yes<br>(516 BGA only)    | No                        |
| Serial       | 3                        | 2                         | 3                        | 2                         |
| eSCI_A       | Yes                      | Yes                       | Yes                      | Yes                       |
| eSCI_B       | Yes                      | Yes                       | Yes                      | Yes                       |
| eSCI_C       | Yes                      | No                        | Yes                      | No                        |
| SPI          | 4                        | 3                         | 4                        | 3                         |
| DSPI_A       | Yes                      | No                        | Yes                      | No                        |
| DSPI_B       | Yes                      | Yes                       | Yes                      | Yes                       |
| DSPI_C       | Yes                      | Yes                       | Yes                      | Yes                       |
| DSPI_D       | Yes                      | Yes                       | Yes                      | Yes                       |
| eMIOS        | 32 channel               | 22 channel                | 32 channel               | 22 channel                |
| eTPU2        | 64 channel               | 47 channel                | 64 channel               | 47 channel                |
| eTPU_A       | Yes (32 ch)              | Yes (26 ch)               | Yes                      | Yes (26 ch)               |
| eTPU_B       | Yes (32 ch)              | Yes (21 ch, no<br>TCRCLK) | Yes                      | Yes (21 ch, no<br>TCRCLK) |
| ADC          | 64 channel               | 48 channel                | 64 channel               | 48 channel                |
| eQADC_A      | Yes (64 ch) <sup>1</sup> | Yes (24 ch)               | Yes (64 ch) <sup>1</sup> | Yes (24 ch)               |
| eQADC_B      |                          | Yes (24 ch)               |                          | Yes (24 ch)               |

<sup>1</sup> There are two pairs of 24 channels plus 16 shared channels. This gives 64 channels total: 40 per ADC (since 16 are shared).

## 2 MPC5674F Blocks

### 2.1 Block Diagram

Figure 2 shows a top-level block diagram of the MPC5674F device.

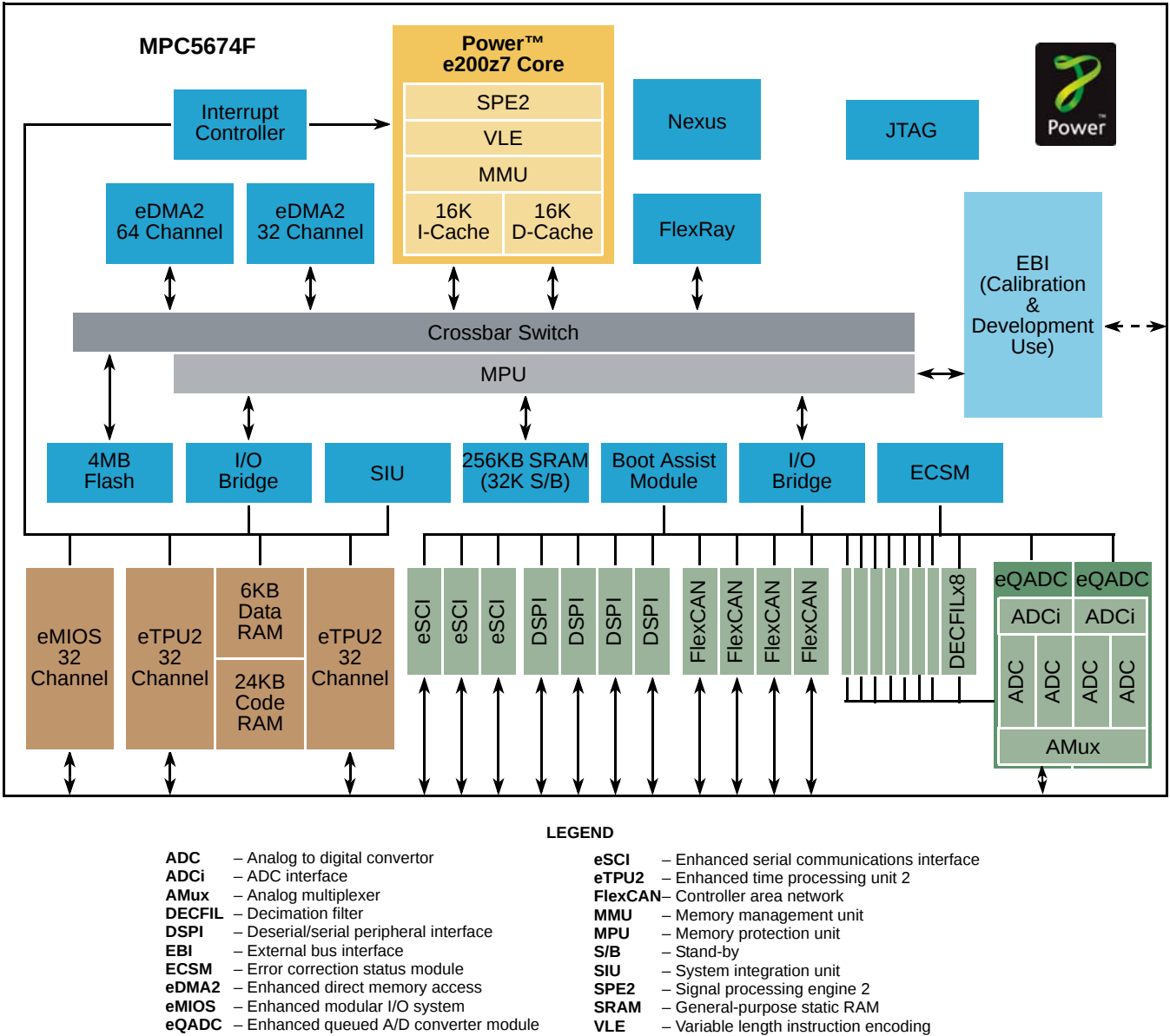


Figure 2. Block Diagram

## 3 Pin Assignments

The figures in this section show the primary pin function. For the full signal properties and muxing table, see [Appendix A, Signal Properties and Muxing](#).

## 3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

|    | 1         | 2       | 3          | 4       | 5          | 6       | 7     | 8      | 9       | 10      | 11        | 12         | 13      | 14         | 15      | 16      | 17      | 18    | 19      | 20      | 21      | 22      |    |
|----|-----------|---------|------------|---------|------------|---------|-------|--------|---------|---------|-----------|------------|---------|------------|---------|---------|---------|-------|---------|---------|---------|---------|----|
| A  | VSS       | VDD     | RSTOUT     | ANA0    | ANA1       | ANA4    | ANA5  | ANA15  | VDDA_A0 | VRH_A   | VRL_A     | REF-BYPCB1 | VDDA_B0 | REF-BYPCB1 | VRL_B   | VRH_B   | ANB2    | ANB3  | ANB6    | ANB7    | ANB22   | VSS     | A  |
| B  | VDDEH1    | VSS     | VDD        | TEST    | ANA2       | ANA3    | ANA6  | ANA7   | VDDA_A0 | VSSA_A1 | REF-BYPCA | REF-BYPCB  | VDDA_B1 | VSSA_B0    | ANB0    | ANB1    | ANB4    | ANB5  | ANB19   | ANB23   | VSS     | TCRCLKC | B  |
| C  | ETPUA21   | ETPUA26 | VSS        | VDD     | ANA8       | ANA10   | ANA9  | ANA13  | ANA17   | ANA19   | ANA21     | ANA23      | ANB10   | ANB9       | ANB11   | ANB12   | ANB14   | ANB16 | ANB20   | VSS     | ETPUC0  | VDDEH7  | C  |
| D  | ETPUA23   | ETPUA25 | ETPUA31    | VSS     | VDD        | ANA11   | ANA12 | ANA14  | ANA16   | ANA18   | ANA20     | ANA22      | ANB8    | ANB13      | ANB15   | ANB17   | ANB18   | ANB21 | VSS     | ETPUC1  | ETPUC3  | ETPUC2  | D  |
| E  | ETPUA20   | ETPUA22 | ETPUA24    | ETPUA30 |            |         |       |        |         |         |           |            |         |            |         |         |         |       | ETPUC5  | ETPUC10 | ETPUC11 | ETPUC4  | E  |
| F  | ETPUA13   | ETPUA14 | ETPUA15    | ETPUA27 |            |         |       |        |         |         |           |            |         |            |         |         |         |       | ETPUC12 | ETPUC14 | ETPUC13 | ETPUC9  | F  |
| G  | ETPUA10   | ETPUA11 | ETPUA12    | ETPUA17 |            |         |       |        |         |         |           |            |         |            |         |         |         |       | ETPUC20 | ETPUC18 | ETPUC19 | ETPUC17 | G  |
| H  | ETPUA5    | ETPUA6  | ETPUA9     | ETPUA16 |            |         |       |        |         |         |           |            |         |            |         |         |         |       | VDDEH7  | ETPUC23 | ETPUC22 | ETPUC21 | H  |
| J  | ETPUA1    | ETPUA2  | ETPUA3     | ETPUA4  |            |         |       |        | VSS     | VSS     | VSS       | VSS        | VSS     | VSS        |         |         |         |       | ETPUC27 | ETPUC28 | ETPUC26 | ETPUC24 | J  |
| K  | TCRCLKA   | ETPUA0  | VDD        | VSTBY   |            |         |       |        | VSS     | VSS     | VSS       | VSS        | VSS     | VSS        |         |         |         |       | ETPUC31 | ETPUC30 | ETPUC29 | ETPUC25 | K  |
| L  | BOOT-CFG1 | PLLCFG1 | PLLCFG2    | VDDEH1  |            |         |       |        | VSS     | VSS     | VSS       | VSS        | VSS     | VSS        |         |         |         |       | ETPUB12 | ETPUB13 | ETPUB14 | VDDEH7  | L  |
| M  | JCOMP     | RESET   | PLLCFG0    | RDY     |            |         |       |        | VDDE2   | VSS     | VSS       | VSS        | VSS     | VSS        |         |         |         |       | ETPUB7  | ETPUB10 | ETPUB11 | ETPUB9  | M  |
| N  | VDDE2     | MCKO    | MSE01      | EVTI    |            |         |       |        | VDDE2   | VDDE2   | VSS       | VSS        | VSS     | VSS        |         |         |         |       | ETPUB0  | VDDEH6  | ETPUB8  | ETPUB6  | N  |
| P  | EVT0      | MSE00   | MDO0       | MDO1    |            |         |       |        | VDDE2   | VDDE2   | VSS       | VSS        | VSS     | VSS        |         |         |         |       | TCRCLKB | ETPUB16 | ETPUB5  | ETPUB4  | P  |
| R  | MDO2      | MDO3    | MDO4       | MDO5    |            |         |       |        |         |         |           |            |         |            |         |         |         |       | ETPUB1  | ETPUB17 | ETPUB3  | ETPUB2  | R  |
| T  | MDO6      | MDO7    | MDO8       | VDDE2   |            |         |       |        |         |         |           |            |         |            |         |         |         |       | ETPUB19 | ETPUB18 | VDDEH6  | REGCTL  | T  |
| U  | MDO9      | MDO10   | MDO11      | MDO15   |            |         |       |        |         |         |           |            |         |            |         |         |         |       | ETPUB31 | ETPUB30 | VDDREG  | VSSSYN  | U  |
| V  | MDO12     | VDDE2   | MDO14      | VDD33_2 |            |         |       |        |         |         |           |            |         |            |         |         |         |       | VDD     | REGSEL  | VSSFL   | EXTAL   | V  |
| W  | TDO       | MDO13   | TMS        | VSS     | VDD        | VDDE2   | PCSB2 | VDDEH4 | VDD     | EMIOS8  | EMIOS9    | EMIOS18    | EMIOS22 | EMIOS27    | EMIOS31 | CNTXC   | CNRXC   | CNRXB | VSS     | VDD     | VDD33_3 | XTAL    | W  |
| Y  | TCK       | TDI     | VSS        | VDD     | FR_A_TX    | FR_B_TX | SCKA  | SCKB   | PCSB0   | EMIOS2  | EMIOS5    | EMIOS14    | EMIOS15 | EMIOS19    | EMIOS23 | EMIOS26 | EMIOS30 | CNTXB | CNRXD   | VSS     | VDD     | VDDSYN  | Y  |
| AA | ENGCLK    | VSS     | VDD        | FR_A_RX | FR_B_RX    | PCSA5   | SINA  | SINB   | EMIOS0  | EMIOS3  | EMIOS10   | EMIOS13    | EMIOS17 | EMIOS21    | EMIOS25 | EMIOS28 | EMIOS29 | CNRXA | SCKC    | SINC    | VSS     | VDD     | AA |
| AB | VSS       | VDD     | FR_A_TX_EN | VDDE2   | FR_B_TX_EN | PCSA0   | SOUTA | SOUTB  | EMIOS1  | EMIOS4  | EMIOS7    | EMIOS11    | EMIOS12 | EMIOS16    | EMIOS20 | EMIOS24 | CNTXA   | SOUTC | PCSC0   | VDDEH4  | CNTXD   | VSS     | AB |
|    | 1         | 2       | 3          | 4       | 5          | 6       | 7     | 8      | 9       | 10      | 11        | 12         | 13      | 14         | 15      | 16      | 17      | 18    | 19      | 20      | 21      | 22      |    |

Figure 3. MPC5674F 324-ball TEPBGA (full diagram)

|    | 1         | 2       | 3          | 4       | 5          | 6       | 7     | 8      | 9       | 10      | 11      |    |
|----|-----------|---------|------------|---------|------------|---------|-------|--------|---------|---------|---------|----|
| A  | VSS       | VDD     | RSTOUT     | ANA0    | ANA1       | ANA4    | ANA5  | ANA15  | VDDA_A0 | VRH_A   | VRL_A   | A  |
| B  | VDDEH1    | VSS     | VDD        | TEST    | ANA2       | ANA3    | ANA6  | ANA7   | VDDA_A0 | VSSA_A1 | REF-BYP | B  |
| C  | ETPUA21   | ETPUA26 | VSS        | VDD     | ANA8       | ANA10   | ANA9  | ANA13  | ANA17   | ANA19   | ANA21   | C  |
| D  | ETPUA23   | ETPUA25 | ETPUA31    | VSS     | VDD        | ANA11   | ANA12 | ANA14  | ANA16   | ANA18   | ANA20   | D  |
| E  | ETPUA20   | ETPUA22 | ETPUA24    | ETPUA30 |            |         |       |        |         |         |         |    |
| F  | ETPUA13   | ETPUA14 | ETPUA15    | ETPUA27 |            |         |       |        |         |         |         |    |
| G  | ETPUA10   | ETPUA11 | ETPUA12    | ETPUA17 |            |         |       |        |         |         |         |    |
| H  | ETPUA5    | ETPUA6  | ETPUA9     | ETPUA16 |            |         |       |        |         |         |         |    |
| J  | ETPUA1    | ETPUA2  | ETPUA3     | ETPUA4  |            |         |       |        | VSS     | VSS     | VSS     | J  |
| K  | TCRCLKA   | ETPUA0  | VDD        | VSTBY   |            |         |       |        | VSS     | VSS     | VSS     | K  |
| L  | BOOT-CFG1 | PLLCFG1 | PLLCFG2    | VDDEH1  |            |         |       |        | VSS     | VSS     | VSS     | L  |
| M  | JCOMP     | RESET   | PLLCFG0    | RDY     |            |         |       |        | VDDE2   | VSS     | VSS     | M  |
| N  | VDDE2     | MCKO    | MSEO1      | EVTI    |            |         |       |        | VDDE2   | VDDE2   | VSS     | N  |
| P  | EVTO      | MSEO0   | MDO0       | MDO1    |            |         |       |        | VDDE2   | VDDE2   | VSS     | P  |
| R  | MDO2      | MDO3    | MDO4       | MDO5    |            |         |       |        |         |         |         |    |
| T  | MDO6      | MDO7    | MDO8       | VDDE2   |            |         |       |        |         |         |         |    |
| U  | MDO9      | MDO10   | MDO11      | MDO15   |            |         |       |        |         |         |         |    |
| V  | MDO12     | VDDE2   | MDO14      | VDD33_2 |            |         |       |        |         |         |         |    |
| W  | TDO       | MDO13   | TMS        | VSS     | VDD        | VDDE2   | PCSB2 | VDDEH4 | VDD     | EMIOS8  | EMIOS9  | W  |
| Y  | TCK       | TDI     | VSS        | VDD     | FR_A_TX    | FR_B_TX | SCKA  | SCKB   | PCSB0   | EMIOS2  | EMIOS5  | Y  |
| AA | ENGCLK    | VSS     | VDD        | FR_A_RX | FR_B_RX    | PCSA5   | SINA  | SINB   | EMIOS0  | EMIOS3  | EMIOS10 | AA |
| AB | VSS       | VDD     | FR_A_TX_EN | VDDE2   | FR_B_TX_EN | PCSA0   | SOUTA | SOUTB  | EMIOS1  | EMIOS4  | EMIOS7  | AB |
|    | 1         | 2       | 3          | 4       | 5          | 6       | 7     | 8      | 9       | 10      | 11      |    |

**MPC5674F 324 TEPBGA**  
(as viewed from top through the package)

Figure 4. MPC5674F 324-ball TEPBGA (1 of 2)

## Pin Assignments

|    | 12         | 13      | 14         | 15      | 16      | 17      | 18    | 19      | 20      | 21      | 22      |    |
|----|------------|---------|------------|---------|---------|---------|-------|---------|---------|---------|---------|----|
| A  | REF-BYPCB1 | VDDA_B0 | REF-BYPCB1 | VRL_B   | VRH_B   | ANB2    | ANB3  | ANB6    | ANB7    | ANB22   | VSS     | A  |
| B  | REF-BYPCB  | VDDA_B1 | VSSA_B0    | ANB0    | ANB1    | ANB4    | ANB5  | ANB19   | ANB23   | VSS     | TCRCLKC | B  |
| C  | ANA23      | ANB10   | ANB9       | ANB11   | ANB12   | ANB14   | ANB16 | ANB20   | VSS     | ETPUC0  | VDDEH7  | C  |
| D  | ANA22      | ANB8    | ANB13      | ANB15   | ANB17   | ANB18   | ANB21 | VSS     | ETPUC1  | ETPUC3  | ETPUC2  | D  |
|    |            |         |            |         |         |         |       | ETPUC5  | ETPUC10 | ETPUC11 | ETPUC4  | E  |
|    |            |         |            |         |         |         |       | ETPUC12 | ETPUC14 | ETPUC13 | ETPUC9  | F  |
|    |            |         |            |         |         |         |       | ETPUC20 | ETPUC18 | ETPUC19 | ETPUC17 | G  |
|    |            |         |            |         |         |         |       | VDDEH7  | ETPUC23 | ETPUC22 | ETPUC21 | H  |
|    |            |         |            |         |         |         |       | ETPUC27 | ETPUC28 | ETPUC26 | ETPUC24 | J  |
|    |            |         |            |         |         |         |       | ETPUC31 | ETPUC30 | ETPUC29 | ETPUC25 | K  |
|    |            |         |            |         |         |         |       | ETPUB12 | ETPUB13 | ETPUB14 | VDDEH7  | L  |
|    |            |         |            |         |         |         |       | ETPUB7  | ETPUB10 | ETPUB11 | ETPUB9  | M  |
|    |            |         |            |         |         |         |       | ETPUB0  | VDDEH6  | ETPUB8  | ETPUB6  | N  |
|    |            |         |            |         |         |         |       | TCRCLKB | ETPUB16 | ETPUB5  | ETPUB4  | P  |
|    |            |         |            |         |         |         |       | ETPUB1  | ETPUB17 | ETPUB3  | ETPUB2  | R  |
|    |            |         |            |         |         |         |       | ETPUB19 | ETPUB18 | VDDEH6  | REGCTL  | T  |
|    |            |         |            |         |         |         |       | ETPUB31 | ETPUB30 | VDDREG  | VSSSYN  | U  |
|    |            |         |            |         |         |         |       | VDD     | REGSEL  | VSSFL   | EXTAL   | V  |
| W  | EMIOS18    | EMIOS22 | EMIOS27    | EMIOS31 | CNTXC   | CNRXC   | CNRXB | VSS     | VDD     | VDD33_3 | XTAL    | W  |
| Y  | EMIOS14    | EMIOS15 | EMIOS19    | EMIOS23 | EMIOS26 | EMIOS30 | CNTXB | CNRXD   | VSS     | VDD     | VDDSYN  | Y  |
| AA | EMIOS13    | EMIOS17 | EMIOS21    | EMIOS25 | EMIOS28 | EMIOS29 | CNRXA | SCKC    | SINC    | VSS     | VDD     | AA |
| AB | EMIOS11    | EMIOS12 | EMIOS16    | EMIOS20 | EMIOS24 | CNTXA   | SOUTC | PCSC0   | VDDEH4  | CNTXD   | VSS     | AB |
|    | 12         | 13      | 14         | 15      | 16      | 17      | 18    | 19      | 20      | 21      | 22      |    |

**MPC5674F 324 TEPBGA**  
(as viewed from top through the package)

**Figure 5. MPC5674F 324-ball TEPBGA (2 of 2)**

## 3.2 416-ball TEPBGA Pin Assignments

Figure 6 shows the 416-ball TEPBGA pin assignments in one figure. The same information is shown in Figure 7 through Figure 10.

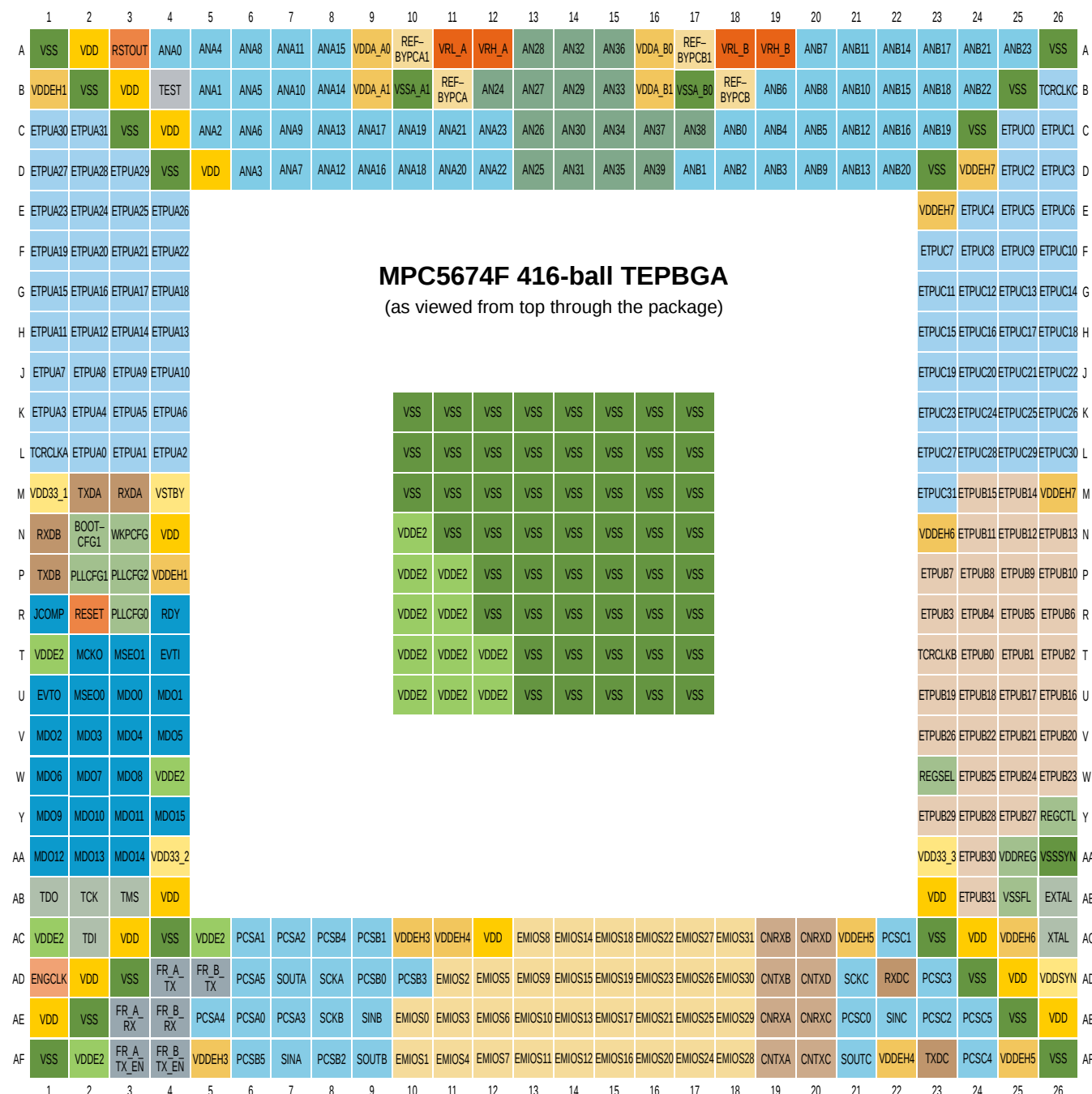


Figure 6. MPC5674F 416-ball TEPBGA (full diagram)

# Pin Assignments

|   | 1       | 2        | 3       | 4       | 5    | 6    | 7     | 8     | 9       | 10         | 11        | 12    | 13   |   |
|---|---------|----------|---------|---------|------|------|-------|-------|---------|------------|-----------|-------|------|---|
| A | VSS     | VDD      | RSTOUT  | ANA0    | ANA4 | ANA8 | ANA11 | ANA15 | VDDA_A0 | REFBYP-CA1 | VRL_A     | VRH_A | AN28 | A |
| B | VDDEH1  | VSS      | VDD     | TEST    | ANA1 | ANA5 | ANA10 | ANA14 | VDDA_A1 | VSSA_A1    | REFBYP-CA | AN24  | AN27 | B |
| C | ETPUA30 | ETPUA31  | VSS     | VDD     | ANA2 | ANA6 | ANA9  | ANA13 | ANA17   | ANA19      | ANA21     | ANA23 | AN26 | C |
| D | ETPUA27 | ETPUA28  | ETPUA29 | VSS     | VDD  | ANA3 | ANA7  | ANA12 | ANA16   | ANA18      | ANA20     | ANA22 | AN25 | D |
| E | ETPUA23 | ETPUA24  | ETPUA25 | ETPUA26 |      |      |       |       |         |            |           |       |      | E |
| F | ETPUA19 | ETPUA20  | ETPUA21 | ETPUA22 |      |      |       |       |         |            |           |       |      | F |
| G | ETPUA15 | ETPUA16  | ETPUA17 | ETPUA18 |      |      |       |       |         |            |           |       |      | G |
| H | ETPUA11 | ETPUA12  | ETPUA14 | ETPUA13 |      |      |       |       |         |            |           |       |      | H |
| J | ETPUA7  | ETPUA8   | ETPUA9  | ETPUA10 |      |      |       |       |         |            |           |       |      | J |
| K | ETPUA3  | ETPUA4   | ETPUA5  | ETPUA6  |      |      |       |       |         | VSS        | VSS       | VSS   | VSS  | K |
| L | TCRCLKA | ETPUA0   | ETPUA1  | ETPUA2  |      |      |       |       |         | VSS        | VSS       | VSS   | VSS  | L |
| M | VDD33_1 | TXDA     | RXDA    | VSTBY   |      |      |       |       |         | VSS        | VSS       | VSS   | VSS  | M |
| N | RXDB    | BOOTCFG1 | WKPCFG  | VDD     |      |      |       |       |         | VDDE2      | VSS       | VSS   | VSS  | N |
|   | 1       | 2        | 3       | 4       | 5    | 6    | 7     | 8     | 9       | 10         | 11        | 12    | 13   |   |

**MPC5674F 416-ball TEPBGA**  
(as viewed from top through the package)  
(1 of 4)

**Figure 7. MPC5674F 416-ball TEPBGA (1 of 4)**

|   | 14   | 15   | 16      | 17         | 18       | 19    | 20   | 21    | 22    | 23      | 24      | 25      | 26      |   |
|---|------|------|---------|------------|----------|-------|------|-------|-------|---------|---------|---------|---------|---|
| A | AN32 | AN36 | VDDA_B0 | REFBYP-CB1 | VRL_B    | VRH_B | ANB7 | ANB11 | ANB14 | ANB17   | ANB21   | ANB23   | VSS     | A |
| B | AN29 | AN33 | VDDA_B1 | VSSA_B0    | REFBYPCB | ANB6  | ANB8 | ANB10 | ANB15 | ANB18   | ANB22   | VSS     | TCRCLKC | B |
| C | AN30 | AN34 | AN37    | AN38       | ANB0     | ANB4  | ANB5 | ANB12 | ANB16 | ANB19   | VSS     | ETPUC0  | ETPUC1  | C |
| D | AN31 | AN35 | AN39    | ANB1       | ANB2     | ANB3  | ANB9 | ANB13 | ANB20 | VSS     | VDDEH7  | ETPUC2  | ETPUC3  | D |
| E |      |      |         |            |          |       |      |       |       | VDDEH7  | ETPUC4  | ETPUC5  | ETPUC6  | E |
| F |      |      |         |            |          |       |      |       |       | ETPUC7  | ETPUC8  | ETPUC9  | ETPUC10 | F |
| G |      |      |         |            |          |       |      |       |       | ETPUC11 | ETPUC12 | ETPUC13 | ETPUC14 | G |
| H |      |      |         |            |          |       |      |       |       | ETPUC15 | ETPUC16 | ETPUC17 | ETPUC18 | H |
| J |      |      |         |            |          |       |      |       |       | ETPUC19 | ETPUC20 | ETPUC21 | ETPUC22 | J |
| K | VSS  | VSS  | VSS     | VSS        |          |       |      |       |       | ETPUC23 | ETPUC24 | ETPUC25 | ETPUC26 | K |
| L | VSS  | VSS  | VSS     | VSS        |          |       |      |       |       | ETPUC27 | ETPUC28 | ETPUC29 | ETPUC30 | L |
| M | VSS  | VSS  | VSS     | VSS        |          |       |      |       |       | ETPUC31 | ETPUB15 | ETPUB14 | VDDEH7  | M |
| N | VSS  | VSS  | VSS     | VSS        |          |       |      |       |       | VDDEH6  | ETPUB11 | ETPUB12 | ETPUB13 | N |
|   | 14   | 15   | 16      | 17         | 18       | 19    | 20   | 21    | 22    | 23      | 24      | 25      | 26      |   |

**MPC5674F 416-ball TEPBGA**  
(as viewed from top through the package)  
(2 of 4)

**Figure 8. MPC5674F 416-ball TEPBGA (2 of 4)**

## Pin Assignments

|    | 1      | 2       | 3          | 4          | 5       | 6     | 7     | 8     | 9     | 10     | 11     | 12     | 13      |    |
|----|--------|---------|------------|------------|---------|-------|-------|-------|-------|--------|--------|--------|---------|----|
| P  | TXDB   | PLLCFG1 | PLLCFG2    | VDDEH1     |         |       |       |       |       | VDDE2  | VDDE2  | VSS    | VSS     | P  |
| R  | JCOMP  | RESET   | PLLCFG0    | RDY        |         |       |       |       |       | VDDE2  | VDDE2  | VSS    | VSS     | R  |
| T  | VDDE2  | MCKO    | MSEO1      | EVTI       |         |       |       |       |       | VDDE2  | VDDE2  | VDDE2  | VSS     | T  |
| U  | EVTO   | MSEO0   | MDO0       | MDO1       |         |       |       |       |       | VDDE2  | VDDE2  | VDDE2  | VSS     | U  |
| V  | MDO2   | MDO3    | MDO4       | MDO5       |         |       |       |       |       |        |        |        |         | V  |
| W  | MDO6   | MDO7    | MDO8       | VDDE2      |         |       |       |       |       |        |        |        |         | W  |
| Y  | MDO9   | MDO10   | MDO11      | MDO15      |         |       |       |       |       |        |        |        |         | Y  |
| AA | MDO12  | MDO13   | MDO14      | VDD33_2    |         |       |       |       |       |        |        |        |         | AA |
| AB | TDO    | TCK     | TMS        | VDD        |         |       |       |       |       |        |        |        |         | AB |
| AC | VDDE2  | TDI     | VDD        | VSS        | VDDE2   | PCSA1 | PCSA2 | PCSB4 | PCSB1 | VDDEH3 | VDDEH4 | VDD    | EMIOS8  | AC |
| AD | ENGCLK | VDD     | VSS        | FR_A_TX    | FR_B_TX | PCSA5 | SOUTA | SCKA  | PCSB0 | PCSB3  | EMIOS2 | EMIOS5 | EMIOS9  | AD |
| AE | VDD    | VSS     | FR_A_RX    | FR_B_RX    | PCSA4   | PCSA0 | PCSA3 | SCKB  | SINB  | EMIOS0 | EMIOS3 | EMIOS6 | EMIOS10 | AE |
| AF | VSS    | VDDE2   | FR_A_TX_EN | FR_B_TX_EN | VDDEH3  | PCSB5 | SINA  | PCSB2 | SOUTB | EMIOS1 | EMIOS4 | EMIOS7 | EMIOS11 | AF |
|    | 1      | 2       | 3          | 4          | 5       | 6     | 7     | 8     | 9     | 10     | 11     | 12     | 13      |    |

**MPC5674F 416-ball TEPBGA**  
(as viewed from top through the package)  
(3 of 4)

**Figure 9. MPC5674F 416-ball TEPBGA (3 of 4)**

|    | 14      | 15      | 16      | 17      | 18      | 19    | 20    | 21     | 22     | 23      | 24      | 25      | 26      |    |
|----|---------|---------|---------|---------|---------|-------|-------|--------|--------|---------|---------|---------|---------|----|
| P  | VSS     | VSS     | VSS     | VSS     |         |       |       |        |        | ETPUB7  | ETPUB8  | ETPUB9  | ETPUB10 | P  |
| R  | VSS     | VSS     | VSS     | VSS     |         |       |       |        |        | ETPUB3  | ETPUB4  | ETPUB5  | ETPUB6  | R  |
| T  | VSS     | VSS     | VSS     | VSS     |         |       |       |        |        | TCRCLKB | ETPUB0  | ETPUB1  | ETPUB2  | T  |
| U  | VSS     | VSS     | VSS     | VSS     |         |       |       |        |        | ETPUB19 | ETPUB18 | ETPUB17 | ETPUB16 | U  |
| V  |         |         |         |         |         |       |       |        |        | ETPUB26 | ETPUB22 | ETPUB21 | ETPUB20 | V  |
| W  |         |         |         |         |         |       |       |        |        | REGSEL  | ETPUB25 | ETPUB24 | ETPUB23 | W  |
| Y  |         |         |         |         |         |       |       |        |        | ETPUB29 | ETPUB28 | ETPUB27 | REGCTL  | Y  |
| AA |         |         |         |         |         |       |       |        |        | VDD33_3 | ETPUB30 | VDDREG  | VSSSYN  | AA |
| AB |         |         |         |         |         |       |       |        |        | VDD     | ETPUB31 | VSSFL   | EXTAL   | AB |
| AC | EMIOS14 | EMIOS18 | EMIOS22 | EMIOS27 | EMIOS31 | CNRXB | CNRXD | VDDEH5 | PCSC1  | VSS     | VDD     | VDDEH6  | XTAL    | AC |
| AD | EMIOS15 | EMIOS19 | EMIOS23 | EMIOS26 | EMIOS30 | CNTXB | CNTXD | SCKC   | RXDC   | PCSC3   | VSS     | VDD     | VDDSYN  | AD |
| AE | EMIOS13 | EMIOS17 | EMIOS21 | EMIOS25 | EMIOS29 | CNRXA | CNRXC | PCSC0  | SINC   | PCSC2   | PCSC5   | VSS     | VDD     | AE |
| AF | EMIOS12 | EMIOS16 | EMIOS20 | EMIOS24 | EMIOS28 | CNTXA | CNTXC | SOUTC  | VDDEH4 | TXDC    | PCSC4   | VDDEH5  | VSS     | AF |
|    | 14      | 15      | 16      | 17      | 18      | 19    | 20    | 21     | 22     | 23      | 24      | 25      | 26      |    |

**MPC5674F 416-ball TEPBGA**  
(as viewed from top through the package)  
(4 of 4)

**Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)**

## 3.3 516-ball TEPBGA Pin Assignments

Figure 11 shows the 516-ball TEPBGA pin assignments in one figure. The same information is shown split into four quadrants in Figure 12 through Figure 15.

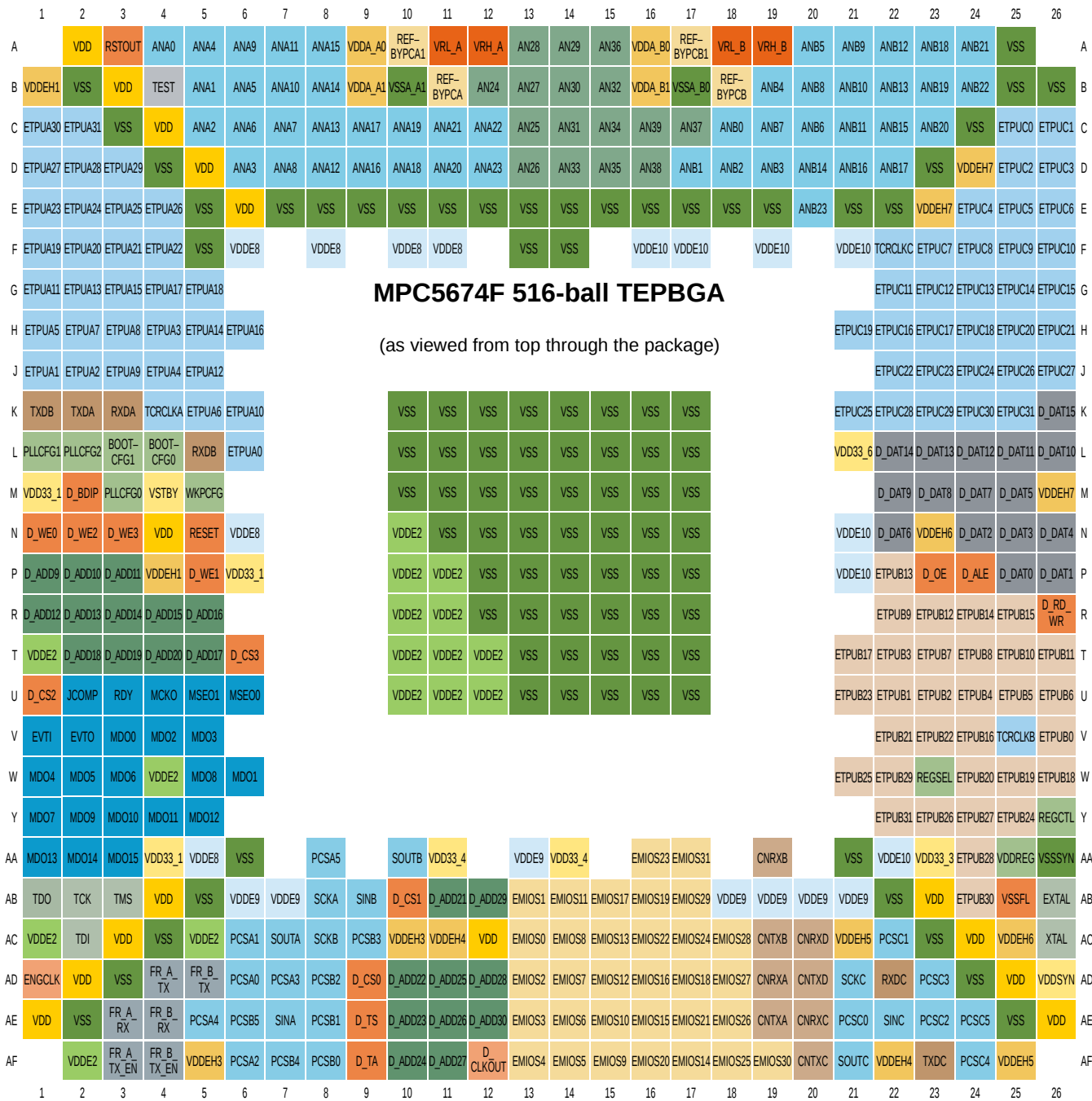


Figure 11. MPC5674F 516-ball TEPBGA (full diagram)

|   | 1       | 2       | 3        | 4        | 5       | 6       | 7     | 8     | 9       | 10         | 11       | 12    | 13   |   |
|---|---------|---------|----------|----------|---------|---------|-------|-------|---------|------------|----------|-------|------|---|
| A |         | VDD     | RSTOUT   | ANA0     | ANA4    | ANA9    | ANA11 | ANA15 | VDDA_A0 | REF-BYPCA1 | VRL_A    | VRH_A | AN28 | A |
| B | VDDEH1  | VSS     | VDD      | TEST     | ANA1    | ANA5    | ANA10 | ANA14 | VDDA_A1 | VSSA_A1    | REFBYPCA | AN24  | AN27 | B |
| C | ETPUA30 | ETPUA31 | VSS      | VDD      | ANA2    | ANA6    | ANA7  | ANA13 | ANA17   | ANA19      | ANA21    | ANA22 | AN25 | C |
| D | ETPUA27 | ETPUA28 | ETPUA29  | VSS      | VDD     | ANA3    | ANA8  | ANA12 | ANA16   | ANA18      | ANA20    | ANA23 | AN26 | D |
| E | ETPUA23 | ETPUA24 | ETPUA25  | ETPUA26  | VSS     | VDD     | VSS   | VSS   | VSS     | VSS        | VSS      | VSS   | VSS  | E |
| F | ETPUA19 | ETPUA20 | ETPUA21  | ETPUA22  | VSS     | VDDE8   |       | VDDE8 |         | VDDE8      | VDDE8    |       | VSS  | F |
| G | ETPUA11 | ETPUA13 | ETPUA15  | ETPUA17  | ETPUA18 |         |       |       |         |            |          |       |      | G |
| H | ETPUA5  | ETPUA7  | ETPUA8   | ETPUA3   | ETPUA14 | ETPUA16 |       |       |         |            |          |       |      | H |
| J | ETPUA1  | ETPUA2  | ETPUA9   | ETPUA4   | ETPUA12 |         |       |       |         |            |          |       |      | J |
| K | TXDB    | TXDA    | RXDA     | TCRCLKA  | ETPUA6  | ETPUA10 |       |       |         | VSS        | VSS      | VSS   | VSS  | K |
| L | PLLCFG1 | PLLCFG2 | BOOTCFG1 | BOOTCFG0 | RXDB    | ETPUA0  |       |       |         | VSS        | VSS      | VSS   | VSS  | L |
| M | VDD33_1 | D_BDIP  | PLLCFG0  | VSTBY    | WKPCFG  |         |       |       |         | VSS        | VSS      | VSS   | VSS  | M |
| N | D_WE0   | D_WE2   | D_WE3    | VDD      | RESET   | VDDE8   |       |       |         | VDDE2      | VSS      | VSS   | VSS  | N |
|   | 1       | 2       | 3        | 4        | 5       | 6       | 7     | 8     | 9       | 10         | 11       | 12    | 13   |   |

**MPC5674F 516-ball TEPBGA**  
(as viewed from top through the package)  
(1 of 4)

**Figure 12. MPC5674F 516-ball TEPBGA (1 of 4)**

## Pin Assignments

|   | 14                                                                                      | 15   | 16      | 17         | 18       | 19     | 20    | 21      | 22      | 23      | 24      | 25      | 26      |   |
|---|-----------------------------------------------------------------------------------------|------|---------|------------|----------|--------|-------|---------|---------|---------|---------|---------|---------|---|
| A | AN29                                                                                    | AN36 | VDDA_B0 | REF-BYPCB1 | VRL_B    | VRH_B  | ANB5  | ANB9    | ANB12   | ANB18   | ANB21   | VSS     |         | A |
| B | AN30                                                                                    | AN32 | VDDA_B1 | VSSA_B0    | REFBYPCB | ANB4   | ANB8  | ANB10   | ANB13   | ANB19   | ANB22   | VSS     | VSS     | B |
| C | AN31                                                                                    | AN34 | AN39    | AN37       | ANB0     | ANB7   | ANB6  | ANB11   | ANB15   | ANB20   | VSS     | ETPUC0  | ETPUC1  | C |
| D | AN33                                                                                    | AN35 | AN38    | ANB1       | ANB2     | ANB3   | ANB14 | ANB16   | ANB17   | VSS     | VDDEH7  | ETPUC2  | ETPUC3  | D |
| E | VSS                                                                                     | VSS  | VSS     | VSS        | VSS      | VSS    | ANB23 | VSS     | VSS     | VDDEH7  | ETPUC4  | ETPUC5  | ETPUC6  | E |
| F | VSS                                                                                     |      | VDDE10  | VDDE10     |          | VDDE10 |       | VDDE10  | TCRCLKC | ETPUC7  | ETPUC8  | ETPUC9  | ETPUC10 | F |
| G | <b>MPC5674F 516-ball TEPBGA</b><br>(as viewed from top through the package)<br>(2 of 4) |      |         |            |          |        |       |         | ETPUC11 | ETPUC12 | ETPUC13 | ETPUC14 | ETPUC15 | G |
| H |                                                                                         |      |         |            |          |        |       | ETPUC19 | ETPUC16 | ETPUC17 | ETPUC18 | ETPUC20 | ETPUC21 | H |
| J |                                                                                         |      |         |            |          |        |       |         | ETPUC22 | ETPUC23 | ETPUC24 | ETPUC26 | ETPUC27 | J |
| K |                                                                                         |      |         |            |          |        |       | ETPUC25 | ETPUC28 | ETPUC29 | ETPUC30 | ETPUC31 | D_DAT15 | K |
| L | VSS                                                                                     | VSS  | VSS     | VSS        |          |        |       | VDD33_6 | D_DAT14 | D_DAT13 | D_DAT12 | D_DAT11 | D_DAT10 | L |
| M | VSS                                                                                     | VSS  | VSS     | VSS        |          |        |       |         | D_DAT9  | D_DAT8  | D_DAT7  | D_DAT5  | VDDEH7  | M |
| N | VSS                                                                                     | VSS  | VSS     | VSS        |          |        |       | VDDE10  | D_DAT6  | VDDEH6  | D_DAT2  | D_DAT3  | D_DAT4  | N |
|   | 14                                                                                      | 15   | 16      | 17         | 18       | 19     | 20    | 21      | 22      | 23      | 24      | 25      | 26      |   |

**Figure 13. MPC5674F 516-ball TEPBGA (2 of 4)**

|    | 1       | 2       | 3          | 4          | 5       | 6       | 7     | 8     | 9     | 10      | 11      | 12       | 13     |    |
|----|---------|---------|------------|------------|---------|---------|-------|-------|-------|---------|---------|----------|--------|----|
| P  | D_ADD9  | D_ADD10 | D_ADD11    | VDDEH1     | D_WE1   | VDD33_1 |       |       |       | VDDE2   | VDDE2   | VSS      | VSS    | P  |
| R  | D_ADD12 | D_ADD13 | D_ADD14    | D_ADD15    | D_ADD16 |         |       |       |       | VDDE2   | VDDE2   | VSS      | VSS    | R  |
| T  | VDDE2   | D_ADD18 | D_ADD19    | D_ADD20    | D_ADD17 | D_CS3   |       |       |       | VDDE2   | VDDE2   | VDDE2    | VSS    | T  |
| U  | D_CS2   | JCOMP   | RDY        | MCKO       | MSE01   | MSE00   |       |       |       | VDDE2   | VDDE2   | VDDE2    | VSS    | U  |
| V  | EVTI    | EVTO    | MDO0       | MDO2       | MDO3    |         |       |       |       |         |         |          |        | V  |
| W  | MDO4    | MDO5    | MDO6       | VDDE2      | MDO8    | MDO1    |       |       |       |         |         |          |        | W  |
| Y  | MDO7    | MDO9    | MDO10      | MDO11      | MDO12   |         |       |       |       |         |         |          |        | Y  |
| AA | MDO13   | MDO14   | MDO15      | VDD33_1    | VDDE8   | VSS     |       | PCSA5 |       | SOUTB   | VDD33_4 |          | VDDE9  | AA |
| AB | TDO     | TCK     | TMS        | VDD        | VSS     | VDDE9   | VDDE9 | SCKA  | SINB  | D_CS1   | D_ADD21 | D_ADD29  | EMIOS1 | AB |
| AC | VDDE2   | TDI     | VDD        | VSS        | VDDE2   | PCSA1   | SOUTA | SCKB  | PCSB3 | VDDEH3  | VDDEH4  | VDD      | EMIOS0 | AC |
| AD | ENGCLK  | VDD     | VSS        | FR_A_TX    | FR_B_TX | PCSA0   | PCSA3 | PCSB2 | D_CS0 | D_ADD22 | D_ADD25 | D_ADD28  | EMIOS2 | AD |
| AE | VDD     | VSS     | FR_A_RX    | FR_B_RX    | PCSA4   | PCSB5   | SINA  | PCSB1 | D_TS  | D_ADD23 | D_ADD26 | D_ADD30  | EMIOS3 | AE |
| AF |         | VDDE2   | FR_A_TX_EN | FR_B_TX_EN | VDDEH3  | PCSA2   | PCSB4 | PCSB0 | D_TA  | D_ADD24 | D_ADD27 | D_CLKOUT | EMIOS4 | AF |
|    | 1       | 2       | 3          | 4          | 5       | 6       | 7     | 8     | 9     | 10      | 11      | 12       | 13     |    |

### MPC5674F 516-ball TEPBGA

(as viewed from top through the package)  
(3 of 4)

Figure 14. MPC5674F 516-ball TEPBGA (3 of 4)

# Pin Assignments

|    | 14                                                                                      | 15      | 16      | 17      | 18      | 19      | 20    | 21      | 22      | 23      | 24      | 25      | 26      |    |
|----|-----------------------------------------------------------------------------------------|---------|---------|---------|---------|---------|-------|---------|---------|---------|---------|---------|---------|----|
| P  | VSS                                                                                     | VSS     | VSS     | VSS     |         |         |       | VDDE10  | ETPUB13 | D_OE    | D_ALE   | D_DAT0  | D_DAT1  | P  |
| R  | VSS                                                                                     | VSS     | VSS     | VSS     |         |         |       |         | ETPUB9  | ETPUB12 | ETPUB14 | ETPUB15 | D_RD_WR | R  |
| T  | VSS                                                                                     | VSS     | VSS     | VSS     |         |         |       | ETPUB17 | ETPUB3  | ETPUB7  | ETPUB8  | ETPUB10 | ETPUB11 | T  |
| U  | VSS                                                                                     | VSS     | VSS     | VSS     |         |         |       | ETPUB23 | ETPUB1  | ETPUB2  | ETPUB4  | ETPUB5  | ETPUB6  | U  |
| V  | <b>MPC5674F 516-ball TEPBGA</b><br>(as viewed from top through the package)<br>(4 of 4) |         |         |         |         |         |       |         | ETPUB21 | ETPUB22 | ETPUB16 | TCRCLKB | ETPUB0  | V  |
| W  |                                                                                         |         |         |         |         |         |       | ETPUB25 | ETPUB29 | REGSEL  | ETPUB20 | ETPUB19 | ETPUB18 | W  |
| Y  |                                                                                         |         |         |         |         |         |       |         | ETPUB31 | ETPUB26 | ETPUB27 | ETPUB24 | REGCTL  | Y  |
| AA | VDD33_4                                                                                 |         | EMIOS23 | EMIOS31 |         | CNRXB   |       | VSS     | VDDE10  | VDD33_3 | ETPUB28 | VDDREG  | VSSSYN  | AA |
| AB | EMIOS11                                                                                 | EMIOS17 | EMIOS19 | EMIOS29 | VDDE9   | VDDE9   | VDDE9 | VDDE9   | VSS     | VDD     | ETPUB30 | VSSSFL  | EXTAL   | AB |
| AC | EMIOS8                                                                                  | EMIOS13 | EMIOS22 | EMIOS24 | EMIOS28 | CNTXB   | CNRXD | VDDEH5  | PCSC1   | VSS     | VDD     | VDDEH6  | XTAL    | AC |
| AD | EMIOS7                                                                                  | EMIOS12 | EMIOS16 | EMIOS18 | EMIOS27 | CNRXA   | CNTXD | SCKC    | RXDC    | PCSC3   | VSS     | VDD     | VDDSYN  | AD |
| AE | EMIOS6                                                                                  | EMIOS10 | EMIOS15 | EMIOS21 | EMIOS26 | CNTXA   | CNRXC | PCSC0   | SINC    | PCSC2   | PCSC5   | VSS     | VDD     | AE |
| AF | EMIOS5                                                                                  | EMIOS9  | EMIOS20 | EMIOS14 | EMIOS25 | EMIOS30 | CNTXC | SOUTC   | VDDEH4  | TXDC    | PCSC4   | VDDEH5  |         | AF |
|    | 14                                                                                      | 15      | 16      | 17      | 18      | 19      | 20    | 21      | 22      | 23      | 24      | 25      | 26      |    |

Figure 15. MPC5674F 516-ball TEPBGA (4 of 4)

## 3.4 Signal Properties and Muxing

See [Appendix A, Signal Properties and Muxing](#), for a listing and description of the pin functions and properties.

## 4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5674F.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

### 4.1 Maximum Ratings

Table 3. Absolute Maximum Ratings<sup>1</sup>

| Spec | Characteristic                                                                     | Symbol                 | Min              | Max                | Unit |
|------|------------------------------------------------------------------------------------|------------------------|------------------|--------------------|------|
| 1    | 1.2 V Core Supply Voltage                                                          | $V_{DD}$               | -0.3             | 2.0 <sup>2</sup>   | V    |
| 2    | SRAM Standby Voltage                                                               | $V_{STBY}$             | -0.3             | 6.4 <sup>3,4</sup> | V    |
| 3    | Clock Synthesizer Voltage                                                          | $V_{DDSYN}$            | -0.3             | 5.3 <sup>4,5</sup> | V    |
| 4    | I/O Supply Voltage (I/O buffers and predrivers)                                    | $V_{DD33}$             | -0.3             | 5.3 <sup>4,5</sup> | V    |
| 5    | Analog Supply Voltage (reference to $V_{SSA}$ <sup>6</sup> )                       | $V_{DDA}$ <sup>7</sup> | -0.3             | 6.4 <sup>3,4</sup> | V    |
| 6    | I/O Supply Voltage (fast I/O pads)                                                 | $V_{DDE}$              | -0.3             | 5.3 <sup>4,5</sup> | V    |
| 7    | I/O Supply Voltage (medium I/O pads)                                               | $V_{DDEH}$             | -0.3             | 6.4 <sup>3,4</sup> | V    |
| 8    | Voltage Regulator Input Supply Voltage                                             | $V_{DDREG}$            | -0.3             | 6.4 <sup>3,4</sup> | V    |
| 9    | Analog Reference High Voltage (reference to $V_{RL}$ <sup>8</sup> )                | $V_{RH}$ <sup>9</sup>  | -0.3             | 6.4 <sup>3,4</sup> | V    |
| 10   | $V_{SS}$ to $V_{SSA}$ <sup>8</sup> Differential Voltage                            | $V_{SS} - V_{SSA}$     | -0.1             | 0.1                | V    |
| 11   | $V_{REF}$ Differential Voltage                                                     | $V_{RH} - V_{RL}$      | -0.3             | 6.4 <sup>3,4</sup> | V    |
| 12   | $V_{RL}$ to $V_{SSA}$ Differential Voltage                                         | $V_{RL} - V_{SSA}$     | -0.3             | 0.3                | V    |
| 13   | $V_{DD33}$ to $V_{DDSYN}$ Differential Voltage                                     | $V_{DD33} - V_{DDSYN}$ | -0.1             | 0.1                | V    |
| 14   | $V_{SSSYN}$ to $V_{SS}$ Differential Voltage                                       | $V_{SSSYN} - V_{SS}$   | -0.1             | 0.1                | V    |
| 15   | Maximum Digital Input Current <sup>10</sup> (per pin, applies to all digital pins) | $I_{MAXD}$             | -3 <sup>11</sup> | 3 <sup>11</sup>    | mA   |
| 16   | Maximum Analog Input Current <sup>12</sup> (per pin, applies to all analog pins)   | $I_{MAXA}$             | -3 <sup>7</sup>  | 3 <sup>7,11</sup>  | mA   |
| 17   | Maximum Operating Temperature Range <sup>13</sup> – Die Junction Temperature       | $T_J$                  | -40.0            | 150.0              | °C   |
| 18   | Storage Temperature Range                                                          | $T_{stg}$              | -55.0            | 150.0              | °C   |
| 19   | Maximum Solder Temperature <sup>14</sup><br>Pb-free package<br>SnPb package        | $T_{sdr}$              | —<br>—           | 260.0<br>245.0     | °C   |
| 20   | Moisture Sensitivity Level <sup>15</sup>                                           | MSL                    | —                | 3                  | —    |

- <sup>1</sup> Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
- <sup>2</sup> 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.
- <sup>3</sup> 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.
- <sup>4</sup> Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
- <sup>5</sup> 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.
- <sup>6</sup> MPC5674F has two analog power supply pins on the pinout: VDDA\_A and VDDA\_B.
- <sup>7</sup> MPC5674F has two analog ground supply pins on the pinout: VSSA\_A and VSSA\_B.
- <sup>8</sup> MPC5674F has two analog low reference voltage pins on the pinout: VRL\_A and VRL\_B.
- <sup>9</sup> MPC5674F has two analog high reference voltage pins on the pinout: VRH\_A and VRH\_B.
- <sup>10</sup> Total injection current for all pins must not exceed 25 mA at maximum operating voltage.
- <sup>11</sup> Injection current of  $\pm 5$  mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or  $V_{DDEH}$  supply when under this stress condition.
- <sup>12</sup> Total injection current for all analog input pins must not exceed 15 mA.
- <sup>13</sup> Lifetime operation at these specification limits is not guaranteed.
- <sup>14</sup> Solder profile per CDF-AEC-Q100.
- <sup>15</sup> Moisture sensitivity per JEDEC test method A112.

## 4.2 Thermal Characteristics

**Table 4. Thermal Characteristics, 416-pin TEPBGA Package<sup>1</sup>**

| Characteristic                                                                | Symbol           | Value | Unit |
|-------------------------------------------------------------------------------|------------------|-------|------|
| Junction to Ambient <sup>2,3</sup> Natural Convection (Single layer board)    | $R_{\theta JA}$  | 24    | °C/W |
| Junction to Ambient <sup>2,4</sup> Natural Convection (Four layer board 2s2p) | $R_{\theta JA}$  | 18    | °C/W |
| Junction to Ambient (@200 ft./min., Single layer board)                       | $R_{\theta JMA}$ | 19    | °C/W |
| Junction to Ambient (@200 ft./min., Four layer board 2s2p)                    | $R_{\theta JMA}$ | 14    | °C/W |
| Junction to Board <sup>5</sup>                                                | $R_{\theta JB}$  | 9     | °C/W |
| Junction to Case <sup>6</sup>                                                 | $R_{\theta JC}$  | 6     | °C/W |
| Junction to Package Top <sup>7</sup> Natural Convection                       | $\Psi_{JT}$      | 2     | °C/W |

- <sup>1</sup> Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.
- <sup>2</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- <sup>3</sup> Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- <sup>4</sup> Per JEDEC JESD51-6 with the board horizontal.
- <sup>5</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- <sup>6</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
- <sup>7</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

**Table 5. Thermal Characteristics, 516-pin TEPBGA Package<sup>1</sup>**

| Characteristic                                                                | Symbol           | Value | Unit |
|-------------------------------------------------------------------------------|------------------|-------|------|
| Junction to Ambient <sup>2,3</sup> Natural Convection (Single layer board)    | $R_{\theta JA}$  | 25    | °C/W |
| Junction to Ambient <sup>2,4</sup> Natural Convection (Four layer board 2s2p) | $R_{\theta JA}$  | 18    | °C/W |
| Junction to Ambient (@200 ft./min., Single layer board)                       | $R_{\theta JMA}$ | 20    | °C/W |
| Junction to Ambient (@200 ft./min., Four layer board 2s2p)                    | $R_{\theta JMA}$ | 15    | °C/W |
| Junction to Board <sup>5</sup>                                                | $R_{\theta JB}$  | 10    | °C/W |
| Junction to Case <sup>6</sup>                                                 | $R_{\theta JC}$  | 6     | °C/W |
| Junction to Package Top <sup>7</sup> Natural Convection                       | $\Psi_{JT}$      | 2     | °C/W |

- <sup>1</sup> Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.
- <sup>2</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- <sup>3</sup> Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- <sup>4</sup> Per JEDEC JESD51-6 with the board horizontal.
- <sup>5</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- <sup>6</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
- <sup>7</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

**Table 6. Thermal Characteristics, 324-pin Package<sup>1</sup>**

| MPC5674F Thermal Characteristic                                                 | Symbol           | Value | Unit |
|---------------------------------------------------------------------------------|------------------|-------|------|
| Junction to ambient <sup>2,3</sup> , natural convection (one-layer board)       | $R_{\theta JA}$  | 29    | °C/W |
| Junction to ambient <sup>1,4</sup> , natural convection (four-layer board 2s2p) | $R_{\theta JA}$  | 19    | °C/W |
| Junction to ambient (@200 ft./min., one-layer board)                            | $R_{\theta JMA}$ | 23    | °C/W |
| Junction to ambient (@200 ft./min., four-layer board 2s2p)                      | $R_{\theta JMA}$ | 16    | °C/W |
| Junction to board <sup>5</sup> (four-layer board 2s2p)                          | $R_{\theta JB}$  | 10    | °C/W |
| Junction to case <sup>6</sup>                                                   | $R_{\theta JC}$  | 7     | °C/W |
| Junction to package top <sup>7</sup> , natural convection                       | $\Psi_{JT}$      | 2     | °C/W |

- <sup>1</sup> Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.
- <sup>2</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- <sup>3</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
- <sup>4</sup> Per JEDEC JESD51-6 with the board horizontal.
- <sup>5</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

- <sup>6</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
- <sup>7</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

## 4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature,  $T_J$ , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \text{Eqn. 1}$$

where:

$T_A$  = ambient temperature for the package ( $^{\circ}\text{C}$ )

$R_{\theta JA}$  = junction to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$P_D$  = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 2}$$

where:

$R_{\theta JA}$  = junction to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  = junction to case thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta CA}$  = case to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} * P_D) \quad \text{Eqn. 3}$$

where:

$T_T$  = thermocouple temperature on top of the package ( $^{\circ}\text{C}$ )

$\Psi_{JT}$  = thermal characterization parameter ( $^{\circ}\text{C}/\text{W}$ )

$P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

## Electrical Characteristics

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### References:

Semiconductor Equipment and Materials International  
3081 Zanker Road  
San Jose, CA 95134  
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at <http://www.jedec.org>.

- C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

## 4.3 EMI (Electromagnetic Interference) Characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for "radiated emissions." The following tables list the values of the device's radiated emissions operating behaviors.

**Table 7. EMC Radiated Emissions Operating Behaviors: 416 BGA**

| Symbol        | Description                                           | Conditions                                                                                                                                                                  | $f_{osc}$<br>$f_{sys}$                                          | Frequency band (MHz) | Level (max.) | Unit       | Notes |
|---------------|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|----------------------|--------------|------------|-------|
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>416 BGA<br>EBI off<br>CLK on<br>FM off              | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 26           | dB $\mu$ V | 1     |
|               |                                                       |                                                                                                                                                                             |                                                                 | 50–150               | 30           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 150–500              | 34           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 500–1000             | 30           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | IEC and SAE level    | $I^2$        | —          | 1, 3  |
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>416 BGA<br>EBI off<br>CLK off<br>FM on <sup>4</sup> | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 24           | dB $\mu$ V | 1     |
|               |                                                       |                                                                                                                                                                             |                                                                 | 50–150               | 25           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 150–500              | 25           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | 500–1000             | 21           |            |       |
|               |                                                       |                                                                                                                                                                             |                                                                 | IEC and SAE level    | $K^5$        | —          | 1, 3  |

<sup>1</sup> Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>2</sup>  $I = 36\text{ dB}\mu\text{V}$

<sup>3</sup> Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>4</sup> “FM on” = FM depth of  $\pm 2\%$

<sup>5</sup> K = 30 dB $\mu$ V

**Table 8. EMC Radiated Emissions Operating Behaviors: 516 BGA**

| Symbol        | Description                                           | Conditions                                                                                                                                                                | $f_{osc}$<br>$f_{sys}$                                          | Frequency band (MHz) | Level (max.)   | Unit       | Notes           |
|---------------|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|----------------------|----------------|------------|-----------------|
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>516 BGA<br>EBI on<br>CLK on<br>FM off             | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 40             | dB $\mu$ V | <sup>1</sup>    |
|               |                                                       |                                                                                                                                                                           |                                                                 | 50–150               | 48             |            |                 |
|               |                                                       |                                                                                                                                                                           |                                                                 | 150–500              | 48             |            |                 |
|               |                                                       |                                                                                                                                                                           |                                                                 | 500–1000             | 47             |            |                 |
|               |                                                       |                                                                                                                                                                           |                                                                 | IEC and SAE level    | G <sup>2</sup> | —          | <sup>1, 3</sup> |
| $V_{RE\_TEM}$ | Radiated emissions, electric field and magnetic field | $V_{DD} = 1.2\text{ V}$<br>$V_{DDE} = 3.3\text{ V}$<br>$V_{DDEH} = 5\text{ V}$<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>516 BGA<br>EBI on<br>CLK on<br>FM on <sup>4</sup> | 40 MHz crystal<br>264 MHz<br>( $f_{EBI\_CAL} = 66\text{ MHz}$ ) | 0.15–50              | 40             | dB $\mu$ V | <sup>1</sup>    |
|               |                                                       |                                                                                                                                                                           |                                                                 | 50–150               | 44             |            |                 |
|               |                                                       |                                                                                                                                                                           |                                                                 | 150–500              | 41             |            |                 |
|               |                                                       |                                                                                                                                                                           |                                                                 | 500–1000             | 36             |            |                 |
|               |                                                       |                                                                                                                                                                           |                                                                 | IEC and SAE level    | G <sup>2</sup> | —          | <sup>1, 3</sup> |

<sup>1</sup> Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>2</sup> G = 48 dB $\mu$ V

<sup>3</sup> Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

<sup>4</sup> “FM on” = FM depth of  $\pm 2\%$

## 4.4 ESD Characteristics

**Table 9. ESD Ratings<sup>1,2</sup>**

| Spec | Characteristic                     | Symbol    | Value                        | Unit |
|------|------------------------------------|-----------|------------------------------|------|
| 1    | ESD for Human Body Model (HBM)     | $V_{HBM}$ | 2000                         | V    |
| 2    | ESD for Charged Device Model (CDM) | $V_{CDM}$ | 750 (corners)<br>500 (other) | V    |

<sup>1</sup> All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 4.5 PMC/POR/LVI Electrical Specifications

**Note:** For ADC internal resource measurements, see Table 21 in Section 4.9.1, “ADC Internal Resource Measurements.”

**Table 10. PMC Operating conditions**

| Name               | Parameter                                                 | Condition           | Min  | Typ | Max  | Unit | Note         |
|--------------------|-----------------------------------------------------------|---------------------|------|-----|------|------|--------------|
| V <sub>DDREG</sub> | Supply voltage VDDREG<br>5V nominal                       | LDO5V / SMPS5V mode | 4.5  | 5   | 5.5  | V    | <sup>1</sup> |
| V <sub>DDREG</sub> | Supply voltage VDDREG<br>3V nominal                       | LDO3V mode          | 3.0  | 3.3 | 3.6  | V    | <sup>1</sup> |
| V <sub>DD33</sub>  | Supply voltage VDDSYN /<br>V <sub>DD33</sub> 3.3V nominal | LDO3V mode          | 3.0  | 3.3 | 3.6  | V    | <sup>2</sup> |
| V <sub>DD</sub>    | Core supply voltage                                       | —                   | 1.14 | 1.2 | 1.32 | V    | <sup>3</sup> |

<sup>1</sup> Voltage should be higher than maximum V<sub>LVDREG</sub> to avoid LVD event

<sup>2</sup> Applies to both V<sub>DD33</sub> (flash supply) and VDDSYN (PLL supply) pads. Voltage should be higher than maximum V<sub>LVD33</sub> to avoid LVD event

<sup>3</sup> Voltage should be higher than maximum V<sub>LVD12</sub> to avoid LVD event

### NOTE

In the following table, "untrimmed" means "at reset" and "trimmed" means "after reset".

**Table 11. PMC Electrical Specifications**

| ID | Name                 | Parameter                                                                                                                                                       | Min                        | Typ                  | Max                        | Unit |
|----|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|----------------------|----------------------------|------|
| 1  | V <sub>BG</sub>      | Nominal bandgap reference voltage                                                                                                                               | 0.608                      | 0.620                | 0.632                      | V    |
| 1a | —                    | Untrimmed bandgap reference voltage                                                                                                                             | V <sub>BG</sub> – 5%       | V <sub>BG</sub>      | V <sub>BG</sub> + 5%       | V    |
| 2  | V <sub>DD12OUT</sub> | Nominal VRC regulated 1.2V output VDD                                                                                                                           | —                          | 1.27                 | —                          | V    |
| 2a | —                    | Untrimmed VRC 1.2V output variation before band gap trim (unloaded)<br><b>Note:</b> Voltage should be higher than maximum V <sub>LVD12</sub> to avoid LVD event | V <sub>DD12OUT</sub> – 14% | V <sub>DD12OUT</sub> | V <sub>DD12OUT</sub> + 10% | V    |
| 2b | —                    | Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max. 1A) <sup>1</sup>                                                    | V <sub>DD12OUT</sub> – 10% | V <sub>DD12OUT</sub> | V <sub>DD12OUT</sub> + 5%  | V    |
| 2c | V <sub>STEPV12</sub> | Trimming step V <sub>DD12OUT</sub>                                                                                                                              | —                          | 10                   | —                          | mV   |
| 3  | V <sub>PORC</sub>    | POR rising VDD 1.2V                                                                                                                                             | —                          | 0.7                  | —                          | V    |
| 3a | —                    | POR VDD 1.2V variation                                                                                                                                          | V <sub>PORC</sub> – 30%    | V <sub>PORC</sub>    | V <sub>PORC</sub> + 30%    |      |
| 3b | —                    | POR 1.2V hysteresis                                                                                                                                             | —                          | 75                   | —                          | mV   |
| 4  | V <sub>LVD12</sub>   | Nominal rising LVD 1.2V<br><b>Note:</b> ~V <sub>DD12OUT</sub> × 0.87                                                                                            | —                          | 1.100                | —                          | V    |
| 4a | —                    | Untrimmed LVD 1.2V variation before band gap trim<br><b>Note:</b> Rising VDD                                                                                    | V <sub>LVD12</sub> – 6%    | V <sub>LVD12</sub>   | V <sub>LVD12</sub> + 6%    | V    |
| 4b | —                    | Trimmed LVD 1.2V variation after band gap trim<br>Rising VDD                                                                                                    | V <sub>LVD12</sub> – 3%    | V <sub>LVD12</sub>   | V <sub>LVD12</sub> + 3%    | V    |

Table 11. PMC Electrical Specifications (continued)

| ID  | Name                   | Parameter                                                                                                                                                                                                                   | Min                       | Typ                  | Max                        | Unit     |
|-----|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|----------------------|----------------------------|----------|
| 4c  | —                      | LVD 1.2V Hysteresis                                                                                                                                                                                                         | 15                        | 20                   | 25                         | mV       |
| 4d  | V <sub>LVDSTEP12</sub> | Trimming step LVD 1.2V                                                                                                                                                                                                      | —                         | 10                   | —                          | mV       |
| 5   | I <sub>REGCTL</sub>    | VRC DC current output on REGCTL                                                                                                                                                                                             | —                         | —                    | 20                         | mA       |
| 6   | —                      | Voltage regulator 1.2V current consumption<br>VDDREG                                                                                                                                                                        | —                         | 3                    | —                          | mA       |
| 7   | V <sub>DD33OUT</sub>   | Nominal V <sub>REG</sub> 3.3V output                                                                                                                                                                                        | —                         | 3.3                  | —                          | V        |
| 7a  | —                      | Untrimmed V <sub>REG</sub> 3.3V output variation before band gap trim (unloaded)<br><b>Note:</b> Rising VDDSYN                                                                                                              | V <sub>DD33OUT</sub> – 6% | V <sub>DD33OUT</sub> | V <sub>DD33OUT</sub> + 10% | V        |
| 7b  | —                      | Trimmed V <sub>REG</sub> 3.3V output variation after band gap trim (max. load 80mA)                                                                                                                                         | V <sub>DD33OUT</sub> – 5% | V <sub>DD33OUT</sub> | V <sub>DD33OUT</sub> + 10% | V        |
| 7c  | V <sub>STEPV33</sub>   | Trimming step VDDSYN                                                                                                                                                                                                        | —                         | 30                   | —                          | mV       |
| 8   | V <sub>LVD33</sub>     | Nominal rising LVD 3.3V<br><b>Note:</b> ~V <sub>DD33OUT</sub> × 0.872                                                                                                                                                       | —                         | 2.950                | —                          | V        |
| 8a  | —                      | Untrimmed LVD 3.3V variation before band gap trim<br><b>Note:</b> Rising VDDSYN                                                                                                                                             | V <sub>LVD33</sub> – 5%   | V <sub>LVD33</sub>   | V <sub>LVD33</sub> + 5%    | V        |
| 8b  | —                      | Trimmed LVD 3.3V variation after bad gap trim<br><b>Note:</b> Rising VDDSYN                                                                                                                                                 | V <sub>LVD33</sub> – 3%   | V <sub>LVD33</sub>   | V <sub>LVD33</sub> + 3%    | V        |
| 8c  | —                      | LVD 3.3V Hysteresis                                                                                                                                                                                                         | —                         | 30                   | —                          | mV       |
| 8d  | V <sub>LVDSTEP33</sub> | Trimming step LVD 3.3V                                                                                                                                                                                                      | —                         | 30                   | —                          | mV       |
| 9   | I <sub>DD33</sub>      | V <sub>REG</sub> = 4.5 V, max DC output current<br>V <sub>REG</sub> = 4.25 V, max DC output current, crank condition<br><b>Note:</b> Max current supplied by VDDSYN that does not cause it to drop below V <sub>LVD33</sub> | —<br>—                    | —<br>—               | 80<br>40                   | mA<br>mA |
| 10  | —                      | Voltage regulator 3.3V current consumption<br>VDDREG<br><b>Note:</b> Except I <sub>DD33</sub>                                                                                                                               | —                         | 2                    | —                          | mA       |
| 11  | V <sub>PORREG</sub>    | POR rising on VDDREG                                                                                                                                                                                                        | —                         | 2.00                 | —                          | V        |
| 11a | —                      | POR VDDREG variation                                                                                                                                                                                                        | V <sub>PORREG</sub> – 30% | V <sub>PORREG</sub>  | V <sub>PORREG</sub> + 30%  | V        |
| 11b | —                      | POR VDDREG hysteresis                                                                                                                                                                                                       | —                         | 250                  | —                          | mV       |
| 12  | V <sub>LVDREG</sub>    | Nominal rising LVD VDDREG<br>(LDO3V / LDO5V mode)                                                                                                                                                                           | —                         | 2.950                | —                          | V        |
| 12a | —                      | Untrimmed LVD VDDREG variation before band gap trim<br><b>Note:</b> Rising VDDREG                                                                                                                                           | V <sub>LVDREG</sub> – 5%  | V <sub>LVDREG</sub>  | V <sub>LVDREG</sub> + 5%   | V        |
| 12b | —                      | Trimmed LVD VDDREG variation after band gap trim<br><b>Note:</b> Rising VDDREG                                                                                                                                              | V <sub>LVDREG</sub> – 3%  | V <sub>LVDREG</sub>  | V <sub>LVDREG</sub> + 3%   | V        |

Table 11. PMC Electrical Specifications (continued)

| ID  | Name                    | Parameter                                                                                                | Min                      | Typ                 | Max                      | Unit |
|-----|-------------------------|----------------------------------------------------------------------------------------------------------|--------------------------|---------------------|--------------------------|------|
| 12c | —                       | LVD VDDREG Hysteresis (LDO3V / LDO5V mode)                                                               | —                        | 30                  | —                        | mV   |
| 12d | V <sub>LVDSTEPREG</sub> | Trimming step LVD VDDREG (LDO3V / LDO5V mode)                                                            | —                        | 30                  | —                        | mV   |
| 13  | V <sub>LVDREG</sub>     | Nominal rising LVD VDDREG (SMPS5V mode)                                                                  | —                        | 4.360               | —                        | V    |
| 13a | —                       | Untrimmed LVD VDDREG variation before band gap trim<br><b>Note:</b> Rising VDDREG                        | V <sub>LVDREG</sub> – 5% | V <sub>LVDREG</sub> | V <sub>LVDREG</sub> + 5% | V    |
| 13b | —                       | Trimmed LVD VDDREG variation after band gap trim<br><b>Note:</b> Rising VDDREG                           | V <sub>LVDREG</sub> – 3% | V <sub>LVDREG</sub> | V <sub>LVDREG</sub> + 3% | V    |
| 13c | —                       | LVD VDDREG Hysteresis (SMPS5V mode)                                                                      | —                        | 50                  | —                        | mV   |
| 13d | V <sub>LVDSTEPREG</sub> | Trimming step LVD VDDREG (SMPS5V mode)                                                                   | —                        | 50                  | —                        | mV   |
| 14  | V <sub>LVDA</sub>       | Nominal rising LVD VDDA                                                                                  | —                        | 4.60                | —                        | V    |
| 14a | —                       | Untrimmed LVD VDDA variation before band gap trim                                                        | V <sub>LVDA</sub> – 5%   | V <sub>LVDA</sub>   | V <sub>LVDA</sub> + 5%   | V    |
| 14b | —                       | Trimmed LVD VDDA variation after band gap trim                                                           | V <sub>LVDA</sub> – 3%   | V <sub>LVDA</sub>   | V <sub>LVDA</sub> + 3%   | V    |
| 14c | —                       | LVD VDDA Hysteresis                                                                                      | —                        | 150                 | —                        | mV   |
| 14d | V <sub>LVDASTEP</sub>   | Trimming step LVD VDDA                                                                                   | —                        | 20                  | —                        | mV   |
| 15  | —                       | SMPS regulator output resistance<br><b>Note:</b> Pulup to VDDREG when high, pulldown to VSSREG when low. | —                        | 15                  | 25                       | Ohm  |
| 16  | —                       | SMPS regulator clock frequency (after reset)                                                             | 1.0                      | 1.5                 | 2.4                      | MHz  |
| 17  | —                       | SMPS regulator overshoot at start-up <sup>2</sup>                                                        | —                        | 1.32                | 1.4                      | V    |
| 18  | —                       | SMPS maximum output current                                                                              | —                        | 1.0                 | —                        | A    |
| 19  | —                       | Voltage variation on current step <sup>2</sup> (20% to 80% of maximum current with 4 usec constant time) | —                        | —                   | 0.1                      | V    |

<sup>1</sup> VRC linear regulator is capable of sourcing a current up to 20 mA and sinking a current up to 500 uA. When using the recommended ballast transistor the maximum output current provided by the voltage regulator VRC/ballast to the VDD core voltage is up to 1A.

<sup>2</sup> Parameter cannot be tested; this value is based on simulation and characterization.

## 4.6 Power Up/Down Sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each  $V_{DDE}/V_{DDEH}$  first and then power up  $V_{DD}$ . For power down, drop  $V_{DD}$  to 0 V first, and then drop all  $V_{DDE}/V_{DDEH}$  supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to [Table 12](#) and [Table 13](#).

**Table 12. Power Sequence Pin States for MH and AE pads**

| VDD  | VDD33 | VDDE | MH Pad                                                                   | MH+LVDS Pads <sup>1</sup> | AE/up-down Pads                       |
|------|-------|------|--------------------------------------------------------------------------|---------------------------|---------------------------------------|
| High | High  | High | Normal operation                                                         | Normal operation          | Normal operation                      |
| —    | Low   | High | Pin is tri-stated (output buffer, input buffer, and weak pulls disabled) | Outputs disabled          | Pull-ups enabled, pull-downs disabled |
| Low  | High  | Low  | Output low, pin unpowered                                                | Outputs disabled          | Output low, pin unpowered             |
| Low  | High  | High | Pin is tri-stated (output buffer, input buffer, and weak pulls disabled) | Outputs disabled          | Pull-ups enabled, pull-downs disabled |

<sup>1</sup> MH+LVDS pads are output-only.

**Table 13. Power Sequence Pin States for F and FS pads**

| VDD  | VDD33 | VDDE | F and FS pads                                                                               |
|------|-------|------|---------------------------------------------------------------------------------------------|
| low  | low   | high | Outputs Disabled                                                                            |
| low  | high  | —    | Outputs Disabled                                                                            |
| high | low   | low  | Outputs Disabled                                                                            |
| high | low   | high | Outputs Disabled                                                                            |
| high | high  | low  | Normal operation - except no drive current and input buffer output is unknown. <sup>1</sup> |
| high | high  | high | Normal Operation                                                                            |

<sup>1</sup> The pad pre-drive circuitry will function normally but since VDDE is unpowered the outputs will not drive high even though the output pmos can be enabled.

### 4.6.1 Power-Up

If  $V_{DDE}/V_{DDEH}$  is powered up first, then a threshold detector tristates all drivers connected to  $V_{DDE}/V_{DDEH}$ . There is no limit to how long after  $V_{DDE}/V_{DDEH}$  powers up before  $V_{DD}$  must power up. If there are multiple  $V_{DDE}/V_{DDEH}$  supplies, they can be powered up in any order. For each  $V_{DDE}/V_{DDEH}$  supply not powered up, the drivers in that  $V_{DDE}/V_{DDEH}$  segment exhibit the characteristics described in the next paragraph.

## Electrical Characteristics

If  $V_{DD}$  is powered up first, then all pads are loaded through the drain diodes to  $V_{DDE}/V_{DDEH}$ . This presents a heavy load that pulls the pad down to a diode above  $V_{SS}$ . Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after  $V_{DD}$  powers up before  $V_{DDE}/V_{DDEH}$  must power up.

The rise times on the power supplies are to be no faster than 25 V/millisecond.

### 4.6.2 Power-Down

If  $V_{DD}$  is powered down first, then all drivers are tristated. There is no limit to how long after  $V_{DD}$  powers down before  $V_{DDE}/V_{DDEH}$  must power down.

If  $V_{DDE}/V_{DDEH}$  is powered down first, then all pads are loaded through the drain diodes to  $V_{DDE}/V_{DDEH}$ . This presents a heavy load that pulls the pad down to a diode above  $V_{SS}$ . Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after  $V_{DDE}/V_{DDEH}$  powers down before  $V_{DD}$  must power down.

There are no limits on the fall times for the power supplies.

### 4.6.3 Power Sequencing and POR Dependent on $V_{DDA}$

During power up or down,  $V_{DDA}$  can lag other supplies (of magnitude greater than  $V_{DDEH}/2$ ) within 1 V to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between  $V_{DDA}$  and  $V_{DDEH}$  is more than 1 V, the following will result:

- Triggers POR (ADC monitors on  $V_{DDEH1}$  segment which powers the RESET pin) if the leakage current path created, when  $V_{DDA}$  is sufficiently low, causes sufficient voltage drop on  $V_{DDEH1}$  node monitored crosses low-voltage detect level.
- If  $V_{DDA}$  is between 0–2 V, powering all the other segments (especially  $V_{DDEH1}$ ) will not be sufficient to get the part out of reset.
- Each  $V_{DDEH}$  will have a leakage current to  $V_{DDA}$  of a magnitude of  $((V_{DDEH} - V_{DDA} - 1 \text{ V (diode drop)})/200 \text{ KOhms})$  up to  $(V_{DDEH}/2 = V_{DDA} + 1 \text{ V})$ .
- Each  $V_{DD}$  has the same behavior; however, the leakage will be small even though there is no current limiting resistor since  $V_{DD} = 1.32 \text{ V max.}$

## 4.7 DC Electrical Specifications

Table 14. DC Electrical Specifications

| Spec | Characteristic                                         | Symbol           | Min               | Max                 | Unit |
|------|--------------------------------------------------------|------------------|-------------------|---------------------|------|
| 1    | Core Supply Voltage (External Regulation)              | $V_{DD}$         | 1.14              | 1.32 <sup>1,2</sup> | V    |
| 1a   | Core Supply Voltage (Internal Regulation) <sup>3</sup> | $V_{DD}$         | 1.08              | 1.32                | V    |
| 2    | I/O Supply Voltage (fast I/O pads)                     | $V_{DDE}$        | 3.0               | 3.6 <sup>1,4</sup>  | V    |
| 3    | I/O Supply Voltage (medium I/O pads)                   | $V_{DDEH}$       | 3.0               | 5.25 <sup>1,5</sup> | V    |
| 4    | 3.3 V I/O Buffer Voltage                               | $V_{DD33}$       | 3.0               | 3.6 <sup>1,4</sup>  | V    |
| 5    | Analog Supply Voltage                                  | $V_{DDA}$        | 4.75              | 5.25 <sup>1,5</sup> | V    |
| 6a   | SRAM Standby Voltage<br>Keep-out Range: 1.2V–2V        | $V_{STBY\_LOW}$  | 0.95 <sup>6</sup> | 1.2                 | V    |
| 6b   | SRAM Standby Voltage<br>Keep-out Range: 1.2V–2V        | $V_{STBY\_HIGH}$ | 2                 | 6                   | V    |
| 7    | Voltage Regulator Control Input Voltage <sup>7</sup>   | $V_{DDREG}$      | 2.7 <sup>8</sup>  | 5.5 <sup>1,5</sup>  | V    |

Table 14. DC Electrical Specifications (continued)

| Spec | Characteristic                                                                                                                                       | Symbol                                    | Min                                              | Max                                              | Unit                 |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|--------------------------------------------------|--------------------------------------------------|----------------------|
| 8    | Clock Synthesizer Operating Voltage <sup>9</sup>                                                                                                     | $V_{DDSYN}$                               | 3.0                                              | 3.6 <sup>1,4</sup>                               | V                    |
| 9    | Fast I/O Input High Voltage<br>Hysteresis enabled<br>Hysteresis disabled                                                                             | $V_{IH\_F}$                               | $0.65 \times V_{DDE}$<br>$0.55 \times V_{DDE}$   | $V_{DDE} + 0.3$                                  | V                    |
| 10   | Fast I/O Input Low Voltage<br>Hysteresis enabled<br>Hysteresis disabled                                                                              | $V_{IL\_F}$                               | $V_{SS} - 0.3$                                   | $0.35 \times V_{DDE}$<br>$0.40 \times V_{DDE}$   | V                    |
| 11   | Medium I/O Input High Voltage<br>Hysteresis enabled<br>Hysteresis disabled                                                                           | $V_{IH\_S}$                               | $0.65 \times V_{DDEH}$<br>$0.55 \times V_{DDEH}$ | $V_{DDEH} + 0.3$                                 | V                    |
| 12   | Medium I/O Input Low Voltage<br>Hysteresis enabled<br>Hysteresis disabled                                                                            | $V_{IL\_S}$                               | $V_{SS} - 0.3$                                   | $0.35 \times V_{DDEH}$<br>$0.40 \times V_{DDEH}$ | V                    |
| 13   | Fast I/O Input Hysteresis                                                                                                                            | $V_{HYS\_F}$                              | $0.1 \times V_{DDE}$                             | —                                                | V                    |
| 14   | Medium I/O Input Hysteresis                                                                                                                          | $V_{HYS\_S}$                              | $0.1 \times V_{DDEH}$                            | —                                                | V                    |
| 15   | Analog Input Voltage                                                                                                                                 | $V_{INDC}$                                | $V_{SSA} - 0.1$                                  | $V_{DDA} + 0.1$                                  | V                    |
| 16   | Fast I/O Output High Voltage <sup>10</sup>                                                                                                           | $V_{OH\_F}$                               | $0.8 \times V_{DDE}$                             | —                                                | V                    |
| 17   | Medium I/O Output High Voltage <sup>11</sup>                                                                                                         | $V_{OH\_S}$                               | $0.8 \times V_{DDEH}$                            | —                                                | V                    |
| 18   | Fast I/O Output Low Voltage <sup>10</sup>                                                                                                            | $V_{OL\_F}$                               | —                                                | $0.2 \times V_{DDE}$                             | V                    |
| 19   | Medium I/O Output Low Voltage <sup>11</sup>                                                                                                          | $V_{OL\_S}$                               | —                                                | $0.2 \times V_{DDEH}$                            | V                    |
| 20   | Load Capacitance (Fast I/O) <sup>12</sup><br>DSC(PCR[8:9]) = 0b00<br>DSC(PCR[8:9]) = 0b01<br>DSC(PCR[8:9]) = 0b10<br>DSC(PCR[8:9]) = 0b11            | $C_L$                                     | —<br>—<br>—<br>—                                 | 10<br>20<br>30<br>50                             | pF<br>pF<br>pF<br>pF |
| 21   | Input Capacitance (Digital Pins)                                                                                                                     | $C_{IN}$                                  | —                                                | 7                                                | pF                   |
| 22   | Input Capacitance (Analog Pins)                                                                                                                      | $C_{IN\_A}$                               | —                                                | 10                                               | pF                   |
| 24   | Operating Current 1.2 V Supplies @ $f_{sys} = 264$ MHz<br>$V_{DD}$ @1.32 V<br>$V_{STBY}$ <sup>13</sup> @1.2 V and 85°C<br>$V_{STBY}$ @6.0 V and 85°C | $I_{DD}$<br>$I_{DDSTBY}$<br>$I_{DDSTBY6}$ | —<br>—<br>—                                      | 850<br>0.10<br>0.15                              | mA<br>mA<br>mA       |
| 25   | Operating Current 3.3 V Supplies @ $f_{sys} = 264$ MHz<br>$V_{DD33}$ <sup>14</sup><br>$V_{DDSYN}$                                                    | $I_{DD33}$<br>$I_{DDSYN}$                 | —<br>—                                           | note <sup>14</sup><br>7 <sup>15</sup>            | mA<br>mA             |
| 26   | Operating Current 5.0 V Supplies @ $f_{sys} = 264$ MHz<br>$V_{DDA}$<br>Analog Reference Supply Current (Transient)<br>$V_{DDREG}$                    | $I_{DDA}$<br>$I_{REF}$<br>$I_{REG}$       | —<br>—<br>—                                      | 50 <sup>16</sup><br>1.0<br>22                    | mA<br>mA<br>mA       |

Table 14. DC Electrical Specifications (continued)

| Spec | Characteristic                                                                                                                                                      | Symbol                                                                                  | Min                             | Max                | Unit                                   |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|---------------------------------|--------------------|----------------------------------------|
| 27   | Operating Current $V_{DDE}/V_{DDEH}$ <sup>17</sup> Supplies<br>$V_{DDE2}$<br>$V_{DDEH1}$<br>$V_{DDEH3}$<br>$V_{DDEH4}$<br>$V_{DDEH5}$<br>$V_{DDEH6}$<br>$V_{DDEH7}$ | $I_{DD2}$<br>$I_{DD1}$<br>$I_{DD3}$<br>$I_{DD4}$<br>$I_{DD5}$<br>$I_{DD6}$<br>$I_{DD7}$ | —<br>—<br>—<br>—<br>—<br>—<br>— | note <sup>17</sup> | mA<br>mA<br>mA<br>mA<br>mA<br>mA<br>mA |
| 28   | Fast I/O Weak Pull Up/Down Current <sup>18</sup><br>3.0 V–3.6 V                                                                                                     | $I_{ACT\_F}$                                                                            | 42                              | 158                | μA                                     |
| 29   | Medium I/O Weak Pull Up/Down Current <sup>19</sup><br>3.0 V–3.6 V<br>4.5 V–5.5 V                                                                                    | $I_{ACT\_S}$                                                                            | 15<br>35                        | 95<br>200          | μA<br>μA                               |
| 30   | I/O Input Leakage Current <sup>20</sup>                                                                                                                             | $I_{INACT\_D}$                                                                          | –2.5                            | 2.5                | μA                                     |
| 31   | DC Injection Current (per pin)                                                                                                                                      | $I_{IC}$                                                                                | –1.0                            | 1.0                | mA                                     |
| 32   | Analog Input Current, Channel Off <sup>21</sup> , AN[0:7], AN38, AN39<br>Analog Input Current, Channel Off, all other analog inputs AN[x]                           | $I_{INACT\_A}$                                                                          | –250<br>–150                    | 250<br>150         | nA<br>nA                               |
| 33   | $V_{SS}$ Differential Voltage                                                                                                                                       | $V_{SS} - V_{SSA}$                                                                      | –100                            | 100                | mV                                     |
| 34   | Analog Reference Low Voltage                                                                                                                                        | $V_{RL}$                                                                                | $V_{SSA}$                       | $V_{SSA} + 100$    | mV                                     |
| 35   | $V_{RL}$ Differential Voltage                                                                                                                                       | $V_{RL} - V_{SSA}$                                                                      | –100                            | 100                | mV                                     |
| 36   | Analog Reference High Voltage                                                                                                                                       | $V_{RH}$                                                                                | $V_{DDA} - 100$                 | $V_{DDA}$          | mV                                     |
| 37   | $V_{REF}$ Differential Voltage                                                                                                                                      | $V_{RH} - V_{RL}$                                                                       | 4.75                            | 5.25               | V                                      |
| 38   | $V_{SSSYN}$ to $V_{SS}$ Differential Voltage                                                                                                                        | $V_{SSSYN} - V_{SS}$                                                                    | –100                            | 100                | mV                                     |
| 39   | Operating Temperature Range—Ambient (Packaged)                                                                                                                      | $T_A$ ( $T_L$ to $T_H$ )                                                                | –40.0                           | 125.0              | °C                                     |
| 40   | Slew rate on power supply pins                                                                                                                                      | —                                                                                       | —                               | 25                 | V/ms                                   |
| 41   | Weak Pull-Up/Down Resistance <sup>22</sup> , 200 K Option                                                                                                           | $R_{PUPD200K}$                                                                          | 130                             | 280                | kΩ                                     |
| 42   | Weak Pull-Up/Down Resistance <sup>22</sup> , 100 K Option                                                                                                           | $R_{PUPD100K}$                                                                          | 65                              | 140                | kΩ                                     |
| 43   | Weak Pull-Up/Down Resistance <sup>22</sup> , 5 K Option                                                                                                             | $R_{PUPD5K}$                                                                            | 1.4                             | 7.5                | kΩ                                     |
| 44   | Pull-Up/Down Resistance Matching Ratios <sup>23</sup> (100K/200K)                                                                                                   | $R_{PUPDMTCH}$                                                                          | –2.5                            | +2.5               | %                                      |

<sup>1</sup> Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

<sup>2</sup> 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

<sup>3</sup> Assumed with DC load.

<sup>4</sup> 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

<sup>5</sup> 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

<sup>6</sup>  $V_{STBY}$  below 0.95 V the RAM will not retain states, but will be operational.  $V_{STBY}$  can be 0 V when bypass standby mode.

<sup>7</sup> Regulator is functional with derated performance, with supply voltage down to 4.0 V for system with  $V_{DDREG} = 4.5$  V (min).

<sup>8</sup> 2.7 V minimum operating voltage allowed during vehicle crank for system with  $V_{DDREG} = 3.0$  V (min). Normal operating voltage should be either  $V_{DDREG} = 3.0$  V (min) or 4.5 V (min) depending on the user regulation voltage system selected.

<sup>9</sup> Required to be supplied when 3.3 V regulator is disabled. See Section 4.5, “PMC/POR/LVI Electrical Specifications.”

- <sup>10</sup>  $I_{OH\_F} = \{16, 32, 47, 77\}$  mA and  $I_{OL\_F} = \{24, 48, 71, 115\}$  mA for {00, 01, 10, 11} drive mode with  $V_{DDE} = 3.0$  V. This spec is for characterization only.
- <sup>11</sup>  $I_{OH\_S} = \{11.6\}$  mA and  $I_{OL\_S} = \{17.7\}$  mA for {medium} I/O with  $V_{DDE} = 4.5$  V;  
 $I_{OH\_S} = \{5.4\}$  mA and  $I_{OL\_S} = \{8.1\}$  mA for {medium} I/O with  $V_{DDE} = 3.0$  V. These specs are for characterization only.
- <sup>12</sup> Applies to D\_CLKOUT, external bus pins, and Nexus pins.
- <sup>13</sup>  $V_{STBY}$  current specified at 1.0 V at a junction temperature of 85 °C.  $V_{STBY}$  current is 700 µA maximum at a junction temperature of 150 °C.
- <sup>14</sup> Power requirements for the  $V_{DD33}$  supply depend on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments. See [Section 4.7.2, “I/O Pad  \$V\_{DD33}\$  Current Specifications,”](#) for information on both fast (F, FS) and medium (MH) pads. Also refer to [Table 16](#) for values to calculate power dissipation for specific operation.
- <sup>15</sup> This value is a target that is subject to change.
- <sup>16</sup> This value allows a 5 V reference to supply ADC + REF.
- <sup>17</sup> Power requirements for each I/O segment depend on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See [Section 4.7.1, “I/O Pad Current Specifications,”](#) for information on I/O pad power. Also refer to [Table 15](#) for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
- <sup>18</sup> Absolute value of current, measured at  $V_{IL}$  and  $V_{IH}$ .
- <sup>19</sup> Absolute value of current, measured at  $V_{IL}$  and  $V_{IH}$ .
- <sup>20</sup> Weak pull up/down inactive. Measured at  $V_{DDE} = 3.6$  V and  $V_{DDEH} = 5.25$  V. Applies to pad types F and MH.
- <sup>21</sup> Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to pad types AE and AE/up-down. See [Appendix A, Signal Properties and Muxing.](#)
- <sup>22</sup> This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics
- <sup>23</sup> Pull-up and pull-down resistances are both enabled and settings are equal.

## 4.7.1 I/O Pad Current Specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from [Table 15](#) based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in [Table 15](#).

The AC timing of these pads are described in the [Section 4.11.2, “Pad AC Specifications.”](#)

**Table 15.  $V_{DDE}/V_{DDEH}$  I/O Pad Average DC Current<sup>1</sup>**

| Spec | Pad Type | Symbol        | Frequency (MHz) | Load <sup>2</sup> (pF) | Voltage (V) | Drive/Slew Rate Select | Current (mA) |
|------|----------|---------------|-----------------|------------------------|-------------|------------------------|--------------|
| 1    | Medium   | $I_{DRV\_MH}$ | 50              | 50                     | 5.25        | 11                     | 16.0         |
| 2    |          |               | 20              | 50                     | 5.25        | 01                     | 6.3          |
| 3    |          |               | 3.0             | 50                     | 5.25        | 00                     | 1.1          |
| 4    |          |               | 2.0             | 200                    | 5.25        | 00                     | 2.4          |
| 5    | Fast     | $I_{DRV\_FC}$ | 66              | 10                     | 3.6         | 00                     | 7.4          |
| 6    |          |               | 66              | 20                     | 3.6         | 01                     | 10.5         |
| 7    |          |               | 66              | 30                     | 3.6         | 10                     | 12.3         |
| 8    |          |               | 66              | 50                     | 3.6         | 11                     | 35.2         |

Table 15.  $V_{DDE}/V_{DDEH}$  I/O Pad Average DC Current<sup>1</sup> (continued)

| Spec | Pad Type             | Symbol         | Frequency (MHz) | Load <sup>2</sup> (pF) | Voltage (V) | Drive/Slew Rate Select | Current (mA) |
|------|----------------------|----------------|-----------------|------------------------|-------------|------------------------|--------------|
| 9    | Fast w/ Slew Control | $I_{DRV\_FSR}$ | 66              | 50                     | 3.6         | 11                     | 12.7         |
| 10   |                      |                | 50              | 50                     | 3.6         | 10                     | 6.7          |
| 11   |                      |                | 33.33           | 50                     | 3.6         | 01                     | 4.2          |
| 12   |                      |                | 20              | 50                     | 3.6         | 00                     | 2.6          |
| 13   |                      |                | 20              | 200                    | 3.6         | 00                     | 9.1          |

<sup>1</sup> These are average IDDE numbers for worst case PVT from simulation. Currents apply to output pins only.

<sup>2</sup> All loads are lumped.

## 4.7.2 I/O Pad $V_{DD33}$ Current Specifications

The power consumption of the  $V_{DD33}$  supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin  $V_{DD33}$  currents for all I/O segments. The  $V_{DD33}$  current draw on fast speed pads can be calculated from Table 16 dependent on the voltage, frequency, and load on all F type pins. The  $V_{DD33}$  current draw on medium pads can be calculated from Table 16 dependent on voltage and independent on the frequency and load on all MH type pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 16.

The AC timing of these pads are described in the Section 4.11.2, “Pad AC Specifications.”

Table 16.  $V_{DD33}$  Pad Average DC Current<sup>1</sup>

| Spec | Pad Type             | Symbol        | Frequency (MHz) | Load <sup>2</sup> (pF) | $V_{DD33}$ (V) | $V_{DDE}$ (V) | Drive/Slew Rate Select | Current (mA) |
|------|----------------------|---------------|-----------------|------------------------|----------------|---------------|------------------------|--------------|
| 1    | Medium               | $I_{33\_MH}$  | —               | —                      | 3.6            | 5.5           | —                      | 0.0007       |
| 2    | Fast                 | $I_{33\_FC}$  | 66              | 10                     | 3.6            | 3.6           | 00                     | 0.92         |
| 3    |                      |               | 66              | 20                     | 3.6            | 3.6           | 01                     | 1.14         |
| 4    |                      |               | 66              | 30                     | 3.6            | 3.6           | 10                     | 1.50         |
| 5    |                      |               | 66              | 50                     | 3.6            | 3.6           | 11                     | 2.19         |
| 6    | Fast w/ Slew Control | $I_{33\_FSR}$ | 66              | 50                     | 3.6            | 3.6           | 11                     | 0.74         |
| 7    |                      |               | 50              | 50                     | 3.6            | 3.6           | 10                     | 0.52         |
| 8    |                      |               | 33.33           | 50                     | 3.6            | 3.6           | 00                     | 0.19         |
| 9    |                      |               | 20              | 50                     | 3.6            | 3.6           | 00                     | 0.19         |
| 10   |                      |               | 20              | 200                    | 3.6            | 3.6           | 00                     | 0.19         |

<sup>1</sup> These are average IDDE for worst case PVT from simulation. Currents apply to output pins only for the fast pads and to input pins only for the medium pads.

<sup>2</sup> All loads are lumped.

### 4.7.3 LVDS Pad Specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol, which is an enhanced feature of the DSPI module.

**Table 17. DSPI LVDS pad specification**

| #                   | Characteristic                                  | Symbol        | Condition        | Min. Value | Typ. Value | Max. Value | Unit |
|---------------------|-------------------------------------------------|---------------|------------------|------------|------------|------------|------|
| <b>Data Rate</b>    |                                                 |               |                  |            |            |            |      |
| 1                   | Data Frequency                                  | $f_{LVDSCLK}$ | —                | —          | 50         | —          | MHz  |
| <b>Driver Specs</b> |                                                 |               |                  |            |            |            |      |
| 2                   | Differential output voltage                     | $V_{OD}$      | SRC=0b00 or 0b11 | 150        | —          | 400        | mV   |
|                     |                                                 |               | SRC=0b01         | 90         | —          | 320        |      |
|                     |                                                 |               | SRC=0b10         | 160        | —          | 480        |      |
| 3                   | Common mode voltage (LVDS), VOS                 | $V_{OS}$      | —                | 1.06       | 1.2        | 1.39       | V    |
| 4                   | Rise/Fall time                                  | $T_R/T_F$     | —                | —          | 2          | —          | ns   |
| 5                   | Propagation delay (Low to High)                 | $T_{PLH}$     | —                | —          | 4          | —          | ns   |
| 6                   | Propagation delay (High to Low)                 | $T_{PHL}$     | —                | —          | 4          | —          | ns   |
| 7                   | Delay (H/L), sync Mode                          | $t_{PDSYNC}$  | —                | —          | 4          | —          | ns   |
| 8                   | Delay, Z to Normal (High/Low)                   | $T_{DZ}$      | —                | —          | 500        | —          | ns   |
| 9                   | Diff Skew $t_{phla-tplhbl}$ or $t_{plhb-tphla}$ | $T_{SKEW}$    | —                | —          | —          | 0.5        | ns   |
| <b>Termination</b>  |                                                 |               |                  |            |            |            |      |
| 10                  | Trans. Line (differential $Z_0$ )               | —             | —                | 95         | 100        | 105        | ohms |
| 11                  | Temperature                                     | —             | —                | −40        | —          | 150        | °C   |

## 4.8 Oscillator and FMPLL Electrical Characteristics

**Table 18. FMPLL Electrical Specifications<sup>1</sup>**

( $V_{DDSYN} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = V_{SSSYN} = 0\text{ V}$ ,  $T_A = T_L\text{ to }T_H$ )

| Spec | Characteristic                                           | Symbol             | Min | Max             | Unit |
|------|----------------------------------------------------------|--------------------|-----|-----------------|------|
| 1    | PLL Reference Frequency Range <sup>2</sup> (Normal Mode) |                    |     |                 | MHz  |
|      | Crystal Reference (PLLCFG2 = 0b0)                        | $f_{ref\_crystal}$ | 8   | 20              |      |
|      | Crystal Reference (PLLCFG2 = 0b1)                        | $f_{ref\_crystal}$ | 16  | 40 <sup>3</sup> |      |
|      | External Reference (PLLCFG2 = 0b0)                       | $f_{ref\_ext}$     | 8   | 20              |      |
|      | External Reference (PLLCFG2 = 0b1)                       | $f_{ref\_ext}$     | 16  | 40              |      |
| 2    | Loss of Reference Frequency <sup>4</sup>                 | $f_{LOR}$          | 100 | 1000            | kHz  |
| 3    | Self Clocked Mode Frequency <sup>5</sup>                 | $f_{SCM}$          | 4   | 16              | MHz  |
| 4    | PLL Lock Time <sup>6</sup>                               | $t_{LPLL}$         | —   | < 400           | μs   |

## Table 18. FMPLL Electrical Specifications<sup>1</sup> (continued)

(V<sub>DDSYN</sub> = 3.0 V to 3.6 V, V<sub>SS</sub> = V<sub>SSSYN</sub> = 0 V, T<sub>A</sub> = T<sub>L</sub> to T<sub>H</sub>)

| Spec | Characteristic                                                                                                | Symbol               | Min   | Max  | Unit                 |
|------|---------------------------------------------------------------------------------------------------------------|----------------------|-------|------|----------------------|
| 5    | Duty Cycle of Reference <sup>7</sup>                                                                          | t <sub>DC</sub>      | 40    | 60   | %                    |
| 6    | Frequency un-LOCK Range                                                                                       | f <sub>UL</sub>      | −4.0  | 4.0  | % f <sub>sys</sub>   |
| 7    | Frequency LOCK Range                                                                                          | f <sub>LCK</sub>     | −2.0  | 2.0  | % f <sub>sys</sub>   |
| 8    | D_CLKOUT Period Jitter <sup>8, 9</sup> Measured at f <sub>sys</sub> Max<br>Cycle-to-cycle Jitter              | C <sub>Jitter</sub>  | −5    | 5    | %f <sub>clkout</sub> |
| 9    | Peak-to-Peak Frequency Modulation Range Limit <sup>10,11</sup><br>(f <sub>sys</sub> Max must not be exceeded) | C <sub>mod</sub>     | 0     | 4    | %f <sub>sys</sub>    |
| 10   | FM Depth Tolerance <sup>12</sup>                                                                              | C <sub>mod_err</sub> | −0.25 | 0.25 | %f <sub>sys</sub>    |
| 11   | VCO Frequency                                                                                                 | f <sub>VCO</sub>     | 192   | 600  | MHz                  |
| 12   | Modulation Rate Limits <sup>13</sup>                                                                          | f <sub>mod</sub>     | 0.400 | 1    | MHz                  |
| 13   | Predivider output frequency range <sup>14</sup>                                                               | f <sub>prediv</sub>  | 4     | 10   | MHz                  |

<sup>1</sup> All values given are initial design targets and subject to change.

<sup>2</sup> Crystal and External reference frequency limits depend on device relying on PLL to lock prior to release of reset, default PREDIV/EPREDIV, MFD/EMFD default settings, and VCO frequency range. Absolute minimum loop frequency is 4 MHz.

<sup>3</sup> Upper tolerance of less than 1% is allowed on 40MHz crystal.

<sup>4</sup> “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

<sup>5</sup> Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f<sub>LOR</sub>. This frequency is measured at D\_CLKOUT. A default RFD value of (0x05) is used in SCM mode, and the programmed MFD and RFD values have no effect

<sup>6</sup> This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

<sup>7</sup> For Flexray operation, duty cycle requirements are higher.

<sup>8</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f<sub>sys</sub>. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V<sub>DDSYN</sub> and V<sub>SSSYN</sub> and variation in crystal oscillator frequency increase the C<sub>Jitter</sub> percentage for a given interval. D\_CLKOUT divider set to divide-by-2.

<sup>9</sup> Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C<sub>Jitter</sub> + C<sub>mod</sub>.

<sup>10</sup> Modulation depth selected must not result in f<sub>p||</sub> value greater than the f<sub>p||</sub> maximum specified value.

<sup>11</sup> Maximum and minimum variation from programmed modulation depth is pending characterization. Depth settings available in control register are: 2%, 3%, and 4% peak-to-peak.

<sup>12</sup> Depth tolerance is the programmed modulation depth ±0.25% of F<sub>sys</sub>. Violating the VCO min/max range may prevent the system from exiting reset.

<sup>13</sup> Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

<sup>14</sup> Violating this range will cause the VCO max/min range to be violated with the default MFD settings out of reset.

**Table 19. Oscillator Electrical Specifications<sup>1</sup>**  
 $(V_{DDSYN} = 3.0 \text{ V to } 3.6 \text{ V}, V_{SS} = V_{SSSYN} = 0 \text{ V}, T_A = T_L \text{ to } T_H)$

| Spec | Characteristic                                                                                        | Symbol                              | Min                                                    | Max                                                                         | Unit |
|------|-------------------------------------------------------------------------------------------------------|-------------------------------------|--------------------------------------------------------|-----------------------------------------------------------------------------|------|
| 1    | Crystal Mode Differential Amplitude <sup>2</sup><br>(Min differential voltage between EXTAL and XTAL) | $V_{\text{crystal\_diff\_amp}}$     | $ V_{\text{extal}} - V_{\text{xtal}}  > 0.4 \text{ V}$ | —                                                                           | V    |
| 2    | Crystal Mode: Internal Differential Amplifier Noise Rejection                                         | $V_{\text{crystal\_diff\_amp\_nr}}$ | —                                                      | $ V_{\text{extal}} - V_{\text{xtal}}  < 0.2 \text{ V}$                      | V    |
| 3    | EXTAL Input High Voltage<br>Bypass mode, External Reference                                           | $V_{\text{IHEXT}}$                  | $((V_{DD33}/2) + 0.4 \text{ V})$                       | —                                                                           | V    |
| 4    | EXTAL Input Low Voltage<br>Bypass mode, External Reference                                            | $V_{\text{ILEXT}}$                  | —                                                      | $(V_{DD33}/2) - 0.4 \text{ V}$                                              | V    |
| 5    | XTAL Current <sup>3</sup>                                                                             | $I_{\text{XTAL}}$                   | 1                                                      | 3                                                                           | mA   |
| 6    | Total On-chip stray capacitance on XTAL                                                               | $C_{\text{S\_XTAL}}$                | —                                                      | 1.5                                                                         | pF   |
| 7    | Total On-chip stray capacitance on EXTAL                                                              | $C_{\text{S\_EXTAL}}$               | —                                                      | 1.5                                                                         | pF   |
| 8    | Crystal manufacturer's recommended capacitive load                                                    | $C_L$                               | See crystal spec                                       | See crystal spec                                                            | pF   |
| 9    | Discrete load capacitance to be connected to EXTAL                                                    | $C_{\text{L\_EXTAL}}$               | —                                                      | $(2 \times C_L - C_{\text{S\_EXTAL}} - C_{\text{PCB\_EXTAL}})$ <sup>4</sup> | pF   |
| 10   | Discrete load capacitance to be connected to XTAL                                                     | $C_{\text{L\_XTAL}}$                | —                                                      | $(2 \times C_L - C_{\text{S\_XTAL}} - C_{\text{PCB\_XTAL}})$ <sup>4</sup>   | pF   |

<sup>1</sup> All values given are initial design targets and subject to change.

<sup>2</sup> This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case,  $V_{\text{extal}} - V_{\text{xtal}} \geq 400 \text{ mV}$  criterion has to be met for oscillator's comparator to produce output clock.

<sup>3</sup>  $I_{\text{xtal}}$  is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

<sup>4</sup>  $C_{\text{PCB\_EXTAL}}$  and  $C_{\text{PCB\_XTAL}}$  are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

## 4.9 eQADC Electrical Characteristics

**Table 20. eQADC Conversion Specifications (Operating)**

| Spec | Characteristic                                                                                                                                                                                                                                                                                          | Symbol             | Min                        | Max                              | Unit             |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|----------------------------|----------------------------------|------------------|
| 1    | ADC Clock (ADCLK) Frequency                                                                                                                                                                                                                                                                             | $f_{\text{ADCLK}}$ | 2                          | 16                               | MHz              |
| 2    | Conversion Cycles<br>Single Ended Conversion Cycles 12 bit resolution<br>Single Ended Conversion Cycles 10 bit resolution<br>Single Ended Conversion Cycles 8 bit resolution<br><b>Note:</b> Differential conversion (min) is one clock cycle less than the single-ended conversion values listed here. | CC                 | 2 + 14<br>2 + 12<br>2 + 10 | 128 + 14<br>128 + 12<br>128 + 10 | ADCLK cycles     |
| 3    | Stop Mode Recovery Time <sup>1</sup>                                                                                                                                                                                                                                                                    | $T_{\text{SR}}$    | 10                         | —                                | $\mu\text{s}$    |
| 4    | Resolution <sup>2</sup>                                                                                                                                                                                                                                                                                 | —                  | 1.25                       | —                                | mV               |
| 5    | INL: 8 MHz ADC Clock <sup>3</sup>                                                                                                                                                                                                                                                                       | INL8               | $-4^4$                     | $4^4$                            | LSB <sup>5</sup> |
| 6    | INL: 16 MHz ADC Clock <sup>3</sup>                                                                                                                                                                                                                                                                      | INL16              | $-8^4$                     | $8^4$                            | LSB              |
| 7    | DNL: 8 MHz ADC Clock <sup>3</sup>                                                                                                                                                                                                                                                                       | DNL8               | $-3^4$                     | $3^4$                            | LSB              |
| 8    | DNL: 16 MHz ADC Clock <sup>3</sup>                                                                                                                                                                                                                                                                      | DNL16              | $-3^4$                     | $3^4$                            | LSB              |

Table 20. eQADC Conversion Specifications (Operating) (continued)

| Spec | Characteristic                                                                                                                                                          | Symbol                                                              | Min                                            | Max                                                                                                                        | Unit        |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-------------|
| 9    | Offset Error without Calibration                                                                                                                                        | OFFNC                                                               | 0 <sup>4</sup>                                 | 100 <sup>4</sup>                                                                                                           | LSB         |
| 10   | Offset Error with Calibration                                                                                                                                           | OFFWC                                                               | -4 <sup>4</sup>                                | 4 <sup>4</sup>                                                                                                             | LSB         |
| 11   | Full Scale Gain Error without Calibration                                                                                                                               | GAINNC                                                              | -120 <sup>4</sup>                              | 0 <sup>4</sup>                                                                                                             | LSB         |
| 12   | Full Scale Gain Error with Calibration                                                                                                                                  | GAINWC                                                              | -4 <sup>4,6</sup>                              | 4 <sup>4,6</sup>                                                                                                           | LSB         |
| 13   | Non-Disruptive Input Injection Current <sup>7, 8, 9, 10</sup>                                                                                                           | I <sub>INJ</sub>                                                    | -3                                             | 3                                                                                                                          | mA          |
| 14   | Incremental Error due to injection current <sup>11, 12</sup>                                                                                                            | E <sub>INJ</sub>                                                    | -4 <sup>4</sup>                                | 4 <sup>4</sup>                                                                                                             | Counts      |
| 15   | TUE value at 8 MHz <sup>13, 14</sup> (with calibration)                                                                                                                 | TUE8                                                                | -4 <sup>4,6</sup>                              | 4 <sup>4,6</sup>                                                                                                           | Counts      |
| 16   | TUE value at 16 MHz <sup>13, 14</sup> (with calibration)                                                                                                                | TUE16                                                               | -8                                             | 8                                                                                                                          | Counts      |
| 17   | Maximum differential voltage <sup>15</sup><br>(DANx+ - DANx-) or (DANx- - DANx+)<br>PREGAIN set to 1X setting<br>PREGAIN set to 2X setting<br>PREGAIN set to 4X setting | DIFF <sub>max</sub><br>DIFF <sub>max2</sub><br>DIFF <sub>max4</sub> | —<br>—<br>—                                    | (V <sub>RH</sub> - V <sub>RL</sub> )/2<br>(V <sub>RH</sub> - V <sub>RL</sub> )/4<br>(V <sub>RH</sub> - V <sub>RL</sub> )/8 | V<br>V<br>V |
| 18   | Differential input Common mode voltage <sup>15</sup><br>(DANx- + DANx+)/2                                                                                               | DIFF <sub>cmv</sub>                                                 | (V <sub>RH</sub> - V <sub>RL</sub> )/2<br>- 5% | (V <sub>RH</sub> - V <sub>RL</sub> )/2<br>+ 5%                                                                             | V           |

<sup>1</sup> Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

<sup>2</sup> At V<sub>RH</sub> - V<sub>RL</sub> = 5.12 V, one count = 1.25 mV without using pregain.

<sup>3</sup> INL and DNL are tested from V<sub>RL</sub> + 50 LSB to V<sub>RH</sub> - 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

<sup>4</sup> New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

<sup>5</sup> At V<sub>RH</sub> - V<sub>RL</sub> = 5.12 V, one LSB = 1.25 mV.

<sup>6</sup> The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

<sup>7</sup> Below disruptive current conditions, the channel being stressed has conversion values of \$3FF for analog inputs greater than V<sub>RH</sub> and \$000 for values less than V<sub>RL</sub>. Other channels are not affected by non-disruptive conditions.

<sup>8</sup> Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

<sup>9</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using V<sub>POSCLAMP</sub> = V<sub>DDA</sub> + 0.5 V and V<sub>NEGCLAMP</sub> = -0.3 V, then use the larger of the calculated values.

<sup>10</sup> Condition applies to two adjacent pins at injection limits.

<sup>11</sup> Performance expected with production silicon.

<sup>12</sup> All channels have same 10 kΩ < R<sub>s</sub> < 100 kΩ Channel under test has R<sub>s</sub> = 10 kΩ, I<sub>INJ</sub> = I<sub>INJMAX</sub> · I<sub>INJMIN</sub>.

<sup>13</sup> The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

<sup>14</sup> TUE does not apply to differential conversions.

<sup>15</sup> Voltages between V<sub>RL</sub> and V<sub>RH</sub> will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

## 4.9.1 ADC Internal Resource Measurements

Table 21. Power Management Control (PMC) Specification

| Spec                   | Characteristic                                             | Symbol       | Min | Typical                                    | Max | Unit |
|------------------------|------------------------------------------------------------|--------------|-----|--------------------------------------------|-----|------|
| <b>PMC Normal Mode</b> |                                                            |              |     |                                            |     |      |
| 1                      | Bandgap 0.62 V<br>ADC0 channel 145                         | $V_{ADC145}$ | —   | 0.62                                       | —   | V    |
| 2                      | Bandgap 1.2 V<br>ADC0 channel 146                          | $V_{ADC146}$ | —   | 1.22                                       | —   | V    |
| 3                      | Vreg1p2 Feedback<br>ADC0 channel 147                       | $V_{ADC147}$ | —   | $V_{DD} / 2.045$                           | —   | V    |
| 4                      | LVD 1.2 V<br>ADC0 channel 180                              | $V_{ADC180}$ | —   | $V_{DD} / 1.774$                           | —   | V    |
| 5                      | Vreg3p3 Feedback<br>ADC0 channel 181                       | $V_{ADC181}$ | —   | $V_{reg3p3} / 5.460$                       | —   | V    |
| 6                      | LVD 3.3 V<br>ADC0 channel 182                              | $V_{ADC182}$ | —   | $V_{reg3p3} / 4.758$                       | —   | V    |
| 7                      | LVD 5.0 V<br>ADC0 channel 183<br>— LDO mode<br>— SMPS mode | $V_{ADC183}$ | —   | $V_{DDREG} / 4.758$<br>$V_{DDREG} / 7.032$ | —   | V    |

Table 22. Standby RAM Regulator Electrical Specifications

| Spec               | Characteristic                                                                                                                         | Symbol       | Min | Typ | Max | Unit |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------|--------------|-----|-----|-----|------|
| <b>Normal Mode</b> |                                                                                                                                        |              |     |     |     |      |
| 1                  | Standby Regulator Output<br>ADC1 channel 194                                                                                           | $V_{ADC194}$ | —   | 1.2 | —   | V    |
| 2                  | Standby Source Bias<br>150 mV to 360 mV (30mV Increment @<br>vref_sel)<br>ADC1 channel 195<br>Default Value 150 mV (@vref_sel = 1 1 1) | $V_{ADC195}$ | 150 | —   | 360 | mV   |
| 3                  | Standby Brownout Reference<br>ADC1 channel 195                                                                                         | $V_{ADC195}$ | 500 | —   | 850 | mV   |

**Table 23. ADC Band Gap Reference / LVI Electrical Specifications**

| Spec | Characteristic                                    | Symbol       | Min   | Typ   | Max   | Unit |
|------|---------------------------------------------------|--------------|-------|-------|-------|------|
| 1    | 4.75 LVD (from $V_{DDA}$ )<br>ADC1 channel 196    | $V_{ADC196}$ | —     | 4.75  | —     | V    |
| 2    | ADC Bandgap<br>ADC0 channel 45<br>ADC1 channel 45 | $V_{ADC45}$  | 1.171 | 1.220 | 1.269 | V    |

**Table 24. Temperature Sensor Electrical Specifications**

| Spec | Characteristic                                                                                                  | Symbol                     | Min | Typ        | Max | Unit   |
|------|-----------------------------------------------------------------------------------------------------------------|----------------------------|-----|------------|-----|--------|
| 1    | Slope<br>–40 °C to 100 °C $\pm 1.0$ °C<br>100 °C to 150 °C $\pm 1.6$ °C<br>ADC0 channel 128<br>ADC1 channel 128 | $V_{SADC128}$ <sup>1</sup> | —   | 5.8        | —   | mV/ °C |
| 2    | Accuracy<br>–40 °C to 150 °C<br>ADC0 channel 128<br>ADC1 channel 128                                            | —                          | —   | $\pm 10.0$ | —   | °C     |

<sup>1</sup> Slope is the measured voltage change per °C.

## 4.10 C90 Flash Memory Electrical Characteristics

**Table 25. Flash Program and Erase Specifications**

| Spec | Characteristic                                  | Symbol            | Min | Typ <sup>1</sup> | Initial Max <sup>2</sup> | Max <sup>3</sup> | Unit    |
|------|-------------------------------------------------|-------------------|-----|------------------|--------------------------|------------------|---------|
| 1    | Double Word (64 bits) Program Time <sup>4</sup> | $t_{dwprogram}$   | —   | 38               | —                        | 500              | $\mu s$ |
| 2    | Page Program Time <sup>4,5</sup>                | $t_{pprogram}$    | —   | 45               | 160                      | 500              | $\mu s$ |
| 3    | 16 KB Block Pre-program and Erase Time          | $t_{16kpperase}$  | —   | 270              | 1000                     | 5000             | ms      |
| 4    | 64 KB Block Pre-program and Erase Time          | $t_{64kpperase}$  | —   | 800              | 1800                     | 5000             | ms      |
| 5    | 128 KB Block Pre-program and Erase Time         | $t_{128kpperase}$ | —   | 1500             | 2600                     | 7500             | ms      |
| 6    | 256 KB Block Pre-program and Erase Time         | $t_{256kpperase}$ | —   | 3000             | 5200                     | 15000            | ms      |

<sup>1</sup> Typical program and erase times assume nominal supply values and operation at 25 °C.

<sup>2</sup> Initial factory condition:  $\leq 100$  program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.

<sup>3</sup> The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

<sup>4</sup> Program times are actual hardware programming times and do not include software overhead.

<sup>5</sup> Page size is 128 bits (4 words).

Table 26. Flash EEPROM Module Life

| Spec | Characteristic                                                                                                                                                                     | Symbol    | Min           | Typical <sup>1</sup> | Unit   |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|---------------|----------------------|--------|
| 1    | Number of program/erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range (T <sub>j</sub> )                                                         | P/E       | 100,000       | —                    | cycles |
| 2    | Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T <sub>j</sub> )                                                       | P/E       | 1,000         | 100,000              | cycles |
| 3    | Minimum Data Retention at 85 °C ambient temperature <sup>2</sup><br>Blocks with 0–1,000 P/E cycles<br>Blocks with 1,001–10,000 P/E cycles<br>Blocks with 10,001–100,000 P/E cycles | Retention | 20<br>10<br>5 | —<br>—<br>—          | years  |

<sup>1</sup> Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

<sup>2</sup> Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 27 shows the Platform Flash Configuration Register 1 (PFCPR1) settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 27. PFCPR1 Settings vs. Frequency of Operation<sup>1</sup>

| Spec                         | Clock Mode        | Maximum Frequency <sup>2</sup> (MHz) |                             | APC = RWSC | WWSC | DPFEN <sup>3</sup> | IPFEN <sup>3</sup> | PFLIM <sup>4</sup>   | BFEN <sup>5</sup> |
|------------------------------|-------------------|--------------------------------------|-----------------------------|------------|------|--------------------|--------------------|----------------------|-------------------|
|                              |                   | Core f <sub>sys</sub>                | Platform f <sub>platf</sub> |            |      |                    |                    |                      |                   |
| 1                            | Enhanced          | 264 MHz <sup>6</sup>                 | 132 MHz <sup>6</sup>        | 0b011      | 0b01 | 0b0<br>0b1         | 0b0<br>0b1         | 0b00<br>0b01<br>0b1x | 0b0<br>0b1        |
| 2                            | Enhanced/<br>Full | 200 MHz                              | 100 MHz                     | 0b010      | 0b01 | 0b0<br>0b1         | 0b0<br>0b1         | 0b00<br>0b01<br>0b1x | 0b0<br>0b1        |
| 3                            | Legacy            | 132 MHz                              | 132 MHz                     | 0b100      | 0b01 | 0b0<br>0b1         | 0b0<br>0b1         | 0b00<br>0b01<br>0b1x | 0b0<br>0b1        |
| Default setting after reset: |                   |                                      |                             | 0b111      | 0b11 | 0b00               | 0b00               | 0b00                 | 0b0               |

<sup>1</sup> Illegal combinations exist. Use entries from the same row in this table.

<sup>2</sup> This is the nominal maximum frequency of operation: platform runs at f<sub>sys</sub>/2 in Enhanced Mode .

<sup>3</sup> For maximum flash performance, set to 0b1.

<sup>4</sup> For maximum flash performance, set to 0b10.

<sup>5</sup> For maximum flash performance, set to 0b1.

<sup>6</sup> This is the nominal maximum frequency of operation in Enhanced Mode. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system core clock(f<sub>sys</sub>) + 2% FM and 132 Mhz platform clock (f<sub>platf</sub>) + 2% FM.

## 4.11 AC Specifications

### 4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.

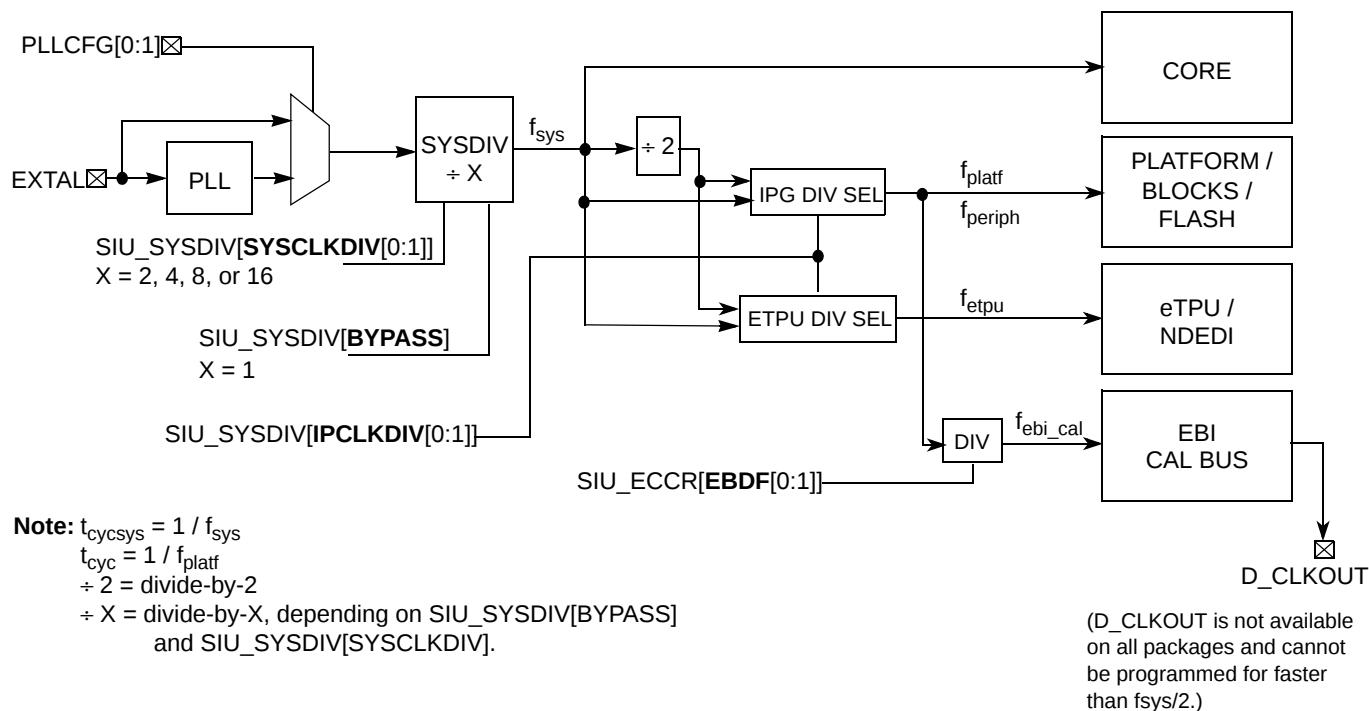


Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 28 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 29 and Table 30 for descriptions of bit settings).

Table 28. MPC5674F Operating Frequencies<sup>1, 2</sup>

| Mode     | SIU_ECCR [EBDF[0:1]] <sup>3</sup> | $f_{sys}$ (core) | $f_{platf}$ (platform and all blocks except eTPU) | $f_{etpu}$ (eTPU, eTPU RAM, and NDEDI) | $f_{ebi\_cal}$ <sup>4,5</sup> | Unit |
|----------|-----------------------------------|------------------|---------------------------------------------------|----------------------------------------|-------------------------------|------|
| Enhanced | 01                                | 264              | 132                                               | 132                                    | 66                            | MHz  |
|          | 11                                | 264              | 132                                               | 132                                    | 33                            |      |
| Full     | 01                                | 200              | 100                                               | 200                                    | 50                            | MHz  |
|          | 11                                | 200              | 100                                               | 200                                    | 25                            |      |
| Legacy   | 01                                | 132              | 132                                               | 132                                    | 66                            | MHz  |
|          | 11                                | 132              | 132                                               | 132                                    | 33                            |      |

<sup>1</sup> The values in the table are specified at:  
 $V_{DD} = 1.02 \text{ V to } 1.32 \text{ V}$   
 $V_{DDE} = 3.0 \text{ V to } 3.6 \text{ V}$   
 $V_{DDEH} = 4.5 \text{ V to } 5.5 \text{ V}$   
 $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V to } 3.6 \text{ V}$   
 $T_A = T_L \text{ to } T_H$ .

- <sup>2</sup> Up to the maximum frequency rating of the device (refer to [Table 1](#)). The  $f_{sys}$  speed is the nominal maximum frequency. 270 Mhz parts allow for 264 Mhz system clock + 2% FM.
- <sup>3</sup> See the *MPC5674F Reference Manual* for full description as not all bit combinations are valid.
- <sup>4</sup> EBI/Calibration bus is not available in all packages.
- <sup>5</sup> The EBI/Calibration Bus operating frequency,  $f_{ebi\_cal}$ , depends on clock divider settings of block's max allowed frequency of operation. Normally  $f_{ebi\_cal} = f_{platf} / 2$ , but can be limited to  $< f_{platf} / 2$  in Full Mode.

**Table 29. IPCLKDIV Settings**

| SIU_SYSDIV<br>[IPCLKDIV[0:1]] | Mode     | Description                                                                                              |
|-------------------------------|----------|----------------------------------------------------------------------------------------------------------|
| 00                            | Enhanced | CPU frequency is doubled (Max 264Mhz). Platform, peripheral, and eTPU clocks are 1/2 of CPU frequency    |
| 01                            | Full     | CPU and eTPU frequency is doubled (Max 200Mhz). Platform and peripheral clocks are 1/2 of CPU frequency. |
| 10                            | —        | Reserved                                                                                                 |
| 11                            | Legacy   | CPU, eTPU, platform, and peripheral's clocks all run at same speed (Max 132Mhz).                         |

**Table 30. SYCLKDIV Settings**

| SIU_SYSDIV<br>[SYCLKDIV[0:1]] | Description   |
|-------------------------------|---------------|
| 00                            | Divide by 2.  |
| 01                            | Divide by 4.  |
| 10                            | Divide by 8.  |
| 11                            | Divide by 16. |

## 4.11.2 Pad AC Specifications

Table 31. Pad AC Specifications ( $V_{DDEH} = 5.0\text{ V}$ ,  $V_{DDE} = 3.3\text{ V}$ )<sup>1</sup>

| Spec | Pad                       | SRC/DSC | Out Delay <sup>2,4</sup><br>L → H/H → L (ns) | Rise/Fall <sup>3,4</sup><br>(ns) | Load Drive<br>(pF) |
|------|---------------------------|---------|----------------------------------------------|----------------------------------|--------------------|
| 1    | Medium <sup>5</sup>       | 00      | 152/165                                      | 70/74                            | 50                 |
| 2    |                           |         | 205/220                                      | 96/96                            | 200                |
| 3    |                           | 01      | 28/34                                        | 12/15                            | 50                 |
| 4    |                           |         | 52/59                                        | 28/31                            | 200                |
| 5    |                           | 11      | 12/12                                        | 5.3/5.9                          | 50                 |
| 6    |                           |         | 32/32                                        | 22/22                            | 200                |
| 7    | Fast <sup>6</sup>         | 00      | 2.5                                          | 1.2                              | 10                 |
| 8    |                           | 01      |                                              |                                  | 20                 |
| 9    |                           | 10      |                                              |                                  | 30                 |
| 10   |                           | 11      |                                              |                                  | 50                 |
| 11   | Fast with Slew Rate       | 00      | 40/40                                        | 16/16                            | 50                 |
| 12   |                           |         | 50/50                                        | 21/21                            | 200                |
| 13   |                           | 01      | 13/13                                        | 5/5                              | 50                 |
| 14   |                           |         | 19/19                                        | 8/8                              | 200                |
| 15   |                           | 10      | 8/8                                          | 2.4/2.4                          | 50                 |
| 16   |                           |         | 12/12                                        | 5/5                              | 200                |
| 17   |                           | 11      | 5/5                                          | 1.1/1/1                          | 50                 |
| 18   |                           |         | 8/8                                          | 2.6                              | 2.6                |
| 19   | Pull Up/Down (3.6 V max)  | —       | —                                            | 7500                             | 50                 |
| 20   | Pull Up/Down (5.25 V max) | —       | 6000                                         | 5000/5000                        | 50                 |

<sup>1</sup> These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at  $V_{DD} = 1.02\text{ V}$  to  $1.32\text{ V}$ ,  $V_{DDE} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $V_{DDEH} = 4.75\text{ V}$  to  $5.25\text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $T_A = T_L$  to  $T_H$ .

<sup>2</sup> This parameter is supplied for reference and is not guaranteed by design and not tested.

<sup>3</sup> This parameter is guaranteed by characterization before qualification rather than 100% tested.

<sup>4</sup> Delay and rise/fall are measured to 20% or 80% of the respective signal.

<sup>5</sup> Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

<sup>6</sup> Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 32. Derated Pad AC Specifications ( $V_{DDEH} = 3.3 \text{ V}$ )<sup>1</sup>

| Spec | Pad                 | SRC/DSC | Out Delay <sup>2,3</sup><br>L → H/H → L (ns) | Rise/Fall <sup>4,3</sup><br>(ns) | Load Drive<br>(pF) |
|------|---------------------|---------|----------------------------------------------|----------------------------------|--------------------|
| 1    | Medium <sup>5</sup> | 00      | 200/210                                      | 86/86                            | 50                 |
| 2    |                     |         | 270/285                                      | 120/120                          | 200                |
| 3    |                     | 01      | 37/45                                        | 15.5/19                          | 50                 |
| 4    |                     |         | 69/82                                        | 38/43                            | 200                |
| 5    |                     | 11      | 18/17                                        | 7.6/8.5                          | 50                 |
| 6    |                     |         | 46/49                                        | 30/34                            | 200                |

<sup>1</sup> These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at  $V_{DD} = 1.08 \text{ V}$  to  $1.32 \text{ V}$ ,  $V_{DDE} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ ,  $V_{DDEH} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ ,  $T_A = T_L$  to  $T_H$ .

<sup>2</sup> This parameter is supplied for reference and is not guaranteed by design and not tested.

<sup>3</sup> Delay and rise/fall are measured to 20% or 80% of the respective signal.

<sup>4</sup> This parameter is guaranteed by characterization before qualification rather than 100% tested.

<sup>5</sup> Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

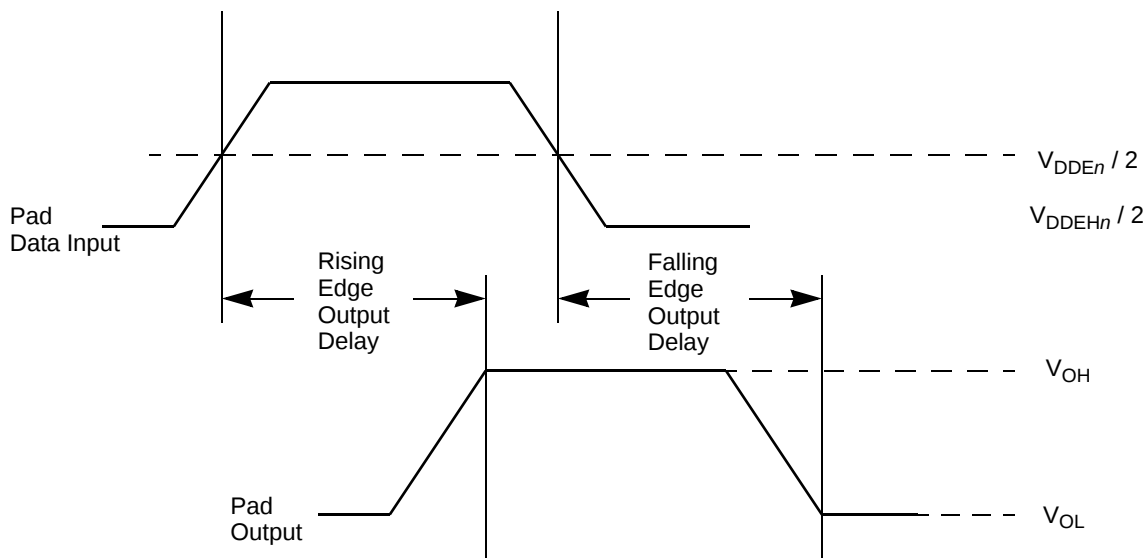
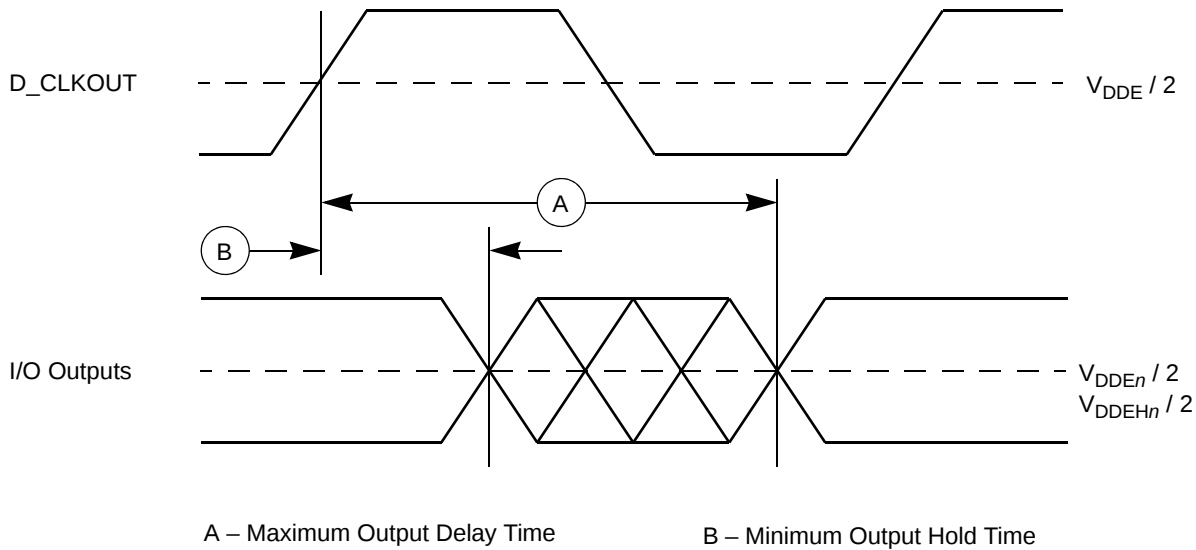


Figure 17. Pad Output Delay

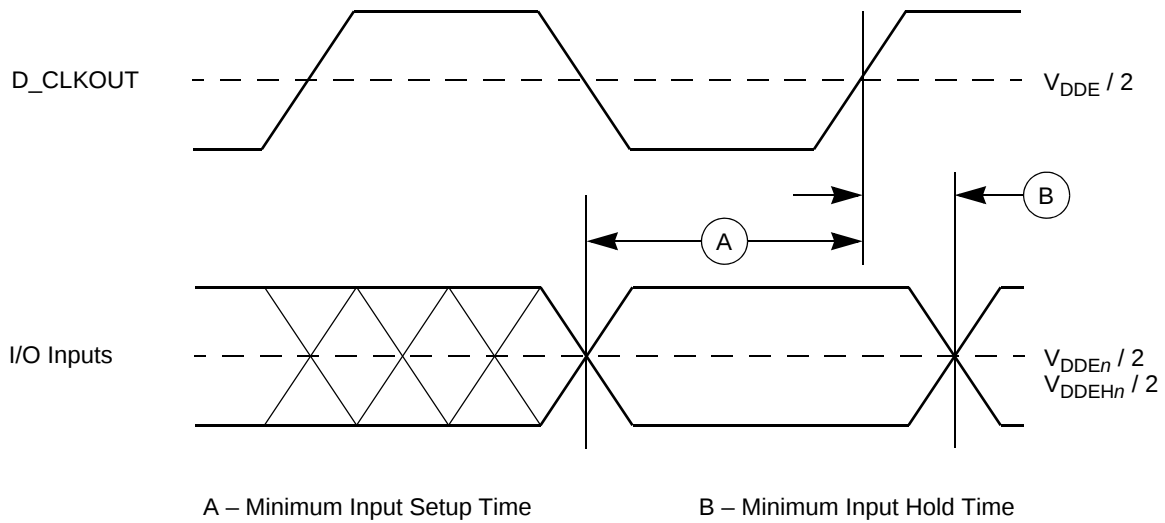
## 4.12 AC Timing

### 4.12.1 Generic Timing Diagrams

The generic timing diagrams in Figure 18 and Figure 19 apply to all I/O pins with pad types F and MH. See Appendix A, Signal Properties and Muxing, for the pad type for each pin.



**Figure 18. Generic Output Delay/Hold Timing**



**Figure 19. Generic Input Setup/Hold Timing**

## 4.12.2 Reset and Configuration Pin Timing

**Table 33. Reset and Configuration Pin Timing<sup>1</sup>**

| Spec | Characteristic                                     | Symbol     | Min | Max | Unit        |
|------|----------------------------------------------------|------------|-----|-----|-------------|
| 1    | RESET Pulse Width                                  | $t_{RPW}$  | 10  | —   | $t_{cyc}^2$ |
| 2    | RESET Glitch Detect Pulse Width                    | $t_{GPW}$  | 2   | —   | $t_{cyc}^2$ |
| 3    | PLLCFG, BOOTCFG, WKPCFG Setup Time to RSTOUT Valid | $t_{RCSU}$ | 10  | —   | $t_{cyc}^2$ |
| 4    | PLLCFG, BOOTCFG, WKPCFG Hold Time to RSTOUT Valid  | $t_{RCH}$  | 0   | —   | $t_{cyc}^2$ |

<sup>1</sup> Reset timing specified at:  $V_{DDEH} = 3.0 \text{ V to } 5.25 \text{ V}$ ,  $V_{DD} = 1.08 \text{ V to } 1.32 \text{ V}$ ,  $T_A = T_L \text{ to } T_H$ .

<sup>2</sup> See Notes on  $t_{\text{CYC}}$  on Figure 16 and Table 28 in Section 4.11.1, “Clocking.”

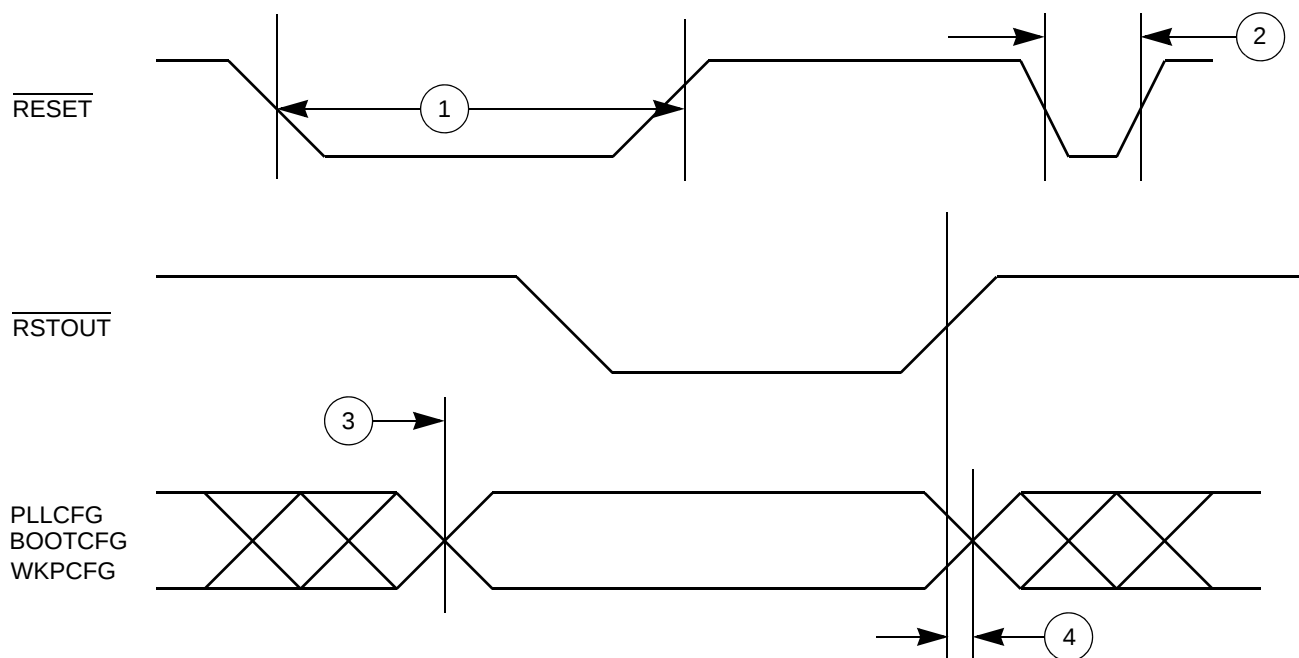


Figure 20. Reset and Configuration Pin Timing

### 4.12.3 IEEE 1149.1 Interface Timing

Table 34. JTAG Pin AC Electrical Characteristics<sup>1</sup>

| Spec | Characteristic                                            | Symbol                             | Min | Max | Unit |
|------|-----------------------------------------------------------|------------------------------------|-----|-----|------|
| 1    | TCK Cycle Time                                            | $t_{\text{JCYC}}$                  | 100 | —   | ns   |
| 2    | TCK Clock Pulse Width (Measured at $V_{\text{DDE}} / 2$ ) | $t_{\text{JDC}}$                   | 40  | 60  | ns   |
| 3    | TCK Rise and Fall Times (40%–70%)                         | $t_{\text{TCKRISE}}$               | —   | 3   | ns   |
| 4    | TMS, TDI Data Setup Time                                  | $t_{\text{TMSS}}, t_{\text{TDIS}}$ | 5   | —   | ns   |
| 5    | TMS, TDI Data Hold Time                                   | $t_{\text{TMSH}}, t_{\text{TDIH}}$ | 25  | —   | ns   |
| 6    | TCK Low to TDO Data Valid                                 | $t_{\text{TDOV}}$                  | —   | 10  | ns   |
| 7    | TCK Low to TDO Data Invalid                               | $t_{\text{TDOI}}$                  | 0   | —   | ns   |
| 8    | TCK Low to TDO High Impedance                             | $t_{\text{TDOHZ}}$                 | —   | 20  | ns   |
| 9    | JCOMP Assertion Time                                      | $t_{\text{JCMPPW}}$                | 100 | —   | ns   |
| 10   | JCOMP Setup Time to TCK Low                               | $t_{\text{JCMPs}}$                 | 40  | —   | ns   |
| 11   | TCK Falling Edge to Output Valid                          | $t_{\text{BSDV}}$                  | —   | 50  | ns   |
| 12   | TCK Falling Edge to Output Valid out of High Impedance    | $t_{\text{BSDVZ}}$                 | —   | 50  | ns   |
| 13   | TCK Falling Edge to Output High Impedance                 | $t_{\text{BSDHZ}}$                 | —   | 50  | ns   |
| 14   | Boundary Scan Input Valid to TCK Rising Edge              | $t_{\text{BSDST}}$                 | 50  | —   | ns   |
| 15   | TCK Rising Edge to Boundary Scan Input Invalid            | $t_{\text{BSDHT}}$                 | 50  | —   | ns   |

## Electrical Characteristics

<sup>1</sup> JTAG timing specified at  $V_{DD} = 1.08 \text{ V to } 1.32 \text{ V}$ ,  $V_{DDE} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $T_A = T_L \text{ to } T_H$ , and  $C_L = 30 \text{ pF}$  with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See [Table 35](#) for functional specifications.

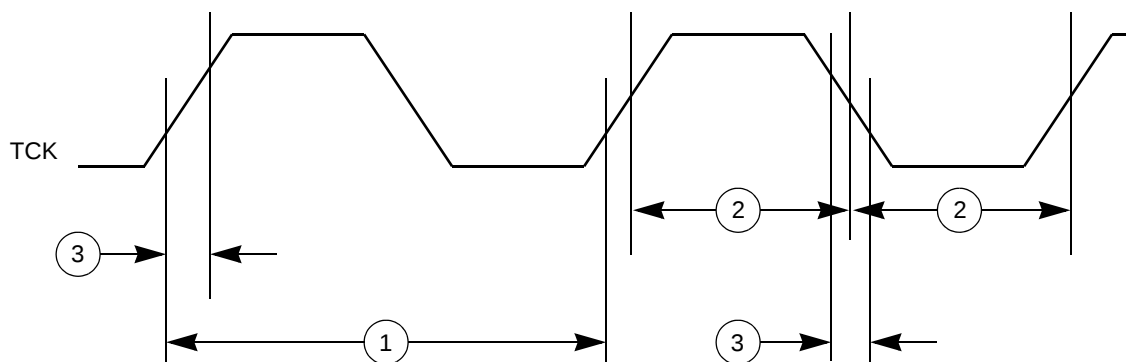


Figure 21. JTAG Test Clock Input Timing

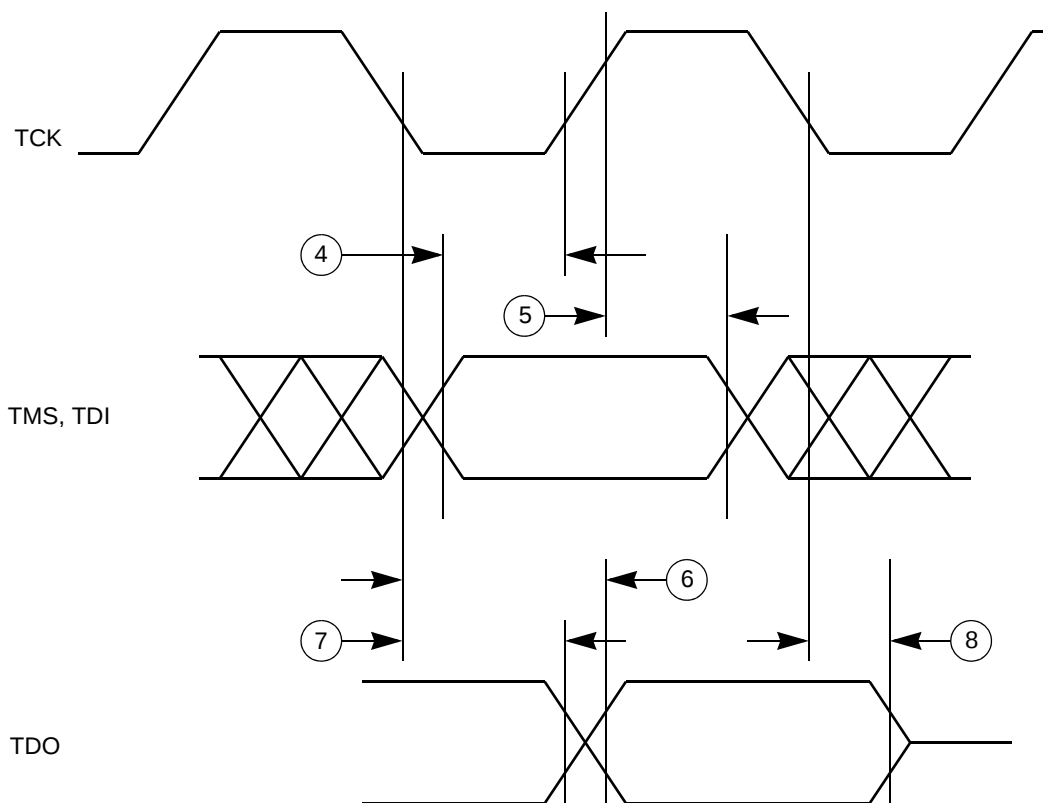


Figure 22. JTAG Test Access Port Timing

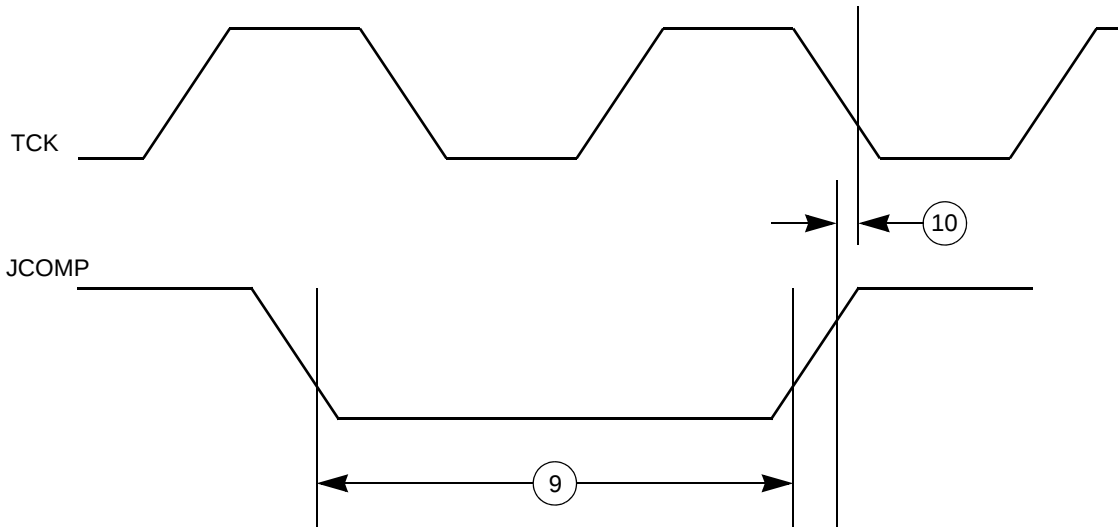


Figure 23. JTAG JCOMP Timing

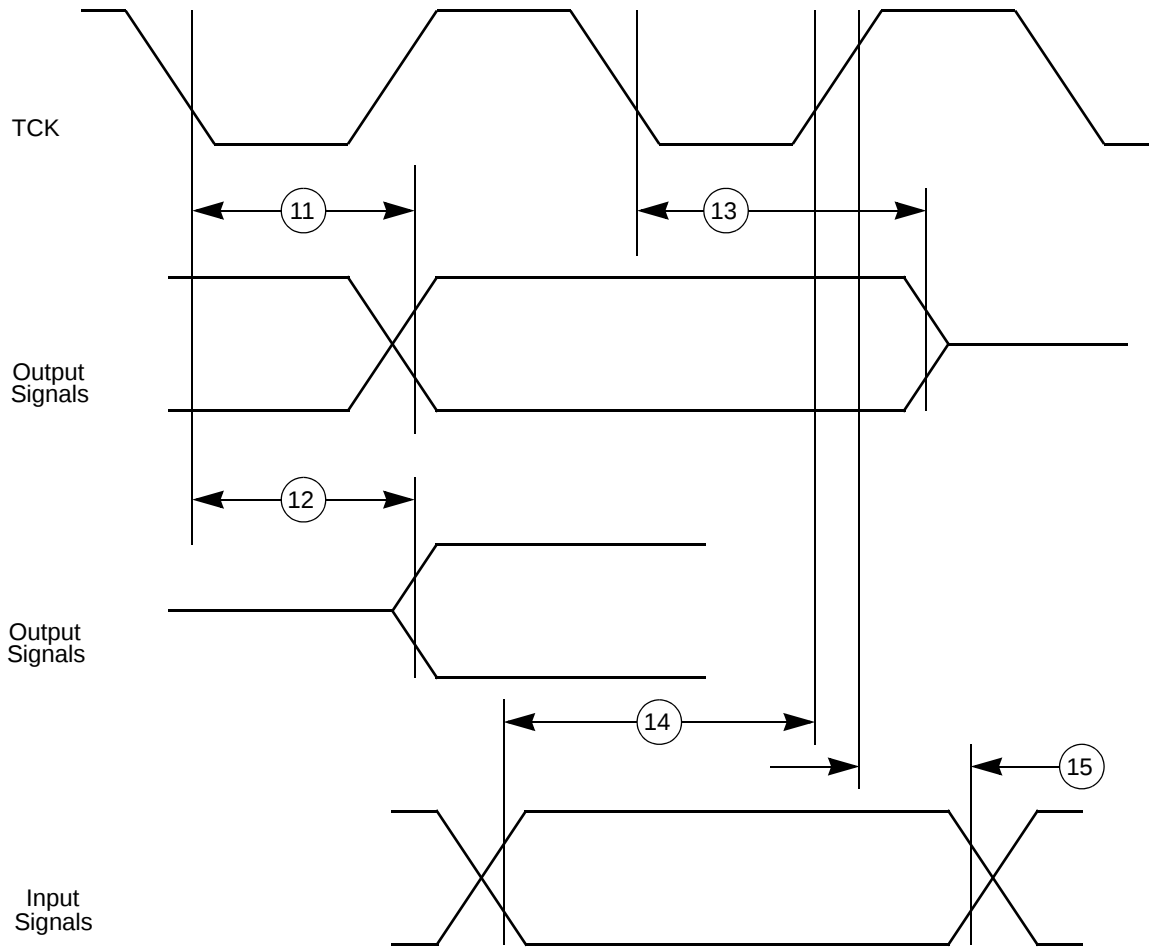


Figure 24. JTAG Boundary Scan Timing

## 4.12.4 Nexus Timing

Table 35. Nexus Debug Port Timing<sup>1</sup>

| Spec | Characteristic                           | Symbol                 | Min            | Max | Unit                    |
|------|------------------------------------------|------------------------|----------------|-----|-------------------------|
| 1    | MCKO Cycle Time                          | $t_{MCYC}$             | 2 <sup>2</sup> | 8   | $t_{CYC}$ <sup>3</sup>  |
| 2    | MCKO Duty Cycle                          | $t_{MDC}$              | 40             | 60  | %                       |
| 3    | MCKO Low to MDO Data Valid <sup>4</sup>  | $t_{MDOV}$             | -0.1           | 0.2 | $t_{MCYC}$              |
| 4    | MCKO Low to MSEO Data Valid <sup>4</sup> | $t_{MSEOV}$            | -0.1           | 0.2 | $t_{MCYC}$              |
| 5    | MCKO Low to EVTO Data Valid <sup>4</sup> | $t_{EVTOV}$            | -0.1           | 0.2 | $t_{MCYC}$              |
| 6    | EVTI Pulse Width                         | $t_{EVTIPW}$           | 4.0            | —   | $t_{TCYC}$ <sup>3</sup> |
| 7    | EVTO Pulse Width                         | $t_{EVTOPW}$           | 1              | —   | $t_{MCYC}$              |
| 8    | TCK Cycle Time                           | $t_{TCYC}$             | 4 <sup>5</sup> | —   | $t_{CYC}$ <sup>3</sup>  |
| 9    | TCK Duty Cycle                           | $t_{TDC}$              | 40             | 60  | %                       |
| 10   | TDI, TMS Data Setup Time                 | $t_{NTDIS}, t_{NTMSS}$ | 8              | —   | ns                      |
| 11   | TDI, TMS Data Hold Time                  | $T_{NTDIH}, t_{NTMSH}$ | 5              | —   | ns                      |
| 12   | TCK Low to TDO Data Valid                | $t_{NTDOV}$            | 0              | 10  | ns                      |
| 13   | RDY Valid to MCKO <sup>6</sup>           | —                      | —              | —   | —                       |

<sup>1</sup> All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at  $V_{DD} = 1.08\text{ V}$  to  $1.32\text{ V}$ ,  $V_{DDE} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $T_A = T_L$  to  $T_H$ , and  $C_L = 30\text{ pF}$  with  $DSC = 0b10$ .

<sup>2</sup> The Nexus AUX port runs up to 82 MHz (pending characterization). Set NPC\_PCR[MKCO\_DIV] to correct division depending on the system frequency, not to exceed maximum Nexus AUX port frequency.

<sup>3</sup> See Notes on  $t_{cyc}$  in Table 28 in Section 4.11.1 Clocking.

<sup>4</sup> MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.

<sup>5</sup> Lower frequency is required to be fully compliant to standard.

<sup>6</sup> The RDY pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

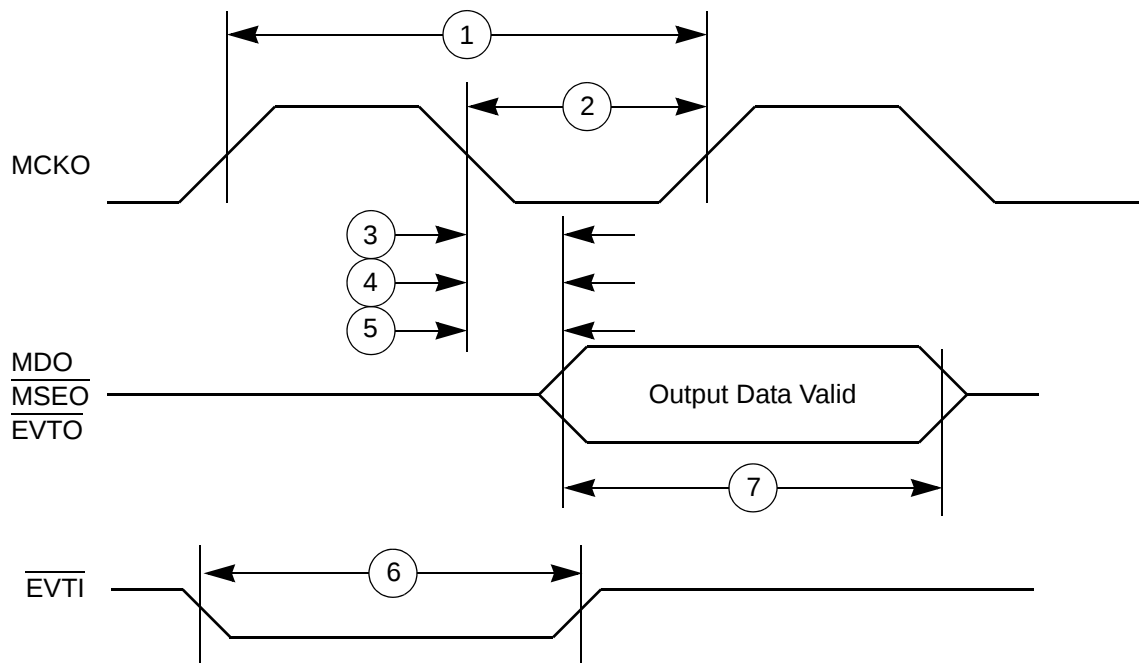


Figure 25. Nexus Timings

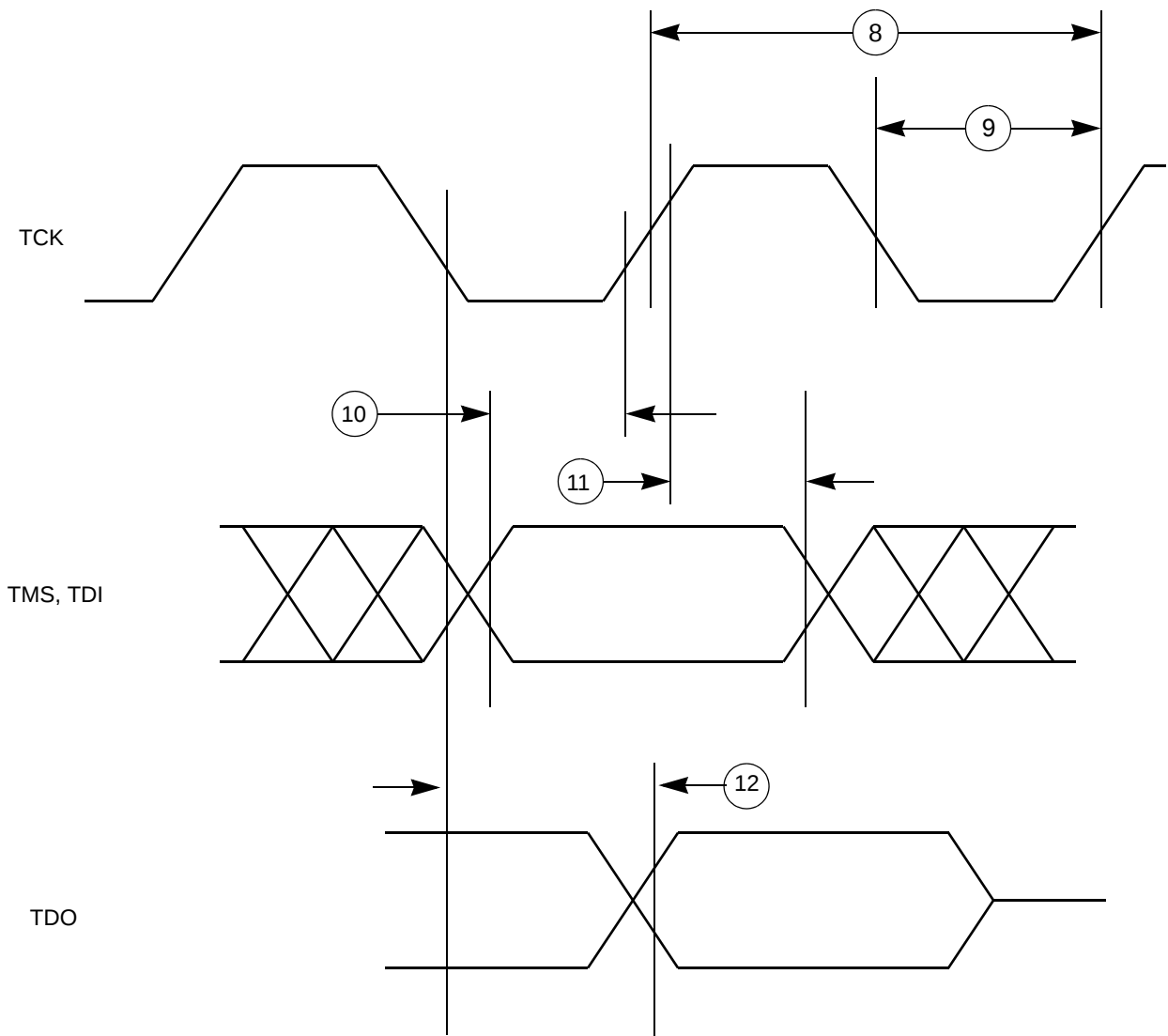


Figure 26. Nexus TCK, TDI, TMS, TDO Timing

## 4.12.5 External Bus Interface (EBI) Timing

Table 36. Bus Operation Timing <sup>1</sup>

| Spec | Characteristic                                                                                                                                                                     | Symbol    | 66 MHz (Ext. Bus Freq) <sup>2 3</sup> |                | Unit  | Notes                                                                                        |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|---------------------------------------|----------------|-------|----------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                    |           | Min                                   | Max            |       |                                                                                              |
| 1    | D_CLKOUT Period                                                                                                                                                                    | $t_C$     | 15.2                                  | —              | ns    | Signals are measured at 50% $V_{DDE}$ .                                                      |
| 2    | D_CLKOUT Duty Cycle                                                                                                                                                                | $t_{CDC}$ | 45%                                   | 55%            | $t_C$ |                                                                                              |
| 3    | D_CLKOUT Rise Time                                                                                                                                                                 | $t_{CRT}$ | —                                     | — <sup>4</sup> | ns    |                                                                                              |
| 4    | D_CLKOUT Fall Time                                                                                                                                                                 | $t_{CFT}$ | —                                     | — <sup>4</sup> | ns    |                                                                                              |
| 5    | D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time)<br><br>D_ADD[9:30]<br>D_BDIP<br>D_CS[0:3]<br>D_DAT[0:15]<br>D_OE<br>D_RD_WR<br>D_TA<br>D_TS<br>D_WE[0:3]/D_BE[0:3] | $t_{COH}$ | 1.0/1.5                               | —              | ns    | Hold time selectable via SIU_ECCR[EBTS] bit:<br>EBTS = 0: 1.0 ns<br>EBTS = 1: 1.5 ns         |
| 6    | D_CLKOUT Posedge to Output Signal Valid (Output Delay)<br><br>D_ADD[9:30]<br>D_BDIP<br>D_CS[0:3]<br>D_DAT[0:15]<br>D_OE<br>D_RD_WR<br>D_TA<br>D_TS<br>D_WE[0:3]/D_BE[0:3]          | $t_{COV}$ | —                                     | 7.0/7.5        | ns    | Output valid time selectable via SIU_ECCR[EBTS] bit:<br>EBTS = 0: 7.0 ns<br>EBTS = 1: 7.5 ns |

Table 36. Bus Operation Timing <sup>1</sup> (continued)

| Spec | Characteristic                                                                                                    | Symbol    | 66 MHz (Ext. Bus Freq) <sup>2 3</sup> |     | Unit | Notes                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------|-----------|---------------------------------------|-----|------|-------------------------------------------------------------------------------------------|
|      |                                                                                                                   |           | Min                                   | Max |      |                                                                                           |
| 7    | Input Signal Valid to D_CLKOUT Posedge (Setup Time)<br><br>D_ADD[9:30]<br>D_DAT[0:15]<br>D_RD_WR<br>D_TA<br>D_TS  | $t_{CIS}$ | 5.0/4.5                               | —   | ns   | Input setup time selectable via SIU_ECCR[EBTS] bit:<br>EBTS = 0; 5.0ns<br>EBTS = 1; 4.5ns |
| 8    | D_CLKOUT Posedge to Input Signal Invalid (Hold Time)<br><br>D_ADD[9:30]<br>D_DAT[0:15]<br>D_RD_WR<br>D_TA<br>D_TS | $t_{CIH}$ | 1.0                                   | —   | ns   |                                                                                           |
| 9    | D_ALE Pulse Width                                                                                                 | $t_{APW}$ | 6.5                                   | —   | ns   | The timing is for Asynchronous external memory system.                                    |
| 10   | D_ALE Negated to Address Invalid                                                                                  | $t_{AAI}$ | 2.0/1.0 <sup>5</sup>                  | —   | ns   | The timing is for Asynchronous external memory system.<br>ALE is measured at 50% of VDDE. |

<sup>1</sup> EBI timing specified at  $V_{DD} = 1.08 \text{ V}$  to  $1.32 \text{ V}$ ,  $V_{DDE} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ ,  $T_A = T_L$  to  $T_H$ , and  $C_L = 30 \text{ pF}$  with DSC = 0b10.

<sup>2</sup> Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

<sup>3</sup> Depending on the internal bus speed, set the SIU\_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.

<sup>4</sup> Refer to Fast pad timing in Table 31 and Table 32.

<sup>5</sup> ALE hold time spec is temperature dependant. 1.0 ns spec applies for temperature range -40 to 0 °C. 2.0 ns spec applies to temperatures > 0 °C. This spec has no dependency on SIU\_ECCR[EBTS] bit.

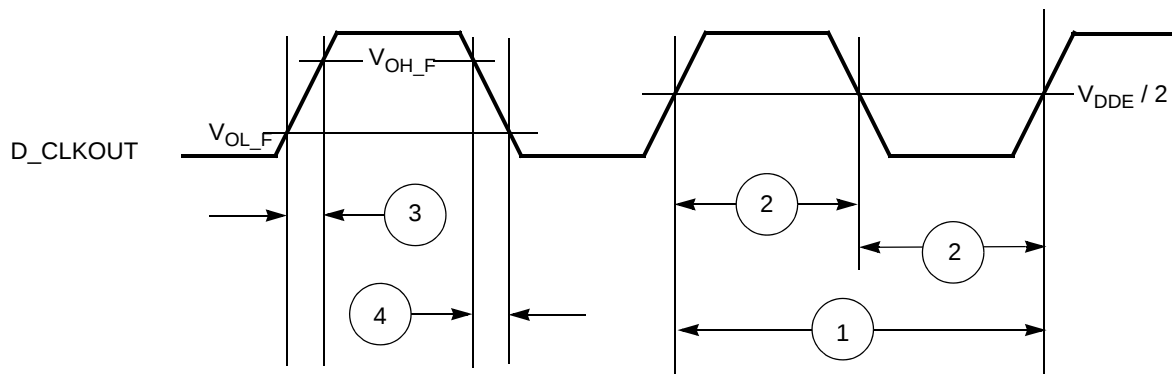


Figure 27. D\_CLKOUT Timing

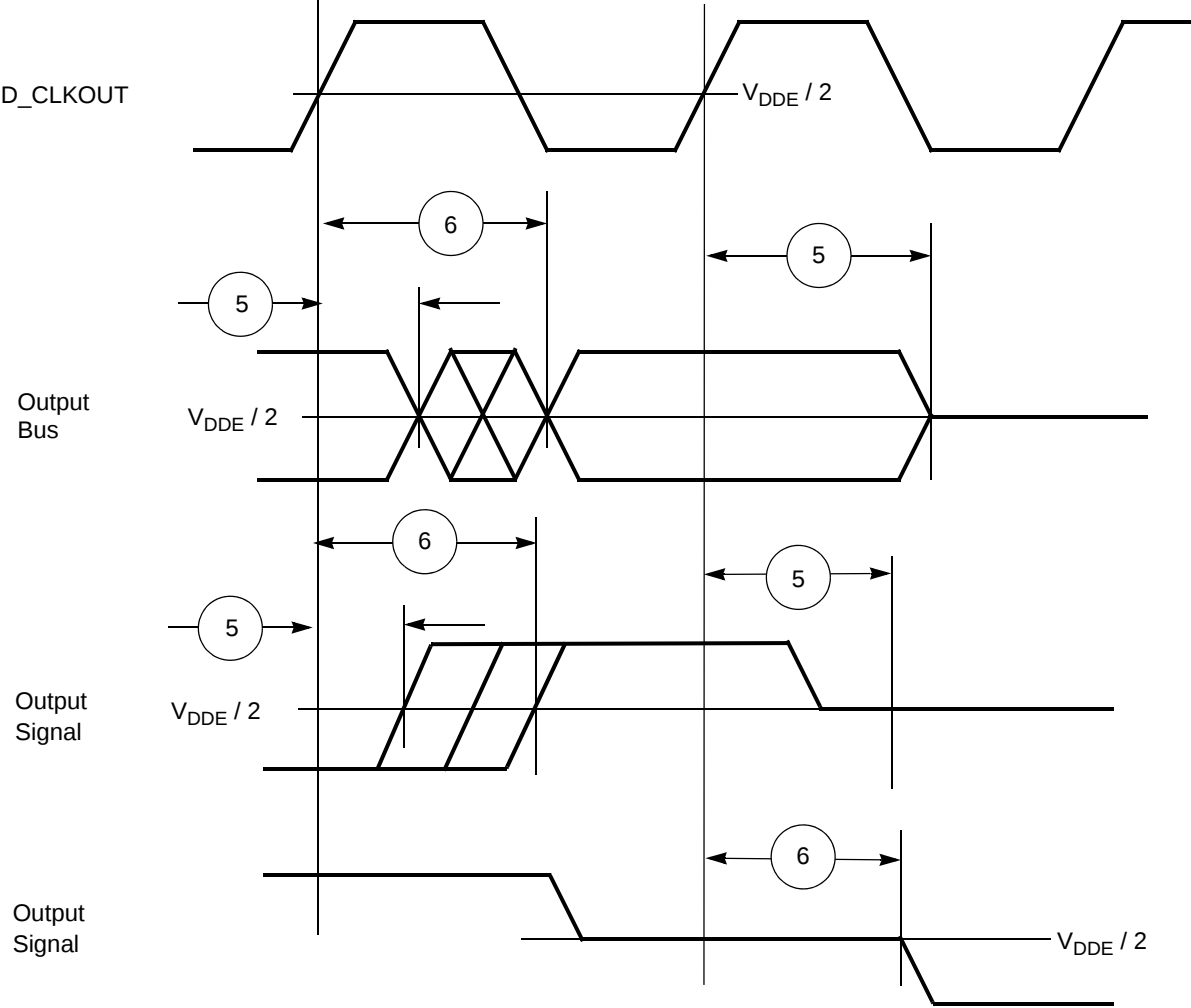


Figure 28. Synchronous Output Timing

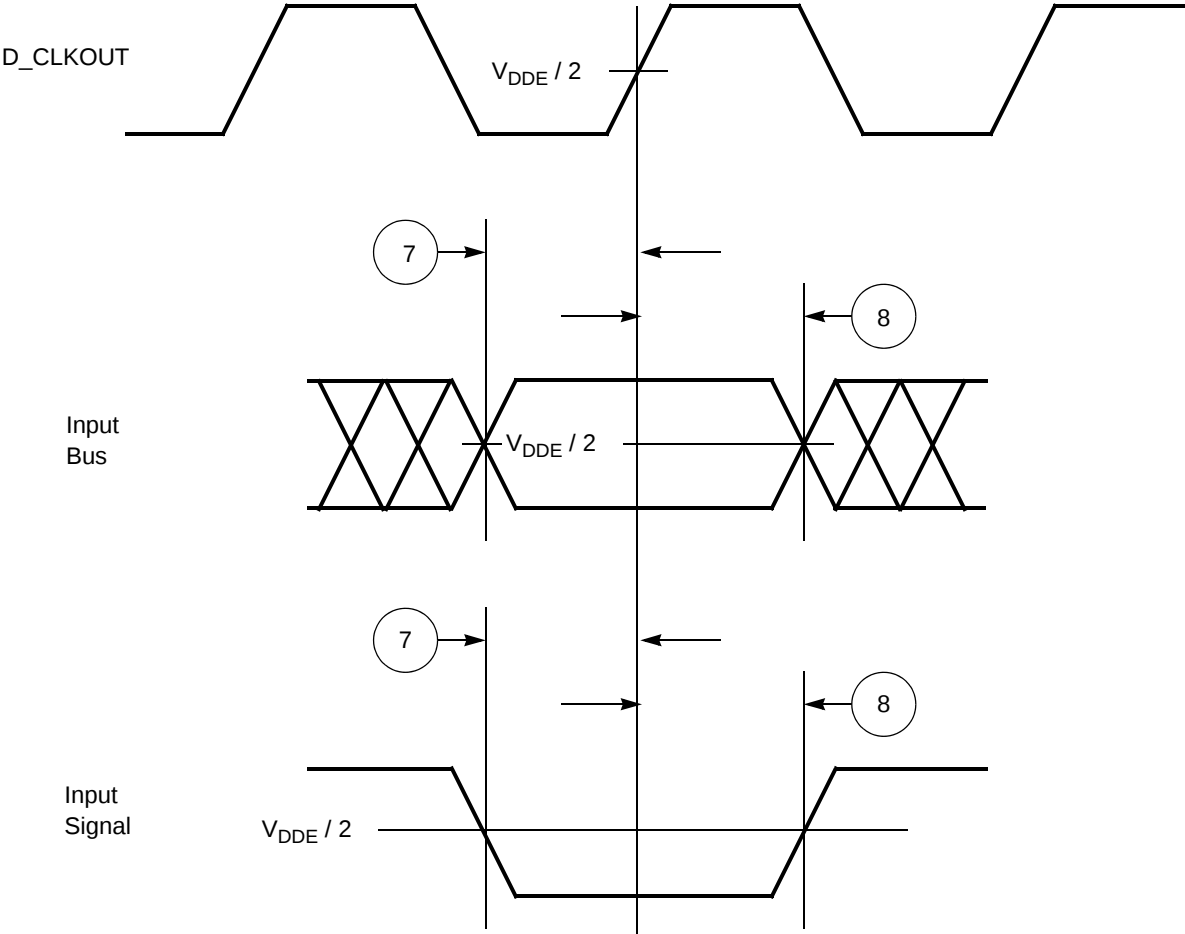


Figure 29. Synchronous Input Timing

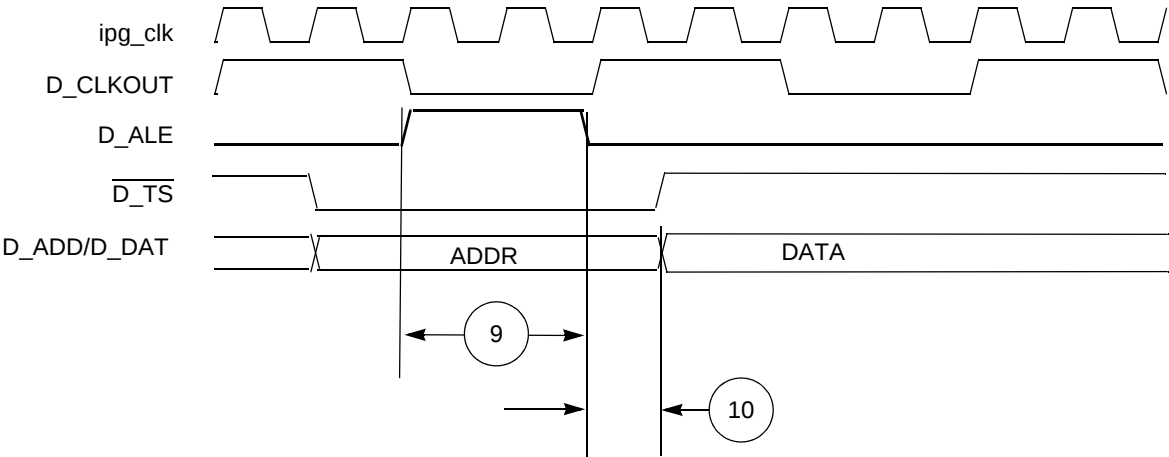


Figure 30. ALE Signal Timing

## 4.12.6 External Interrupt Timing (IRQ Pin)

Table 37. External Interrupt Timing<sup>1</sup>

| Spec | Characteristic                     | Symbol     | Min | Max | Unit        |
|------|------------------------------------|------------|-----|-----|-------------|
| 1    | IRQ Pulse Width Low                | $t_{IPWL}$ | 3   | —   | $t_{cyc}^2$ |
| 2    | IRQ Pulse Width High               | $t_{IPWH}$ | 3   | —   | $t_{cyc}^2$ |
| 3    | IRQ Edge to Edge Time <sup>3</sup> | $t_{ICYC}$ | 6   | —   | $t_{cyc}^2$ |

<sup>1</sup> IRQ timing specified at  $V_{DD} = 1.08\text{ V}$  to  $1.32\text{ V}$ ,  $V_{DDEH} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $T_A = T_L$  to  $T_H$ .

<sup>2</sup> See Notes on  $t_{cyc}$  on Figure 16 and Table 28 in Section 4.11.1 Clocking.

<sup>3</sup> Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

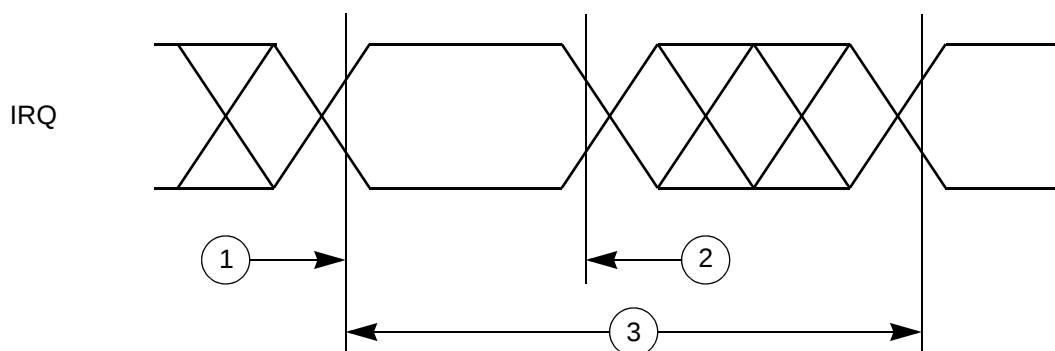


Figure 31. External Interrupt Timing

## 4.12.7 eTPU Timing

Table 38. eTPU Timing<sup>1</sup>

| Spec | Characteristic                  | Symbol     | Min            | Max | Unit        |
|------|---------------------------------|------------|----------------|-----|-------------|
| 1    | eTPU Input Channel Pulse Width  | $t_{ICPW}$ | 4              | —   | $t_{cyc}^2$ |
| 2    | eTPU Output Channel Pulse Width | $t_{OCPW}$ | 1 <sup>3</sup> | —   | $t_{cyc}^2$ |

<sup>1</sup> eTPU timing specified at  $V_{DD} = 1.08\text{ V}$  to  $1.32\text{ V}$ ,  $V_{DDEH} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $T_A = T_L$  to  $T_H$ , and  $C_L = 200\text{ pF}$  with  $SRC = 0b00$ .

<sup>2</sup> See Notes on  $t_{cyc}$  on Figure 16 and Table 28 in Section 4.11.1 Clocking.

<sup>3</sup> This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

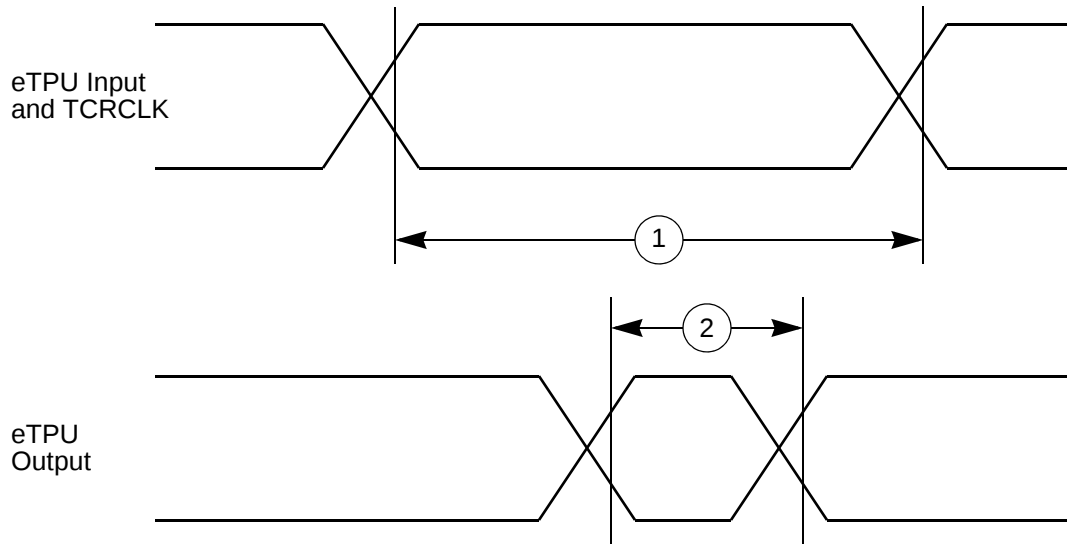


Figure 32. eTPU Timing

### 4.12.8 eMIOS Timing

Table 39. eMIOS Timing<sup>1</sup>

| Spec | Characteristic           | Symbol     | Min            | Max | Unit        |
|------|--------------------------|------------|----------------|-----|-------------|
| 1    | eMIOS Input Pulse Width  | $t_{MIPW}$ | 4              | —   | $t_{cyc}^2$ |
| 2    | eMIOS Output Pulse Width | $t_{MOPW}$ | 1 <sup>3</sup> | —   | $t_{cyc}^2$ |

<sup>1</sup> eMIOS timing specified at  $V_{DD} = 1.08 \text{ V}$  to  $1.32 \text{ V}$ ,  $V_{DDEH} = 3.0 \text{ V}$  to  $5.5 \text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ ,  $T_A = T_L$  to  $T_H$ , and  $C_L = 50 \text{ pF}$  with  $SRC = 0b00$ .

<sup>2</sup> See Notes on  $t_{cyc}$  on [Figure 16](#) and [Table 28](#) in [Section 4.11.1 Clocking](#).

<sup>3</sup> This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

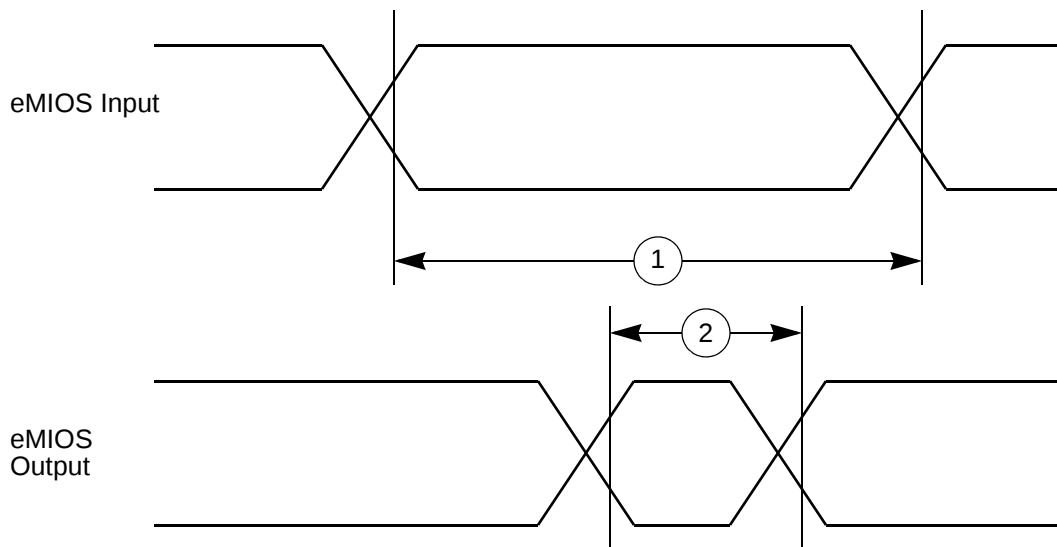


Figure 33. eMIOS Timing

### 4.12.9 DSPI Timing

Table 40. DSPI Timing<sup>1 2</sup>

| Spec | Characteristic                                                                                                    | Symbol     | Peripheral Bus Freq: 132 MHz                                 |                       | Unit |
|------|-------------------------------------------------------------------------------------------------------------------|------------|--------------------------------------------------------------|-----------------------|------|
|      |                                                                                                                   |            | Min                                                          | Max                   |      |
| 1    | DSPI Cycle Time <sup>3, 4</sup><br>Master (MTFE = 0)<br>Slave (MTFE = 0)<br>Master (MTFE = 1)<br>Slave (MTFE = 1) | $t_{SCK}$  | $t_{SYS} * 2$                                                | $t_{SYS} * 32768 * 7$ | ns   |
| 2    | PCS to SCK Delay <sup>5</sup>                                                                                     | $t_{CSC}$  | 12                                                           | —                     | ns   |
| 3    | After SCK Delay <sup>6</sup><br>Master mode<br>Slave mode                                                         | $t_{ASC}$  | $t_{SYS} * 2$<br>$t_{SYS} * 3 -$<br>constraints <sup>7</sup> | —                     | ns   |
| 4    | SCK Duty Cycle                                                                                                    | $t_{SDC}$  | $0.33 * t_{SCK}$                                             | $0.66 * t_{SCK}$      | ns   |
| 5    | Slave Access Time<br>( $\overline{SS}$ active to SOUT valid)                                                      | $t_A$      | —                                                            | 25                    | ns   |
| 6    | Slave SOUT Disable Time<br>( $\overline{SS}$ inactive to SOUT High-Z or invalid)                                  | $t_{DIS}$  | —                                                            | 25                    | ns   |
| 7    | $\overline{PCSx}$ to $\overline{PCSS}$ time                                                                       | $t_{PCSC}$ | $t_{SYS} * 2$                                                | $t_{SYS} * 7$         | ns   |
| 8    | $\overline{PCSS}$ to $\overline{PCSx}$ time                                                                       | $t_{PASC}$ | $t_{SYS} * 2$                                                | $t_{SYS} * 7$         | ns   |

Table 40. DSPI Timing<sup>1 2</sup> (continued)

| Spec | Characteristic                           | Symbol    | Peripheral Bus Freq: 132 MHz |     | Unit |
|------|------------------------------------------|-----------|------------------------------|-----|------|
|      |                                          |           | Min                          | Max |      |
| 9    | Data Setup Time for Inputs               | $t_{SUI}$ |                              |     |      |
|      | Master (MTFE = 0)                        |           | 20                           | —   | ns   |
|      | Slave                                    |           | 4                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 0) <sup>8</sup> |           | 6                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | 20                           | —   | ns   |
| 10   | Data Hold Time for Inputs                | $t_{HI}$  |                              |     |      |
|      | Master (MTFE = 0)                        |           | –3                           | —   | ns   |
|      | Slave                                    |           | 7                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 0) <sup>8</sup> |           | 12                           | —   | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | –3                           | —   | ns   |
| 11   | Data Valid (after SCK edge)              | $t_{SUO}$ |                              |     |      |
|      | Master (MTFE = 0)                        |           | —                            | 5   | ns   |
|      | Slave                                    |           | —                            | 25  | ns   |
|      | Master (MTFE = 1, CPHA = 0)              |           | —                            | 13  | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | —                            | 5   | ns   |
| 12   | Data Hold Time for Outputs               | $t_{HO}$  |                              |     |      |
|      | Master (MTFE = 0)                        |           | –5                           | —   | ns   |
|      | Slave                                    |           | 2.5                          | —   | ns   |
|      | Master (MTFE = 1, CPHA = 0)              |           | 3                            | —   | ns   |
|      | Master (MTFE = 1, CPHA = 1)              |           | –5                           | —   | ns   |

<sup>1</sup> DSPI timing specified at  $V_{DD} = 1.08 \text{ V}$  to  $1.32 \text{ V}$ ,  $V_{DDEH} = 3.0 \text{ V}$  to  $5.5 \text{ V}$ ,  $V_{DD33}$  and  $V_{DDSYN} = 3.0 \text{ V}$  to  $3.6 \text{ V}$ , and  $T_A = T_L$  to  $T_H$

<sup>2</sup> Speed is the nominal maximum frequency of platform clock ( $f_{platt}$ ). Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 Mhz for system core clock ( $f_{sys}$ ) + 2% FM.

<sup>3</sup> The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

<sup>4</sup> The actual minimum SCK cycle time is limited by pad performance.

<sup>5</sup> The maximum value is programmable in DSPI\_CTARn[PSSCK] and DSPI\_CTARn[CSSCK].

<sup>6</sup> The maximum value is programmable in DSPI\_CTARn[PASC] and DSPI\_CTARn[ASC].

<sup>7</sup> For example, external master should start SCK clock not earlier than 3 system clock periods after assertion SS

<sup>8</sup> This number is calculated assuming the SMPL\_PT bitfield in DSPI\_MCR is set to 0b10.

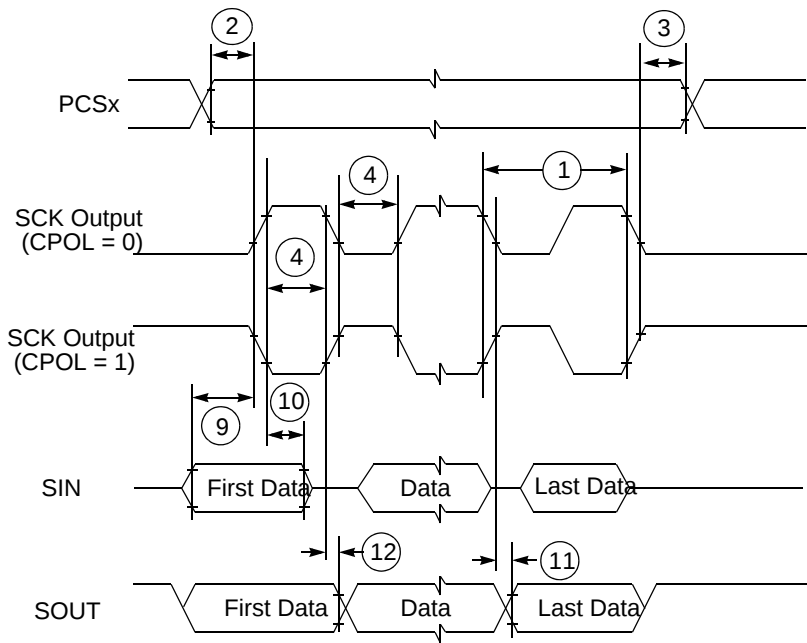
The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

Table 41. DSPI LVDS Timing<sup>1, 2</sup>

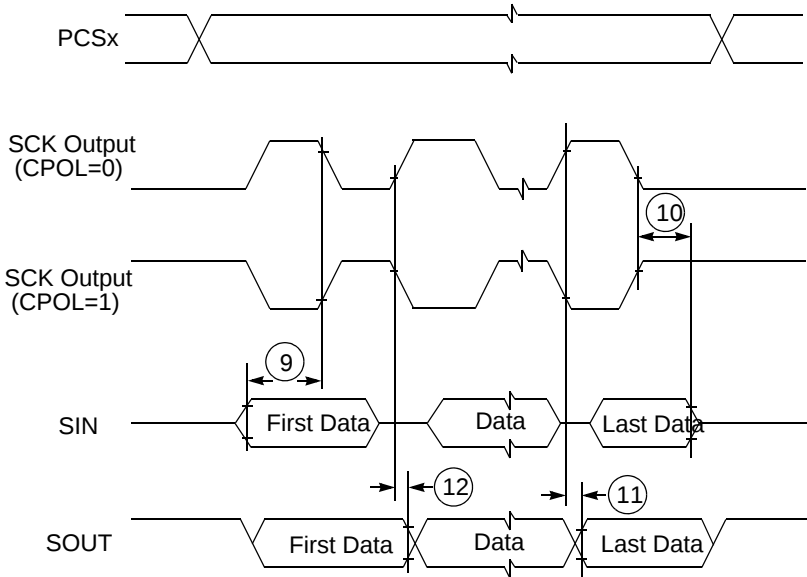
| Characteristic                         | Symbol                | Min                     | Max                     | Unit |
|----------------------------------------|-----------------------|-------------------------|-------------------------|------|
| LVDS Clock to Data/Chip Select Outputs | $t_{LVDS\text{DATA}}$ | $-0.25 \times t_{SCYC}$ | $+0.25 \times t_{SCYC}$ | ns   |

<sup>1</sup> These are typical values that are estimated from simulation.

<sup>2</sup> See DSPI LVDS Pad related data in [Table 17](#).



**Figure 34. DSPI Classic SPI Timing — Master, CPHA = 0**



**Figure 35. DSPI Classic SPI Timing — Master, CPHA = 1**

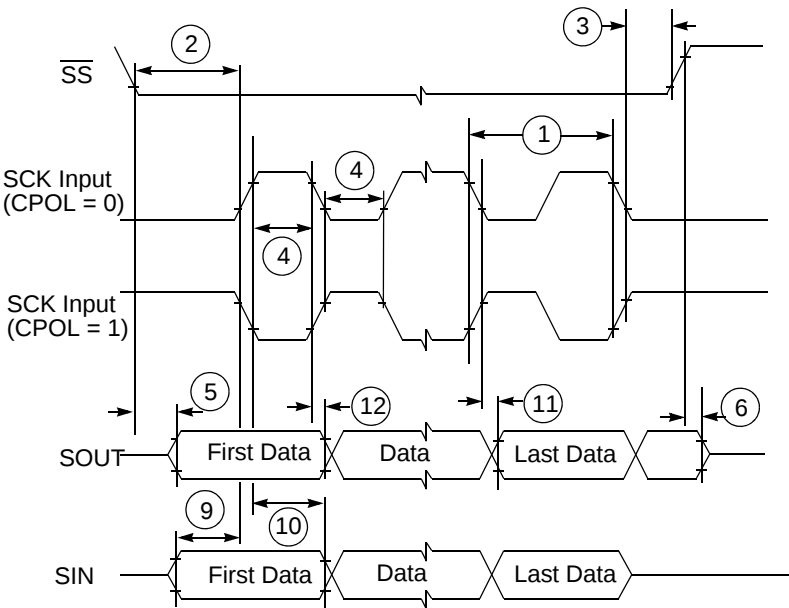


Figure 36. DSPI Classic SPI Timing — Slave, CPHA = 0

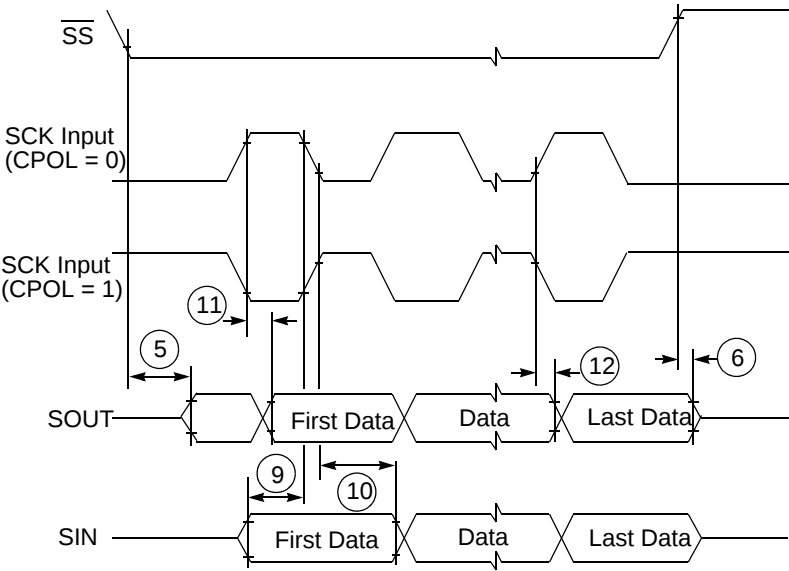


Figure 37. DSPI Classic SPI Timing — Slave, CPHA = 1

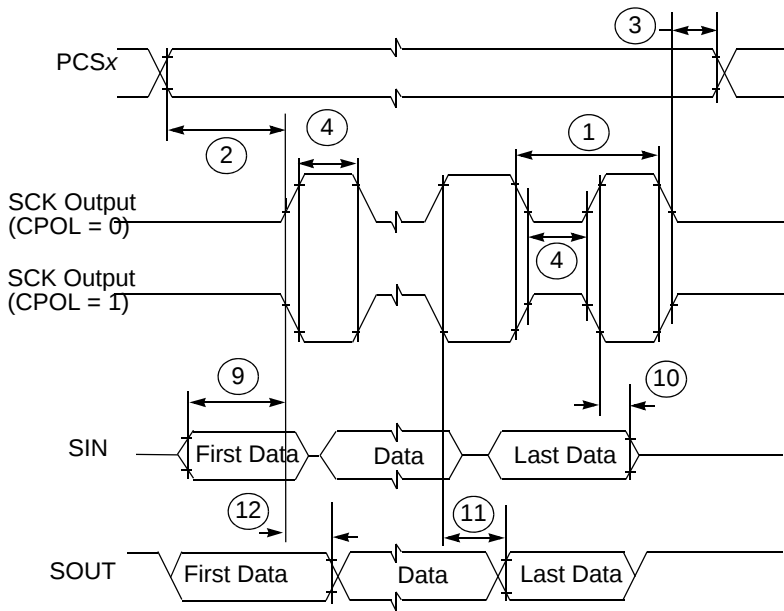


Figure 38. DSPI Modified Transfer Format Timing — Master, CPHA = 0

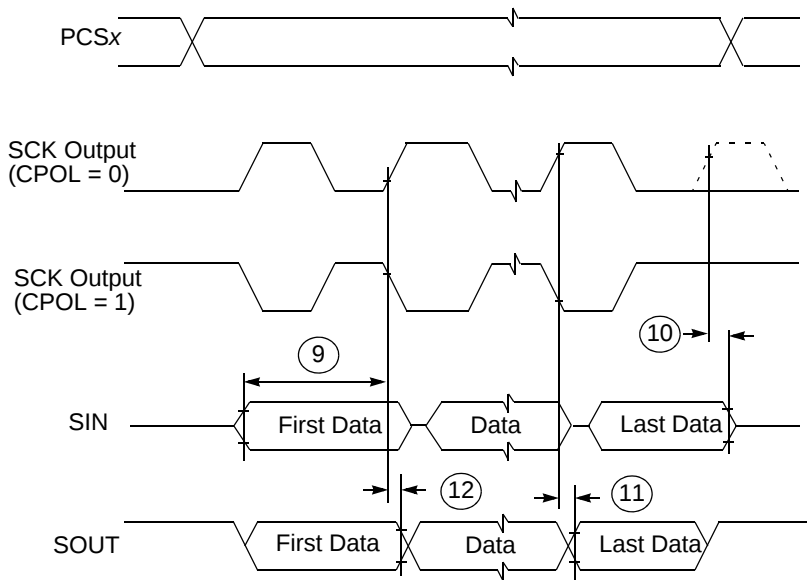


Figure 39. DSPI Modified Transfer Format Timing — Master, CPHA = 1

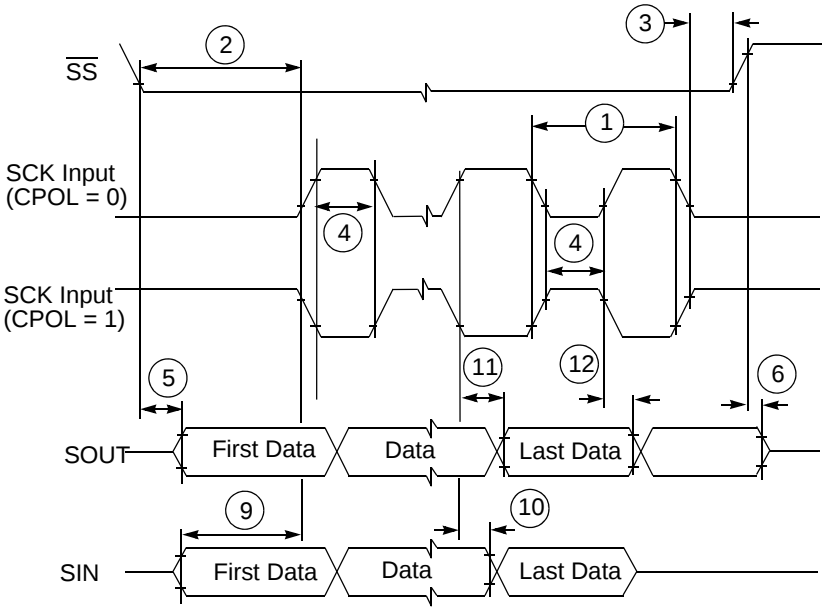


Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

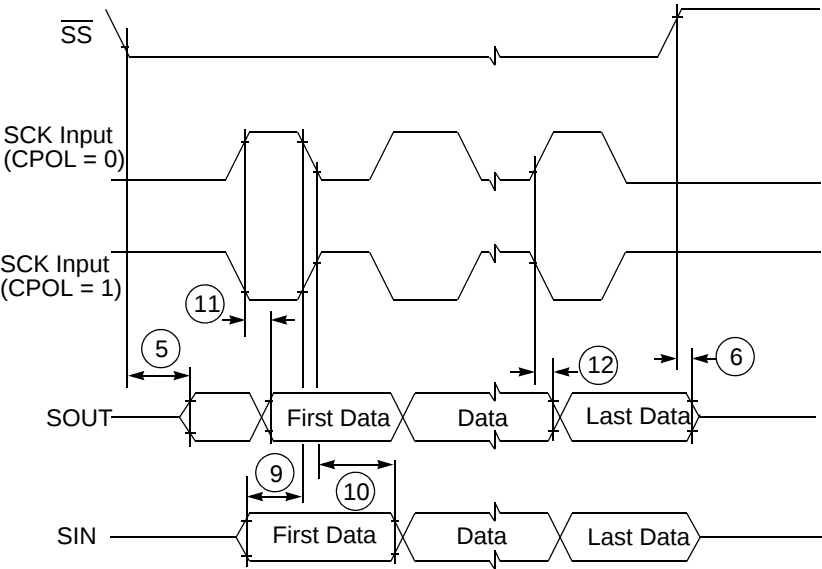


Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

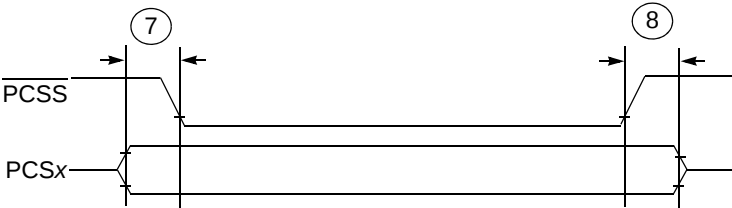


Figure 42. DSPI PCS Strobe (PCSS) Timing

# 5 Package Information

The latest package outline drawings are available on the product summary pages on our website: <http://www.freescale.com/powerarchitecture>. The following table lists the package case number. Use these numbers in the webpage’s keyword search engine to find the latest package outline drawings.

**Table 42. Package Information**

| Package Type | Case Outline Number |
|--------------|---------------------|
| 324 TEPBGA   | 98ASS23840W         |
| 416 TEPBGA   | 98ARE10523D         |
| 516 TEPBGA   | 98ARS10503D         |

# 5.1 324-Pin Package

The package drawings of the 324-pin TEPBGA package are shown in [Figure 43](#) and [Figure 44](#).

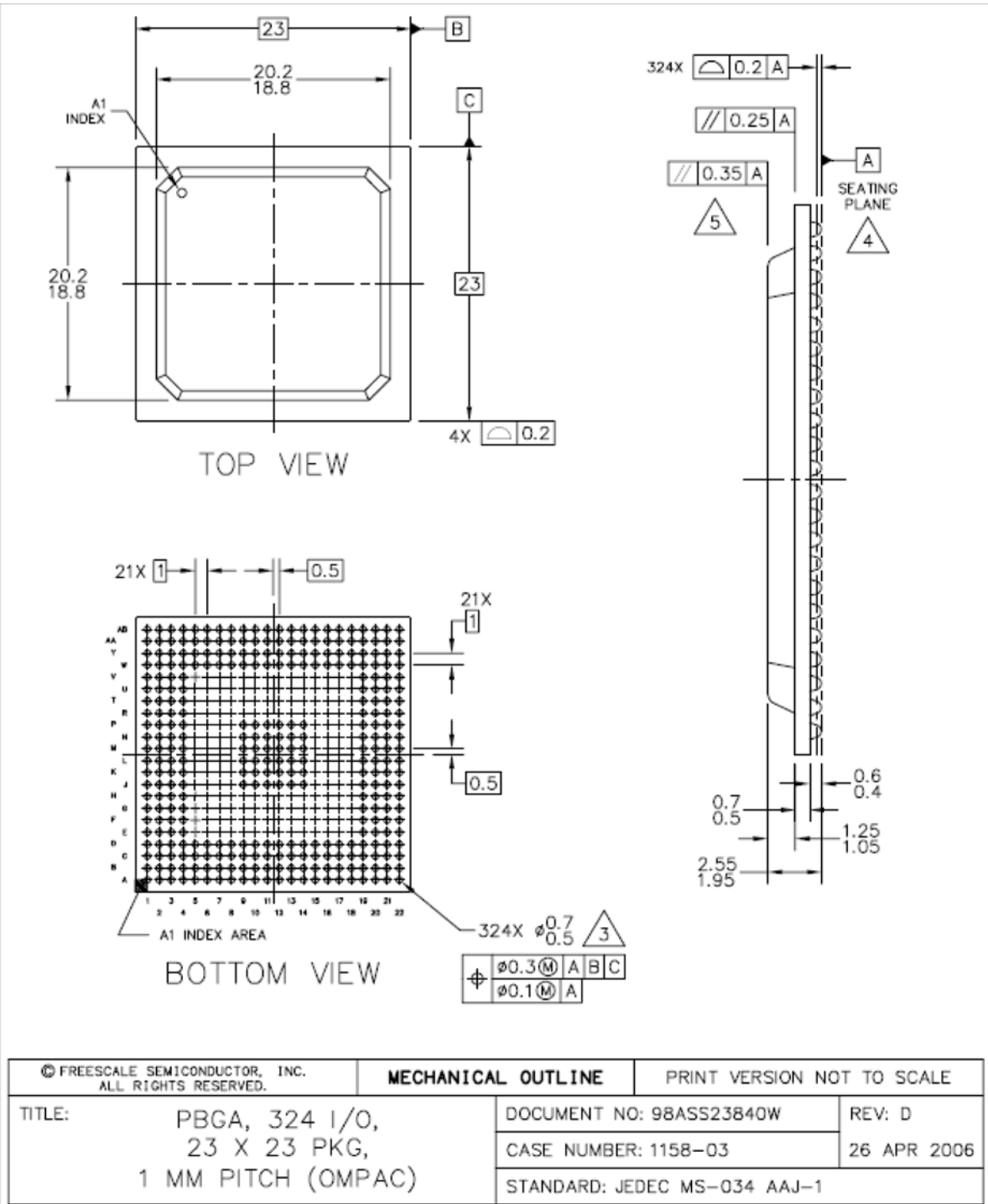


Figure 43. 324 TEPBGA Package (1 of 2)

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

|                                                         |                                                      |                              |                            |             |
|---------------------------------------------------------|------------------------------------------------------|------------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. |                                                      | MECHANICAL OUTLINE           | PRINT VERSION NOT TO SCALE |             |
| TITLE:                                                  | PBGA, 324 I/O,<br>23 X 23 PKG,<br>1 MM PITCH (OMPAC) | DOCUMENT NO: 98ASS23840W     |                            | REV: D      |
|                                                         |                                                      | CASE NUMBER: 1158-03         |                            | 26 APR 2006 |
|                                                         |                                                      | STANDARD: JEDEC MS-034 AAJ-1 |                            |             |

Figure 44. 324 TEPBGA Package (2 of 2)

# 5.2 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 45 and Figure 46.

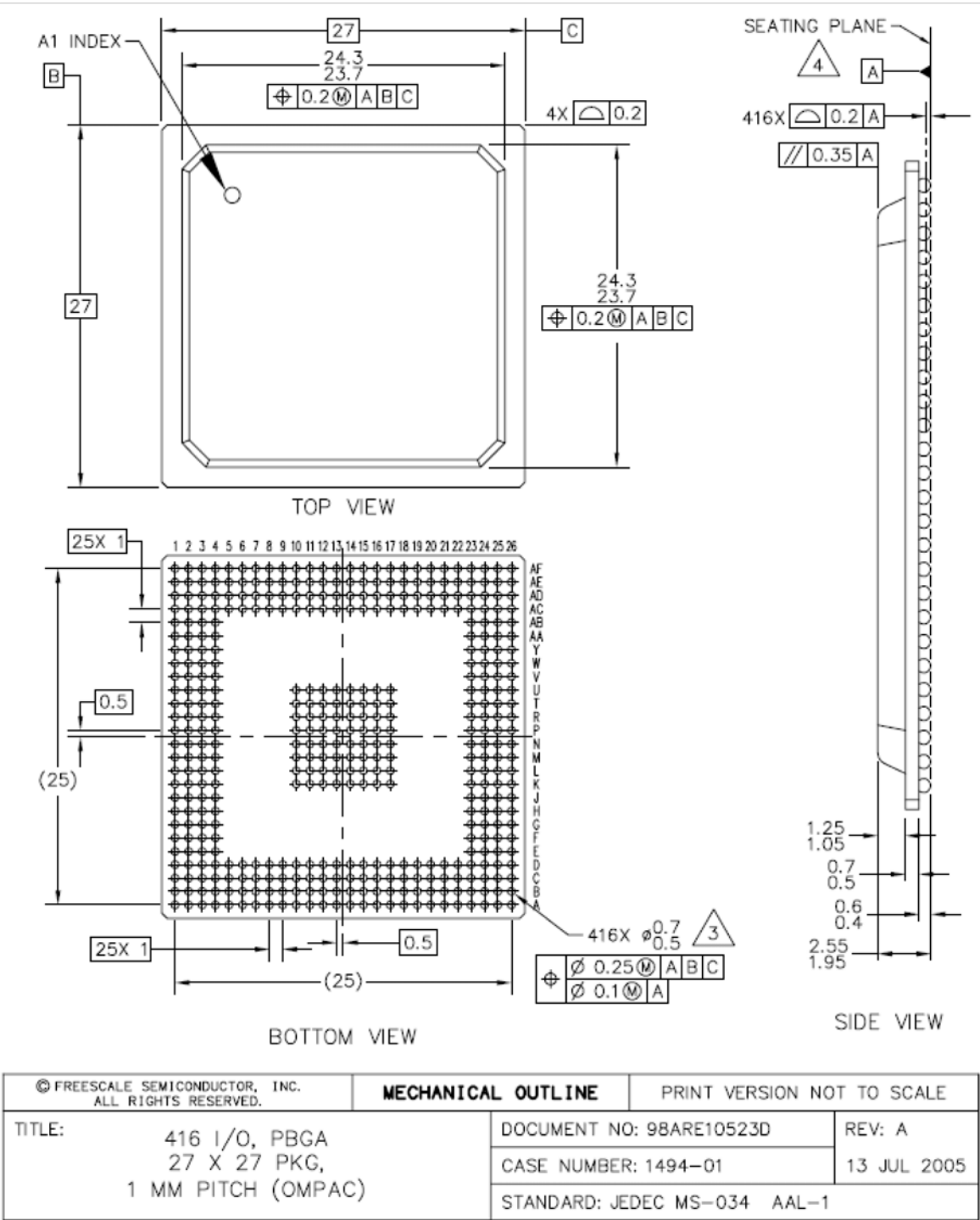


Figure 45. 416 TEPBGA Package (1 of 2)

NOTES:

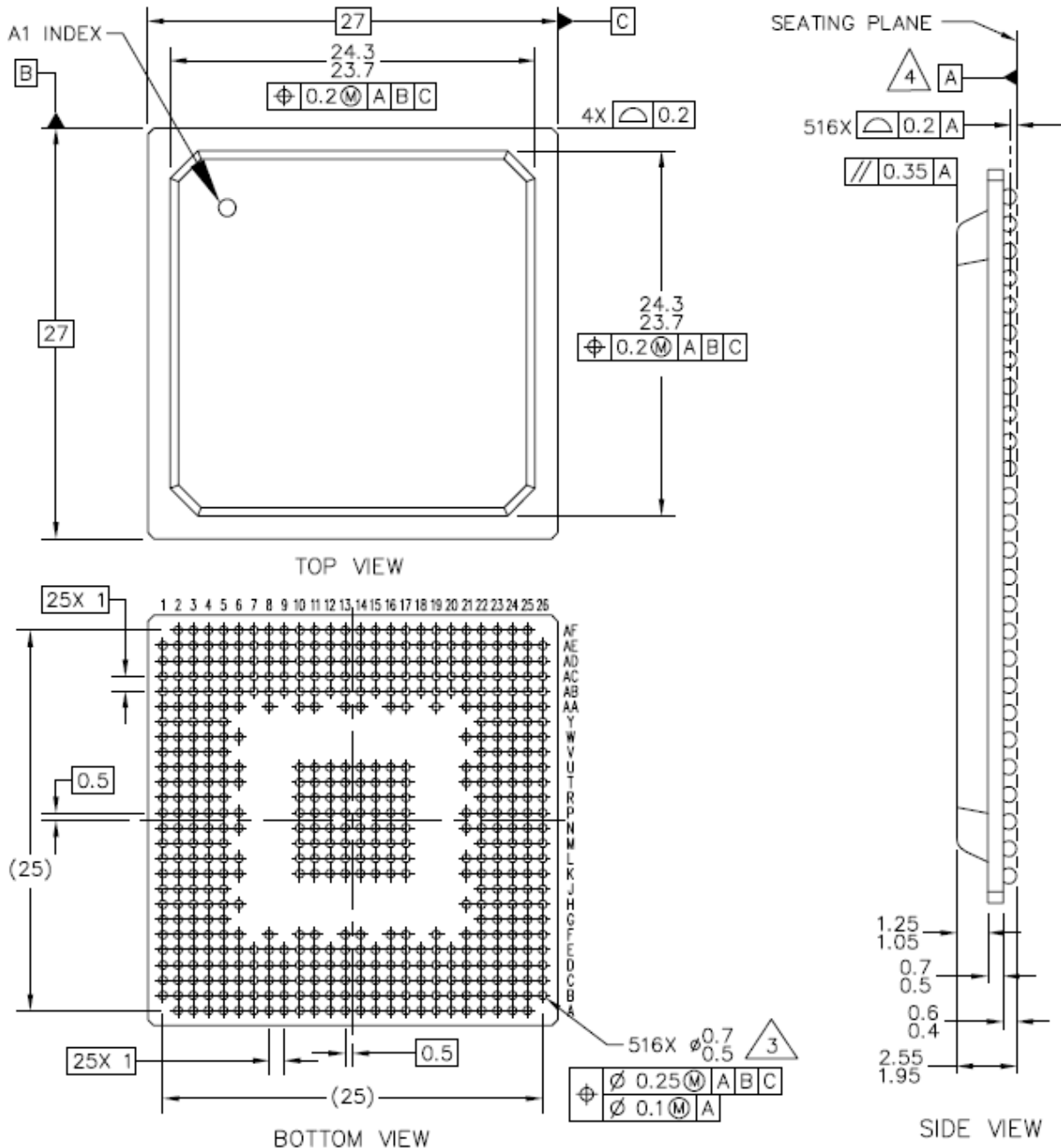
- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

|                                                               |                              |                    |                            |
|---------------------------------------------------------------|------------------------------|--------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.       |                              | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE:<br>416 I/O, PBGA<br>27 X 27 PKG,<br>1 MM PITCH (OMPAC) | DOCUMENT NO: 98ARE10523D     |                    | REV: A                     |
|                                                               | CASE NUMBER: 1494-01         |                    | 13 JUL 2005                |
|                                                               | STANDARD: JEDEC MS-034 AAL-1 |                    |                            |

Figure 46. 416 TEPBGA Package (2 of 2)

### 5.3 516-Pin Package

The package drawings of the 516-pin TEPBGA package are shown in Figure 47 and Figure 48.



|                                                               |  |                              |  |                            |  |
|---------------------------------------------------------------|--|------------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.       |  | MECHANICAL OUTLINE           |  | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>516 I/O, PBGA<br>27 X 27 PKG,<br>1 MM PITCH (OMPAC) |  | DOCUMENT NO: 98ARS10503D     |  | REV: B                     |  |
|                                                               |  | CASE NUMBER: 1164A-01        |  | 09 AUG 2005                |  |
|                                                               |  | STANDARD: JEDEC MS-034 AAL-1 |  |                            |  |

Figure 47. 516 TEPBGA Package (1 of 2)

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 5. PACKAGE CODES: 5193 & 5198.

|                                                         |                                                     |                              |                            |             |
|---------------------------------------------------------|-----------------------------------------------------|------------------------------|----------------------------|-------------|
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| TITLE:                                                  | 516 I/O, PBGA<br>27 X 27 PKG,<br>1 MM PITCH (OMPAC) | DOCUMENT NO: 98ARS10503D     |                            | REV: B      |
|                                                         |                                                     | CASE NUMBER: 1164A–01        |                            | 09 AUG 2005 |
|                                                         |                                                     | STANDARD: JEDEC MS–034 AAL–1 |                            |             |

Figure 48. 516 TEPBGA Package (2 of 2)

## 6 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: <http://www.freescale.com>.

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *MPC5674F Microprocessor Reference Manual* (document number MPC5674FRM).

# Appendix A Signal Properties and Muxing

The following table shows the signals properties for each pin on the MPC5674F. For each port pin that has an associated SIU\_PCRn register to control its pin properties, the supported functions column lists the functions associated with the programming of the SIU\_PCRn[PA] bit in the order: Primary function (P), Function 2 (F2), Function 3 (F3), and GPIO (G). See [Figure 49](#).

| Table 2. Signal Properties Summary                      |                           |                          |               |                       |                            |     |             |
|---------------------------------------------------------|---------------------------|--------------------------|---------------|-----------------------|----------------------------|-----|-------------|
|                                                         | GPIO/<br>PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/<br>F/<br>G | Function <sup>3</sup> | Function Summary           | I/O | Pad<br>Type |
| <b>Primary</b> Functions<br>are listed First →          | 113                       | TCRCLKA_IRQ7_GPIO113     | P             | TCRCLKA               | eTPU A TCR clock           | I   | 5V M        |
|                                                         |                           |                          | A1            | IRQ7                  | External interrupt request | I   |             |
|                                                         |                           |                          | A2            | —                     | —                          | —   |             |
|                                                         |                           |                          | G             | GPIO113               | GPIO                       | I/O |             |
| <b>Secondary</b> Functions<br>are alternate functions → |                           |                          |               |                       |                            |     |             |
| GPIO Functions are<br>listed <b>Last</b> →              |                           |                          |               |                       |                            |     |             |
|                                                         |                           |                          |               |                       |                            |     |             |
| Function not implemented on this device                 |                           |                          |               |                       |                            |     |             |

Figure 49. Supported Functions Example

### Table 43. Signal Properties and Muxing Summary

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary             | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|----------------------------|--------------------|-----------------------|------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                            |                    |                       |                              |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| eTPU_A                |                            |                    |                       |                              |           |                       |                      |                                 |                                |                  |     |     |
| 113                   | TCRCLKA_IRQ7_<br>GPIO113   | P                  | TCRCLKA               | eTPU A TCR clock             | I         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | K1               | L1  | K4  |
|                       |                            | A1                 | IRQ7                  | External interrupt request   | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO113               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 114                   | ETPUA0_ETPUA12_<br>GPIO114 | P                  | ETPUA0                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | K2               | L2  | L6  |
|                       |                            | A1                 | ETPUA12               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO114               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 115                   | ETPUA1_ETPUA13_<br>GPIO115 | P                  | ETPUA1                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | J1               | L3  | J1  |
|                       |                            | A1                 | ETPUA13               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO115               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 116                   | ETPUA2_ETPUA14_<br>GPIO116 | P                  | ETPUA2                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | J2               | L4  | J2  |
|                       |                            | A1                 | ETPUA14               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO116               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 117                   | ETPUA3_ETPUA15_<br>GPIO117 | P                  | ETPUA3                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | J3               | K1  | H4  |
|                       |                            | A1                 | ETPUA15               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO117               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 118                   | ETPUA4_ETPUA16_<br>GPIO118 | P                  | ETPUA4                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | J4               | K2  | J4  |
|                       |                            | A1                 | ETPUA16               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO118               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>    | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary             | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|-----------------------------|--------------------|-----------------------|------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                             |                    |                       |                              |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 119                   | ETPUA5_ETPUA17_<br>GPIO119  | P                  | ETPUA5                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | H1               | K3  | H1  |
|                       |                             | A1                 | ETPUA17               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO119               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 120                   | ETPUA6_ETPUA18_<br>GPIO120  | P                  | ETPUA6                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | H2               | K4  | K5  |
|                       |                             | A1                 | ETPUA18               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO120               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 121                   | ETPUA7_ETPUA19_<br>GPIO121  | P                  | ETPUA7                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | J1  | H2  |
|                       |                             | A1                 | ETPUA19               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO121               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 122                   | ETPUA8_ETPUA20_<br>GPIO122  | P                  | ETPUA8                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | J2  | H3  |
|                       |                             | A1                 | ETPUA20               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO122               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 123                   | ETPUA9_ETPUA21_<br>GPIO123  | P                  | ETPUA9                | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | H3               | J3  | J3  |
|                       |                             | A1                 | ETPUA21               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO123               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 124                   | ETPUA10_ETPUA22_<br>GPIO124 | P                  | ETPUA10               | eTPU A channel               | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | G1               | J4  | K6  |
|                       |                             | A1                 | ETPUA22               | eTPU A channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO124               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 125                   | ETPUA11_ETPUA23_GPIO125  | P                  | ETPUA11               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | G2               | H1  | G1  |
|                       |                          | A1                 | ETPUA23               | eTPU A channel (output only)  | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO125               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 126                   | ETPUA12_PCSB1_GPIO126    | P                  | ETPUA12               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | G3               | H2  | J5  |
|                       |                          | A1                 | PCSB1                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO126               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 127                   | ETPUA13_PCSB3_GPIO127    | P                  | ETPUA13               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | F1               | H4  | G2  |
|                       |                          | A1                 | PCSB3                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO127               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 128                   | ETPUA14_PCSB4_GPIO128    | P                  | ETPUA14               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | F2               | H3  | H5  |
|                       |                          | A1                 | PCSB4                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO128               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 129                   | ETPUA15_PCSB5_GPIO129    | P                  | ETPUA15               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | F3               | G1  | G3  |
|                       |                          | A1                 | PCSB5                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO129               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 130                   | ETPUA16_PCSD1_GPIO130    | P                  | ETPUA16               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | H4               | G2  | H6  |
|                       |                          | A1                 | PCSD1                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO130               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>  | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|---------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                           |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 131                   | ETPUA17_PCSD2_<br>GPIO131 | P                  | ETPUA17               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | G4               | G3  | G4  |
|                       |                           | A1                 | PCSD2                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | G                  | GPIO131               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 132                   | ETPUA18_PCSD3_<br>GPIO132 | P                  | ETPUA18               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | G4  | G5  |
|                       |                           | A1                 | PCSD3                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | G                  | GPIO132               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 133                   | ETPUA19_PCSD4_<br>GPIO133 | P                  | ETPUA19               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | F1  | F1  |
|                       |                           | A1                 | PCSD4                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | G                  | GPIO133               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 134                   | ETPUA20_IRQ8_<br>GPIO134  | P                  | ETPUA20               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | E1               | F2  | F2  |
|                       |                           | A1                 | IRQ8                  | External interrupt request    | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | G                  | GPIO134               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 135                   | ETPUA21_IRQ9_<br>GPIO135  | P                  | ETPUA21               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | C1               | F3  | F3  |
|                       |                           | A1                 | IRQ9                  | External interrupt request    | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | G                  | GPIO135               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 136                   | ETPUA22_IRQ10_<br>GPIO136 | P                  | ETPUA22               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | E2               | F4  | F4  |
|                       |                           | A1                 | IRQ10                 | External interrupt request    | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                           | G                  | GPIO136               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| <b>GPIO/PCR<sup>1</sup></b> | <b>Signal Name<sup>2</sup></b> | <b>P/A/G<sup>3</sup></b> | <b>Function<sup>4</sup></b> | <b>Function Summary</b>       | <b>Direction</b> | <b>Pad Type<sup>5</sup></b> | <b>Voltage<sup>6</sup></b> | <b>State during RESET<sup>7</sup></b> | <b>State after RESET<sup>8</sup></b> | <b>Package Location</b> |            |            |
|-----------------------------|--------------------------------|--------------------------|-----------------------------|-------------------------------|------------------|-----------------------------|----------------------------|---------------------------------------|--------------------------------------|-------------------------|------------|------------|
|                             |                                |                          |                             |                               |                  |                             |                            |                                       |                                      | <b>324</b>              | <b>416</b> | <b>516</b> |
| 137                         | ETPUA23_IRQ11_<br>GPIO137      | P                        | ETPUA23                     | eTPU A channel                | I/O              | MH                          | V <sub>DDEH1</sub>         | —/WKPCFG                              | —/WKPCFG                             | D1                      | E1         | E1         |
|                             |                                | A1                       | IRQ11                       | External interrupt request    | I                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | A2                       | —                           | —                             | —                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | G                        | GPIO137                     | GPIO                          | I/O              |                             |                            |                                       |                                      |                         |            |            |
| 138                         | ETPUA24_IRQ12_<br>GPIO138      | P                        | ETPUA24                     | eTPU A channel                | I/O              | MH                          | V <sub>DDEH1</sub>         | —/WKPCFG                              | —/WKPCFG                             | E3                      | E2         | E2         |
|                             |                                | A1                       | IRQ12                       | External interrupt request    | I                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | A2                       | —                           | —                             | —                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | G                        | GPIO138                     | GPIO                          | I/O              |                             |                            |                                       |                                      |                         |            |            |
| 139                         | ETPUA25_IRQ13_<br>GPIO139      | P                        | ETPUA25                     | eTPU A channel                | I/O              | MH                          | V <sub>DDEH1</sub>         | —/WKPCFG                              | —/WKPCFG                             | D2                      | E3         | E3         |
|                             |                                | A1                       | IRQ13                       | External interrupt request    | I                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | A2                       | —                           | —                             | —                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | G                        | GPIO139                     | GPIO                          | I/O              |                             |                            |                                       |                                      |                         |            |            |
| 140                         | ETPUA26_IRQ14_<br>GPIO140      | P                        | ETPUA26                     | eTPU A channel                | I/O              | MH                          | V <sub>DDEH1</sub>         | —/WKPCFG                              | —/WKPCFG                             | C2                      | E4         | E4         |
|                             |                                | A1                       | IRQ14                       | External interrupt request    | I                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | A2                       | —                           | —                             | —                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | G                        | GPIO140                     | GPIO                          | I/O              |                             |                            |                                       |                                      |                         |            |            |
| 141                         | ETPUA27_IRQ15_<br>GPIO141      | P                        | ETPUA27                     | eTPU A channel                | I/O              | MH                          | V <sub>DDEH1</sub>         | —/WKPCFG                              | —/WKPCFG                             | F4                      | D1         | D1         |
|                             |                                | A1                       | IRQ15                       | External interrupt request    | I                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | A2                       | —                           | —                             | —                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | G                        | GPIO141                     | GPIO                          | I/O              |                             |                            |                                       |                                      |                         |            |            |
| 142                         | ETPUA28_PCSC1_<br>GPIO142      | P                        | ETPUA28                     | eTPU A channel                | I/O              | MH                          | V <sub>DDEH1</sub>         | —/WKPCFG                              | —/WKPCFG                             | —                       | D2         | D2         |
|                             |                                | A1                       | PCSC1                       | DSPI C peripheral chip select | O                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | A2                       | —                           | —                             | —                |                             |                            |                                       |                                      |                         |            |            |
|                             |                                | G                        | GPIO142                     | GPIO                          | I/O              |                             |                            |                                       |                                      |                         |            |            |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|----------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                            |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 143                   | ETPUA29_PCSC2_<br>GPIO143  | P                  | ETPUA29               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | D3  | D3  |
|                       |                            | A1                 | PCSC2                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO143               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 144                   | ETPUA30_PCSC3_<br>GPIO144  | P                  | ETPUA30               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | E4               | C1  | C1  |
|                       |                            | A1                 | PCSC3                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO144               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 145                   | ETPUA31_PCSC4_<br>GPIO145  | P                  | ETPUA31               | eTPU A channel                | I/O       | MH                    | V <sub>DDEH1</sub>   | —/WKPCFG                        | —/WKPCFG                       | D3               | C2  | C2  |
|                       |                            | A1                 | PCSC4                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO145               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| eTPU_B                |                            |                    |                       |                               |           |                       |                      |                                 |                                |                  |     |     |
| 146                   | TCRCLKB_IRQ6_<br>GPIO146   | P                  | TCRCLKB               | eTPU B TCR clock              | I         | MH                    | V <sub>DDEH6</sub>   | —/Up                            | —/Up                           | P19              | T23 | V25 |
|                       |                            | A1                 | IRQ6                  | External interrupt request    | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO146               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 147                   | ETPUB0_ETPUB16_<br>GPIO147 | P                  | ETPUB0                | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | N19              | T24 | V26 |
|                       |                            | A1                 | ETPUB16               | eTPU B channel (output only)  | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO147               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 148                   | ETPUB1_ETPUB17_<br>GPIO148 | P                  | ETPUB1                | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | R19              | T25 | U22 |
|                       |                            | A1                 | ETPUB17               | eTPU B channel (output only)  | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO148               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary             | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|----------------------------|--------------------|-----------------------|------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                            |                    |                       |                              |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 149                   | ETPUB2_ETPUB18_<br>GPIO149 | P                  | ETPUB2                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | R22              | T26 | U23 |
|                       |                            | A1                 | ETPUB18               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO149               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 150                   | ETPUB3_ETPUB19_<br>GPIO150 | P                  | ETPUB3                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | R21              | R23 | T22 |
|                       |                            | A1                 | ETPUB19               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO150               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 151                   | ETPUB4_ETPUB20_<br>GPIO151 | P                  | ETPUB4                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | P22              | R24 | U24 |
|                       |                            | A1                 | ETPUB20               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO151               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 152                   | ETPUB5_ETPUB21_<br>GPIO152 | P                  | ETPUB5                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | P21              | R25 | U25 |
|                       |                            | A1                 | ETPUB21               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO152               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 153                   | ETPUB6_ETPUB22_<br>GPIO153 | P                  | ETPUB6                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | N22              | R26 | U26 |
|                       |                            | A1                 | ETPUB22               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO153               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 154                   | ETPUB7_ETPUB23_<br>GPIO154 | P                  | ETPUB7                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | M19              | P23 | T23 |
|                       |                            | A1                 | ETPUB23               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                            | G                  | GPIO154               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>    | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary             | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|-----------------------------|--------------------|-----------------------|------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                             |                    |                       |                              |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 155                   | ETPUB8_ETPUB24_<br>GPIO155  | P                  | ETPUB8                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | N21              | P24 | T24 |
|                       |                             | A1                 | ETPUB24               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO155               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 156                   | ETPUB9_ETPUB25_<br>GPIO156  | P                  | ETPUB9                | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | M22              | P25 | R22 |
|                       |                             | A1                 | ETPUB25               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO156               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 157                   | ETPUB10_ETPUB26_<br>GPIO157 | P                  | ETPUB10               | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | M20              | P26 | T25 |
|                       |                             | A1                 | ETPUB26               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO157               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 158                   | ETPUB11_ETPUB27_<br>GPIO158 | P                  | ETPUB11               | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | M21              | N24 | T26 |
|                       |                             | A1                 | ETPUB27               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO158               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 159                   | ETPUB12_ETPUB28_<br>GPIO159 | P                  | ETPUB12               | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | L19              | N25 | R23 |
|                       |                             | A1                 | ETPUB28               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO159               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 160                   | ETPUB13_ETPUB29_<br>GPIO160 | P                  | ETPUB13               | eTPU B channel               | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | L20              | N26 | P22 |
|                       |                             | A1                 | ETPUB29               | eTPU B channel (output only) | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | A2                 | —                     | —                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                             | G                  | GPIO160               | GPIO                         | I/O       |                       |                      |                                 |                                |                  |     |     |

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 161                   | ETPUB14_ETPUB30_ GPIO161 | P                  | ETPUB14               | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | L21              | M25 | R24 |
|                       |                          | A1                 | ETPUB30               | eTPU B channel (output only)  | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO161               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 162                   | ETPUB15_ETPUB31_ GPIO162 | P                  | ETPUB15               | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | M24 | R25 |
|                       |                          | A1                 | ETPUB31               | eTPU B channel (output only)  | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO162               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 163                   | ETPUB16_PCSA1_ GPIO163   | P                  | ETPUB16               | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | P20              | U26 | V24 |
|                       |                          | A1                 | PCSA1                 | DSPI A peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO163               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 164                   | ETPUB17_PCSA2_ GPIO164   | P                  | ETPUB17               | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | R20              | U25 | T21 |
|                       |                          | A1                 | PCSA2                 | DSPI A peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO164               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 165                   | ETPUB18_PCSA3_ GPIO165   | P                  | ETPUB18               | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | T20              | U24 | W26 |
|                       |                          | A1                 | PCSA3                 | DSPI A peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO165               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 166                   | ETPUB19_PCSA4_ GPIO166   | P                  | ETPUB19               | eTPU B channel                | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | T19              | U23 | W25 |
|                       |                          | A1                 | PCSA4                 | DSPI A peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO166               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                  |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 167                   | ETPUB20_<br>GPIO167      | P                  | ETPUB20               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | V26 | W24 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO167               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 168                   | ETPUB21_<br>GPIO168      | P                  | ETPUB21               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | V25 | V22 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO168               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 169                   | ETPUB22_<br>GPIO169      | P                  | ETPUB22               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | V24 | V23 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO169               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 170                   | ETPUB23_<br>GPIO170      | P                  | ETPUB23               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | W26 | U21 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO170               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 171                   | ETPUB24_<br>GPIO171      | P                  | ETPUB24               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | W25 | Y25 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO171               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 172                   | ETPUB25_<br>GPIO172      | P                  | ETPUB25               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | W24 | W21 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO172               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                  |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 173                   | ETPUB26_<br>GPIO173      | P                  | ETPUB26               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | V23  | Y23  |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO173               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 174                   | ETPUB27_<br>GPIO174      | P                  | ETPUB27               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | Y25  | Y24  |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO174               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 175                   | ETPUB28_<br>GPIO175      | P                  | ETPUB28               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | Y24  | AA24 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO175               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 176                   | ETPUB29_<br>GPIO176      | P                  | ETPUB29               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | Y23  | W22  |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO176               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 177                   | ETPUB30_<br>GPIO177      | P                  | ETPUB30               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | U20              | AA24 | AB24 |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO177               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 178                   | ETPUB31_<br>GPIO178      | P                  | ETPUB31               | eTPU B channel   | I/O       | MH                    | V <sub>DDEH6</sub>   | —/WKPCFG                        | —/WKPCFG                       | U19              | AB24 | Y22  |
|                       |                          | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO178               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>      | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|-------------------------------|--------------------|-----------------------|------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                               |                    |                       |                  |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| GPIO, IRQ, FlexRay    |                               |                    |                       |                  |           |                       |                      |                                 |                                |                  |     |     |
| 440                   | TCRCLKC_ GPIO440 <sup>9</sup> | P                  | —                     | —                | —         | MH                    | V <sub>DDEH7</sub>   | —/Up                            | —/Up                           | B22              | B26 | F22 |
|                       |                               | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | G                  | GPIO440               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 441                   | ETPUC0_ GPIO441 <sup>9</sup>  | P                  | —                     | —                | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | C21              | C25 | C25 |
|                       |                               | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | G                  | GPIO441               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 442                   | ETPUC1_ GPIO442 <sup>9</sup>  | P                  | —                     | —                | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | D20              | C26 | C26 |
|                       |                               | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | G                  | GPIO442               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 443                   | ETPUC2_ GPIO443 <sup>9</sup>  | P                  | —                     | —                | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | D22              | D25 | D25 |
|                       |                               | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | G                  | GPIO443               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 444                   | ETPUC3_ GPIO444 <sup>9</sup>  | P                  | —                     | —                | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | D21              | D26 | D26 |
|                       |                               | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | G                  | GPIO444               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |
| 445                   | ETPUC4_ GPIO445 <sup>9</sup>  | P                  | —                     | —                | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | E22              | E24 | E24 |
|                       |                               | A1                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                               | G                  | GPIO445               | GPIO             | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>            | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary           | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|-------------------------------------|--------------------|-----------------------|----------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                     |                    |                       |                            |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 446                   | ETPUC5_ GPIO446 <sup>9</sup>        | P                  | —                     | —                          | I/O       | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | E19              | E25 | E25 |
|                       |                                     | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | G                  | GPIO446               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 447                   | ETPUC6_ GPIO447 <sup>9</sup>        | P                  | —                     | —                          | I/O       | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | E26 | E26 |
|                       |                                     | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | G                  | GPIO447               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 448                   | ETPUC7_ GPIO448 <sup>9</sup>        | P                  | —                     | —                          | I/O       | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | F23 | F23 |
|                       |                                     | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | G                  | GPIO448               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 449                   | ETPUC8_ GPIO449 <sup>9</sup>        | P                  | —                     | —                          | I/O       | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | F24 | F24 |
|                       |                                     | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | G                  | GPIO449               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 450                   | ETPUC9_ IRQ0_ GPIO450 <sup>9</sup>  | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | F22              | F25 | F25 |
|                       |                                     | A1                 | IRQ0                  | External interrupt request | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | G                  | GPIO450               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 451                   | ETPUC10_ IRQ1_ GPIO451 <sup>9</sup> | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | E20              | F26 | F26 |
|                       |                                     | A1                 | IRQ1                  | External interrupt request | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                     | G                  | GPIO451               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>                 | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary           | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|------------------------------------------|--------------------|-----------------------|----------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                          |                    |                       |                            |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 452                   | ETPUC11_IRQ2_<br>GPIO452 <sup>9</sup>    | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | E21              | G23 | G22 |
|                       |                                          | A1                 | IRQ2                  | External interrupt request | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | G                  | GPIO452               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 453                   | ETPUC12_IRQ3_<br>GPIO453 <sup>9</sup>    | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | F19              | G24 | G23 |
|                       |                                          | A1                 | IRQ3                  | External interrupt request | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | G                  | GPIO453               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 454                   | ETPUC13_3_IRQ4_<br>GPIO454 <sup>9</sup>  | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | F21              | G25 | G24 |
|                       |                                          | A1                 | IRQ4                  | External interrupt request | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | G                  | GPIO454               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 455                   | ETPUC14_4_IRQ5_<br>GPIO455 <sup>9</sup>  | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | F20              | G26 | G25 |
|                       |                                          | A1                 | IRQ5                  | External interrupt request | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | G                  | GPIO455               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 456                   | ETPUC15_<br>GPIO456 <sup>9</sup>         | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | H23 | G26 |
|                       |                                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | G                  | GPIO456               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 457                   | ETPUC16_FR_A_TX_<br>GPIO457 <sup>9</sup> | P                  | —                     | —                          | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | H24 | H22 |
|                       |                                          | A1                 | FR_A_TX               | FlexRay A transfer         | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                          | G                  | GPIO457               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>                    | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary          | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|---------------------------------------------|--------------------|-----------------------|---------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                             |                    |                       |                           |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 458                   | ETPUC17_FR_A_RX_<br>GPIO458 <sup>9</sup>    | P                  | —                     | —                         | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | G22              | H25 | H23 |
|                       |                                             | A1                 | FR_A_RX               | FlexRay A receive         | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | A2                 | —                     | —                         | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | G                  | GPIO458               | GPIO                      | I/O       |                       |                      |                                 |                                |                  |     |     |
| 459                   | ETPUC18_FR_A_TX_EN_<br>GPIO459 <sup>9</sup> | P                  | —                     | —                         | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | G20              | H26 | H24 |
|                       |                                             | A1                 | FR_A_TX_EN            | FlexRay A transfer enable | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | A2                 | —                     | —                         | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | G                  | GPIO459               | GPIO                      | I/O       |                       |                      |                                 |                                |                  |     |     |
| 460                   | ETPUC19_TXDA_<br>GPIO460 <sup>9</sup>       | P                  | —                     | —                         | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | G21              | J23 | H21 |
|                       |                                             | A1                 | TXDA                  | eSCI A transmit           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | A2                 | —                     | —                         | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | G                  | GPIO460               | GPIO                      | I/O       |                       |                      |                                 |                                |                  |     |     |
| 461                   | ETPUC20_RXDA_<br>GPIO461 <sup>9</sup>       | P                  | —                     | —                         | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | G19              | J24 | H25 |
|                       |                                             | A1                 | RXDA                  | eSCI A receive            | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | A2                 | —                     | —                         | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | G                  | GPIO461               | GPIO                      | I/O       |                       |                      |                                 |                                |                  |     |     |
| 462                   | ETPUC21_TXDB_<br>GPIO462 <sup>9</sup>       | P                  | —                     | —                         | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | H22              | J25 | H26 |
|                       |                                             | A1                 | TXDB                  | eSCI B transmit           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | A2                 | —                     | —                         | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | G                  | GPIO462               | GPIO                      | I/O       |                       |                      |                                 |                                |                  |     |     |
| 463                   | ETPUC22_RXDB_<br>GPIO463 <sup>9</sup>       | P                  | —                     | —                         | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | H21              | J26 | J22 |
|                       |                                             | A1                 | RXDB                  | eSCI B receive            | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | A2                 | —                     | —                         | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                             | G                  | GPIO463               | GPIO                      | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>               | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|----------------------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                        |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 464                   | ETPUC23_PCSD5_<br>GPIO464 <sup>9</sup> | P                  | —                     | —                             | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | H20              | K23 | J23 |
|                       |                                        | A1                 | PCSD5                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A2                 | MAA0                  | ADC A Mux Address 0           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A3                 | MAB0                  | ADC B Mux Address 0           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | G                  | GPIO464               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 465                   | ETPUC24_PCSD4_<br>GPIO465 <sup>9</sup> | P                  | —                     | —                             | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | J22              | K24 | J24 |
|                       |                                        | A1                 | PCSD4                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A2                 | MAA1                  | ADC A Mux Address 1           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A4                 | MAB1                  | ADC B Mux Address 1           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | G                  | GPIO465               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 466                   | ETPUC25_PCSD3_<br>GPIO466 <sup>9</sup> | P                  | —                     | —                             | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | K22              | K25 | K21 |
|                       |                                        | A1                 | PCSD3                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A2                 | MAA2                  | ADC A Mux Address 2           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A3                 | MAB2                  | ADC B Mux Address 2           | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | G                  | GPIO466               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 467                   | ETPUC26_PCSD2_<br>GPIO467 <sup>9</sup> | P                  | —                     | —                             | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | J21              | K26 | J25 |
|                       |                                        | A1                 | PCSD2                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | G                  | GPIO467               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 468                   | ETPUC27_PCSD1_<br>GPIO468 <sup>9</sup> | P                  | —                     | —                             | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | J19              | L23 | J26 |
|                       |                                        | A1                 | PCSD1                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | G                  | GPIO468               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 469                   | ETPUC28_PCSD0_<br>GPIO469 <sup>9</sup> | P                  | —                     | —                             | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | J20              | L24 | K22 |
|                       |                                        | A1                 | PCSD0                 | DSPI D peripheral chip select | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                        | G                  | GPIO469               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>               | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary   | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|----------------------------------------|--------------------|-----------------------|--------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                                        |                    |                       |                    |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 470                   | ETPUC29_SCKD_<br>GPIO470 <sup>9</sup>  | P                  | —                     | —                  | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | K21              | L25  | K23  |
|                       |                                        | A1                 | SCKD                  | DSPI D clock       | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | A2                 | —                     | —                  | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | G                  | GPIO470               | GPIO               | I/O       |                       |                      |                                 |                                |                  |      |      |
| 471                   | ETPUC30_SOUTD_<br>GPIO471 <sup>9</sup> | P                  | —                     | —                  | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | K20              | L26  | K24  |
|                       |                                        | A1                 | SOUTD                 | DSPI D data output | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | A2                 | —                     | —                  | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | G                  | GPIO471               | GPIO               | I/O       |                       |                      |                                 |                                |                  |      |      |
| 472                   | ETPUC31_SIND_<br>GPIO472 <sup>9</sup>  | P                  | —                     | —                  | —         | MH                    | V <sub>DDEH7</sub>   | —/WKPCFG                        | —/WKPCFG                       | K19              | M23  | K25  |
|                       |                                        | A1                 | SIND                  | DSPI D data input  | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | A2                 | —                     | —                  | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | G                  | GPIO472               | GPIO               | I/O       |                       |                      |                                 |                                |                  |      |      |
| eMIOS                 |                                        |                    |                       |                    |           |                       |                      |                                 |                                |                  |      |      |
| 179                   | EMIOS0_ETPUA0_<br>GPIO179              | P                  | EMIOS0                | eMIOS channel      | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA9              | AE10 | AC13 |
|                       |                                        | A1                 | ETPUA0                | eTPU A channel     | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | A2                 | —                     | —                  | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | G                  | GPIO179               | GPIO               | I/O       |                       |                      |                                 |                                |                  |      |      |
| 180                   | EMIOS1_ETPUA1_<br>GPIO180              | P                  | EMIOS1                | eMIOS channel      | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB9              | AF10 | AB13 |
|                       |                                        | A1                 | ETPUA1                | eTPU A channel     | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | A2                 | —                     | —                  | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | G                  | GPIO180               | GPIO               | I/O       |                       |                      |                                 |                                |                  |      |      |
| 181                   | EMIOS2_ETPUA2_<br>GPIO181              | P                  | EMIOS2                | eMIOS channel      | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y10              | AD11 | AD13 |
|                       |                                        | A1                 | ETPUA2                | eTPU A channel     | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | A2                 | —                     | —                  | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                        | G                  | GPIO181               | GPIO               | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>  | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|---------------------------|--------------------|-----------------------|------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                           |                    |                       |                  |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 182                   | EMIOS3_ETPUA3_<br>GPIO182 | P                  | EMIOS3                | eMIOS channel    | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA10             | AE11 | AE13 |
|                       |                           | A1                 | ETPUA3                | eTPU A channel   | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | G                  | GPIO182               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 183                   | EMIOS4_ETPUA4_<br>GPIO183 | P                  | EMIOS4                | eMIOS channel    | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB10             | AF11 | AF13 |
|                       |                           | A1                 | ETPUA4                | eTPU A channel   | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | G                  | GPIO183               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 184                   | EMIOS5_ETPUA5_<br>GPIO184 | P                  | EMIOS5                | eMIOS channel    | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y11              | AD12 | AF14 |
|                       |                           | A1                 | ETPUA5                | eTPU A channel   | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | G                  | GPIO184               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 185                   | EMIOS6_ETPUA6_<br>GPIO185 | P                  | EMIOS6                | eMIOS channel    | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | —                | AE12 | AE14 |
|                       |                           | A1                 | ETPUA6                | eTPU A channel   | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | G                  | GPIO185               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 186                   | EMIOS7_ETPUA7_<br>GPIO186 | P                  | EMIOS7                | eMIOS channel    | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB11             | AF12 | AD14 |
|                       |                           | A1                 | ETPUA7                | eTPU A channel   | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | G                  | GPIO186               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |
| 187                   | EMIOS8_ETPUA8_<br>GPIO187 | P                  | EMIOS8                | eMIOS channel    | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | W10              | AC13 | AC14 |
|                       |                           | A1                 | ETPUA8                | eTPU A channel   | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | A2                 | —                     | —                | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                           | G                  | GPIO187               | GPIO             | I/O       |                       |                      |                                 |                                |                  |      |      |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary           | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|----------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                            |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 188                   | EMIOS9_ETPUA9_GPIO188    | P                  | EMIOS9                | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | W11              | AD13 | AF15 |
|                       |                          | A1                 | ETPUA9                | eTPU A channel             | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO188               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 189                   | EMIOS10_SCKD_GPIO189     | P                  | EMIOS10               | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA11             | AE13 | AE15 |
|                       |                          | A1                 | SCKD                  | DSPI D clock               | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO189               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 190                   | EMIOS11_SIND_GPIO190     | P                  | EMIOS11               | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB12             | AF13 | AB14 |
|                       |                          | A1                 | SIND                  | DSPI D data input          | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO190               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 191                   | EMIOS12_SOUTC_GPIO191    | P                  | EMIOS12               | eMIOS channel              | O         | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB13             | AF14 | AD15 |
|                       |                          | A1                 | SOUTC                 | DSPI C data output         | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO191               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 192                   | EMIOS13_SOUTD_GPIO192    | P                  | EMIOS13               | eMIOS channel              | O         | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA12             | AE14 | AC15 |
|                       |                          | A1                 | SOUTD                 | DSPI D data output         | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO192               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 193                   | EMIOS14_IRQ0_GPIO193     | P                  | EMIOS14               | eMIOS channel              | O         | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y12              | AC14 | AF17 |
|                       |                          | A1                 | IRQ0                  | External interrupt request | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | CNTXD                 | FlexCAN D transmit         | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO193               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary           | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|----------------------------|--------------------|-----------------------|----------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                            |                    |                       |                            |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 194                   | EMIOS15_IRQ1_<br>GPIO194   | P                  | EMIOS15               | eMIOS channel              | O         | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y13              | AD14 | AE16 |
|                       |                            | A1                 | IRQ1                  | External interrupt request | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | CNRXD                 | FlexCAN D receive          | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO194               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 195                   | EMIOS16_ETPUB0_<br>GPIO195 | P                  | EMIOS16               | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB14             | AF15 | AD16 |
|                       |                            | A1                 | ETPUB0                | eTPU B channel             | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | FR_DBG[3]             | FlexRay debug              | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO195               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 196                   | EMIOS17_ETPUB1_<br>GPIO196 | P                  | EMIOS17               | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA13             | AE15 | AB15 |
|                       |                            | A1                 | ETPUB1                | eTPU B channel             | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | FR_DBG[2]             | FlexRay debug              | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO196               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 197                   | EMIOS18_ETPUB2_<br>GPIO197 | P                  | EMIOS18               | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | W12              | AC15 | AD17 |
|                       |                            | A1                 | ETPUB2                | eTPU B channel             | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | FR_DBG[1]             | FlexRay debug              | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO197               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 198                   | EMIOS19_ETPUB3_<br>GPIO198 | P                  | EMIOS19               | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y14              | AD15 | AB16 |
|                       |                            | A1                 | ETPUB3                | eTPU B channel             | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | FR_DBG[0]             | FlexRay debug              | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO198               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |
| 199                   | EMIOS20_ETPUB4_<br>GPIO199 | P                  | EMIOS20               | eMIOS channel              | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB15             | AF16 | AF16 |
|                       |                            | A1                 | ETPUB4                | eTPU B channel             | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO199               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |      |      |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|----------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                            |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 200                   | EMIOS21_ETPUB5_<br>GPIO200 | P                  | EMIOS21               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA14             | AE16 | AE17 |
|                       |                            | A1                 | ETPUB5                | eTPU B channel                | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO200               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 201                   | EMIOS22_ETPUB6_<br>GPIO201 | P                  | EMIOS22               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | W13              | AC16 | AC16 |
|                       |                            | A1                 | ETPUB6                | eTPU B channel                | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO201               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 202                   | EMIOS23_ETPUB7_<br>GPIO202 | P                  | EMIOS23               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y15              | AD16 | AA16 |
|                       |                            | A1                 | ETPUB7                | eTPU B channel                | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO202               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 203                   | EMIOS24_PCSB0_<br>GPIO203  | P                  | EMIOS24               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AB16             | AF17 | AC17 |
|                       |                            | A1                 | PCSB0                 | DSPI B peripheral chip select | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO203               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 204                   | EMIOS25_PCSB1_<br>GPIO204  | P                  | EMIOS25               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA15             | AE17 | AF18 |
|                       |                            | A1                 | PCSB1                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO204               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 432                   | EMIOS26_PCSB2_<br>GPIO432  | P                  | EMIOS26               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y16              | AD17 | AE18 |
|                       |                            | A1                 | PCSB2                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO432               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 433                   | EMIOS27_PCSB3_GPIO433    | P                  | EMIOS27               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | W14              | AC17 | AD18 |
|                       |                          | A1                 | PCSB3                 | DSPI B peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO433               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 434                   | EMIOS28_PCSC0_GPIO434    | P                  | EMIOS28               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA16             | AF18 | AC18 |
|                       |                          | A1                 | PCSC0                 | DSPI C peripheral chip select | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO434               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 435                   | EMIOS29_PCSC1_GPIO435    | P                  | EMIOS29               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | AA17             | AE18 | AB17 |
|                       |                          | A1                 | PCSC1                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO435               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 436                   | EMIOS30_PCSC2_GPIO436    | P                  | EMIOS30               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | Y17              | AD18 | AF19 |
|                       |                          | A1                 | PCSC2                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO436               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 437                   | EMIOS31_PCSC5_GPIO437    | P                  | EMIOS31               | eMIOS channel                 | I/O       | MH                    | V <sub>DDEH4</sub>   | —/WKPCFG                        | —/WKPCFG                       | W15              | AC18 | AA17 |
|                       |                          | A1                 | PCSC5                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO437               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| eQADC                 |                          |                    |                       |                               |           |                       |                      |                                 |                                |                  |      |      |
| —                     | ANA0                     | P                  | ANA0 <sup>10</sup>    | eQADC A analog input          | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA0                            | ANA0                           | A4               | A4   | A4   |
| —                     | ANA1                     | P                  | ANA1 <sup>10</sup>    | eQADC A analog input          | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA1                            | ANA1                           | A5               | B5   | B5   |
| —                     | ANA2                     | P                  | ANA2 <sup>10</sup>    | eQADC A analog input          | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA2                            | ANA2                           | B5               | C5   | C5   |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                  | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-----------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                   |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| —                     | ANA3                     | P                  | ANA3 <sup>10</sup>    | eQADC A analog input              | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA3                            | ANA3                           | B6               | D6  | D6  |
| —                     | ANA4                     | P                  | ANA4 <sup>10</sup>    | eQADC A analog input              | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA4                            | ANA4                           | A6               | A5  | A5  |
| —                     | ANA5                     | P                  | ANA5 <sup>10</sup>    | eQADC A analog input              | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA5                            | ANA5                           | A7               | B6  | B6  |
| —                     | ANA6                     | P                  | ANA6 <sup>10</sup>    | eQADC A analog input              | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA6                            | ANA6                           | B7               | C6  | C6  |
| —                     | ANA7                     | P                  | ANA7 <sup>10</sup>    | eQADC A analog input              | I         | AE/up-down            | V <sub>DDA_A1</sub>  | ANA7                            | ANA7                           | B8               | D7  | C7  |
| —                     | ANA8                     | P                  | ANA8                  | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA8                            | ANA8                           | C5               | A6  | D7  |
| —                     | ANA9                     | P                  | ANA9                  | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA9                            | ANA9                           | C7               | C7  | A6  |
| —                     | ANA10                    | P                  | ANA10                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA10                           | ANA10                          | C6               | B7  | B7  |
| —                     | ANA11                    | P                  | ANA11                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA11                           | ANA11                          | D6               | A7  | A7  |
| —                     | ANA12                    | P                  | ANA12                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA12                           | ANA12                          | D7               | D8  | D8  |
| —                     | ANA13                    | P                  | ANA13                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA13                           | ANA13                          | C8               | C8  | C8  |
| —                     | ANA14                    | P                  | ANA14                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA14                           | ANA14                          | D8               | B8  | B8  |
| —                     | ANA15                    | P                  | ANA15                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA15                           | ANA15                          | A8               | A8  | A8  |
| —                     | ANA16                    | P                  | ANA16                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA16                           | ANA16                          | D9               | D9  | D9  |
| —                     | ANA17                    | P                  | ANA17                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA17                           | ANA17                          | C9               | C9  | C9  |
| —                     | ANA18                    | P                  | ANA18                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA18                           | ANA18                          | D10              | D10 | D10 |
| —                     | ANA19                    | P                  | ANA19                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA19                           | ANA19                          | C10              | C10 | C10 |
| —                     | ANA20                    | P                  | ANA20                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA20                           | ANA20                          | D11              | D11 | D11 |
| —                     | ANA21                    | P                  | ANA21                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA21                           | ANA21                          | C11              | C11 | C11 |
| —                     | ANA22                    | P                  | ANA22                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA22                           | ANA22                          | D12              | D12 | C12 |
| —                     | ANA23                    | P                  | ANA23                 | eQADC A analog input              | I         | AE                    | V <sub>DDA_A1</sub>  | ANA23                           | ANA23                          | C12              | C12 | D12 |
| —                     | AN24                     | P                  | AN24                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_A0</sub>  | AN24                            | AN24                           | —                | B12 | B12 |
| —                     | AN25                     | P                  | AN25                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_A0</sub>  | AN25                            | AN25                           | —                | D13 | C13 |
| —                     | AN26                     | P                  | AN26                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_A0</sub>  | AN26                            | AN26                           | —                | C13 | D13 |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                  | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-----------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                   |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| —                     | AN27                     | P                  | AN27                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_A0</sub>  | AN27                            | AN27                           | —                | B13 | B13 |
| —                     | AN28                     | P                  | AN28                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_A0</sub>  | AN28                            | AN28                           | —                | A13 | A13 |
| —                     | AN29                     | P                  | AN29                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_A0</sub>  | AN29                            | AN29                           | —                | B14 | A14 |
| —                     | AN30                     | P                  | AN30                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B1</sub>  | AN30                            | AN30                           | —                | C14 | B14 |
| —                     | AN31                     | P                  | AN31                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B1</sub>  | AN31                            | AN31                           | —                | D14 | C14 |
| —                     | AN32                     | P                  | AN32                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B1</sub>  | AN32                            | AN32                           | —                | A14 | B15 |
| —                     | AN33                     | P                  | AN33                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B0</sub>  | AN33                            | AN33                           | —                | B15 | D14 |
| —                     | AN34                     | P                  | AN34                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B0</sub>  | AN34                            | AN34                           | —                | C15 | C15 |
| —                     | AN35                     | P                  | AN35                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B0</sub>  | AN35                            | AN35                           | —                | D15 | D15 |
| —                     | AN36                     | P                  | AN36                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B1</sub>  | AN36                            | AN36                           | —                | A15 | A15 |
| —                     | AN37                     | P                  | AN37                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B0</sub>  | AN37                            | AN37                           | —                | C16 | C17 |
| —                     | AN38                     | P                  | AN38                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B0</sub>  | AN38                            | AN38                           | —                | C17 | D16 |
| —                     | AN39                     | P                  | AN39                  | eQADC A and B shared analog input | I         | AE                    | V <sub>DDA_B0</sub>  | AN39                            | AN39                           | —                | D16 | C16 |
| —                     | ANB0                     | P                  | ANB0                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB0                            | ANB0                           | B15              | C18 | C18 |
| —                     | ANB1                     | P                  | ANB1                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB1                            | ANB1                           | B16              | D17 | D17 |
| —                     | ANB2                     | P                  | ANB2                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB2                            | ANB2                           | A17              | D18 | D18 |
| —                     | ANB3                     | P                  | ANB3                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB3                            | ANB3                           | A18              | D19 | D19 |
| —                     | ANB4                     | P                  | ANB4                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB4                            | ANB4                           | B17              | C19 | B19 |
| —                     | ANB5                     | P                  | ANB5                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB5                            | ANB5                           | B18              | C20 | A20 |
| —                     | ANB6                     | P                  | ANB6                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB6                            | ANB6                           | A19              | B19 | C20 |
| —                     | ANB7                     | P                  | ANB7                  | eQADC B analog input              | I         | AE/up-down            | V <sub>DDA_B0</sub>  | ANB7                            | ANB7                           | A20              | A20 | C19 |
| —                     | ANB8                     | P                  | ANB8                  | eQADC B analog input              | I         | AE                    | V <sub>DDA_B0</sub>  | ANB8                            | ANB8                           | D13              | B20 | B20 |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                 | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|----------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                  |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| —                     | ANB9                     | P                  | ANB9                  | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB9                            | ANB9                           | C14              | D20 | A21 |
| —                     | ANB10                    | P                  | ANB10                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB10                           | ANB10                          | C13              | B21 | B21 |
| —                     | ANB11                    | P                  | ANB11                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB11                           | ANB11                          | C15              | A21 | C21 |
| —                     | ANB12                    | P                  | ANB12                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB12                           | ANB12                          | C16              | C21 | A22 |
| —                     | ANB13                    | P                  | ANB13                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB13                           | ANB13                          | D14              | D21 | B22 |
| —                     | ANB14                    | P                  | ANB14                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB14                           | ANB14                          | C17              | A22 | D20 |
| —                     | ANB15                    | P                  | ANB15                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB15                           | ANB15                          | D15              | B22 | C22 |
| —                     | ANB16                    | P                  | ANB16                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB16                           | ANB16                          | C18              | C22 | D21 |
| —                     | ANB17                    | P                  | ANB17                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB17                           | ANB17                          | D16              | A23 | D22 |
| —                     | ANB18                    | P                  | ANB18                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB18                           | ANB18                          | D17              | B23 | A23 |
| —                     | ANB19                    | P                  | ANB19                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB19                           | ANB19                          | B19              | C23 | B23 |
| —                     | ANB20                    | P                  | ANB20                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB20                           | ANB20                          | C19              | D22 | C23 |
| —                     | ANB21                    | P                  | ANB21                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB21                           | ANB21                          | D18              | A24 | A24 |
| —                     | ANB22                    | P                  | ANB22                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB22                           | ANB22                          | A21              | B24 | B24 |
| —                     | ANB23                    | P                  | ANB23                 | eQADC B analog input             | I         | AE                    | V <sub>DDA_B0</sub>  | ANB23                           | ANB23                          | B20              | A25 | E20 |
| —                     | VRH_A                    | P                  | VRH_A                 | ADC A Voltage reference high     | I         | VDDINT                | V <sub>RH_A</sub>    | VRH_A                           | VRH_A                          | A10              | A12 | A12 |
| —                     | VRL_A                    | P                  | VRL_A                 | ADC A Voltage reference low      | I         | VSSINT                | V <sub>RL_A</sub>    | VRL_A                           | VRL_A                          | A11              | A11 | A11 |
| —                     | VRH_B                    | P                  | VRH_B                 | ADC B Voltage reference high     | I         | VDDINT                | V <sub>RH_B</sub>    | VRH_B                           | VRH_B                          | A16              | A19 | A19 |
| —                     | VRL_B                    | P                  | VRL_B                 | ADC B Voltage reference low      | I         | VSSINT                | V <sub>RL_B</sub>    | VRL_B                           | VRL_B                          | A15              | A18 | A18 |
| —                     | REFBYPCB                 | P                  | REFBYPCB              | ADC B Reference bypass capacitor | I         | AE                    | V <sub>DDA_B0</sub>  | REFBYPCB                        | REFBYPCB                       | B12              | B18 | B18 |
| —                     | REFBYPCA                 | P                  | REFBYPCA              | ADC A Reference bypass capacitor | I         | AE                    | V <sub>DDA_A1</sub>  | REFBYPCA                        | REFBYPCA                       | B11              | B11 | B11 |
| —                     | VDDA_A0                  | P                  | VDDA_A                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_A0</sub>  | VDDA_A0                         | VDDA_A0                        | A9               | A9  | A9  |
| —                     | VDDA_A1                  | P                  | VDDA_A                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_A1</sub>  | VDDA_A1                         | VDDA_A1                        | B9               | B9  | B9  |
| —                     | REFBYPCA1                | P                  | REFBYPCA1             | ADC A Reference bypass capacitor | I         | AE                    | V <sub>DDA_A1</sub>  | REFBYPCA1                       | REFBYPCA1                      | A12              | A10 | A10 |
| —                     | VSSA_A1                  | P                  | VSSA_A                | Ground                           | I         | VSSE                  | V <sub>SSA_A1</sub>  | VSSA_A1                         | VSSA_A1                        | B10              | B10 | B10 |
| —                     | VDDA_B0                  | P                  | VDDA_B                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_B0</sub>  | VDDA_B0                         | VDDA_B0                        | A13              | A16 | A16 |
| —                     | VDDA_B1                  | P                  | VDDA_B                | Internal logic supply input      | I         | VDDE                  | V <sub>DDA_B1</sub>  | VDDA_B1                         | VDDA_B1                        | B13              | B16 | B16 |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                 | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup>          | State after RESET <sup>8</sup>           | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|----------------------------------|-----------|-----------------------|----------------------|------------------------------------------|------------------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                  |           |                       |                      |                                          |                                          | 324              | 416 | 516 |
| —                     | VSSA_B0                  | P                  | VSSA_B                | Ground                           | I         | VSSE                  | V <sub>SSA_B0</sub>  | VSSA_B0                                  | VSSA_B0                                  | B14              | B17 | B17 |
| —                     | REFBYPCB1                | P                  | REFBYPCB1             | ADC B Reference bypass capacitor | I         | AE                    | V <sub>DDA_B0</sub>  | REFBYPCB1                                | REFBYPCB1                                | A14              | A17 | A17 |
| FlexRay               |                          |                    |                       |                                  |           |                       |                      |                                          |                                          |                  |     |     |
| 248                   | FR_A_TX_<br>GPIO248      | P                  | FR_A_TX               | FlexRay A transfer               | O         | FS                    | V <sub>DDE2</sub>    | —/Up<br>(—/— for Rev.1 of<br>the device) | —/Up<br>(—/— for Rev.1 of<br>the device) | Y5               | AD4 | AD4 |
|                       |                          | A1                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | A2                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | G                  | GPIO248               | GPIO                             | I/O       |                       |                      |                                          |                                          |                  |     |     |
| 249                   | FR_A_RX_<br>GPIO249      | P                  | FR_A_RX               | FlexRay A receive                | I         | FS                    | V <sub>DDE2</sub>    | —/Up<br>(—/— for Rev.1 of<br>the device) | —/Up<br>(—/— for Rev.1 of<br>the device) | AA4              | AE3 | AE3 |
|                       |                          | A1                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | A2                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | G                  | GPIO249               | GPIO                             | I/O       |                       |                      |                                          |                                          |                  |     |     |
| 250                   | FR_A_TX_EN_<br>GPIO250   | P                  | FR_A_TX_EN            | FlexRay A transfer enable        | O         | FS                    | V <sub>DDE2</sub>    | —/Up<br>(—/— for Rev.1 of<br>the device) | —/Up<br>(—/— for Rev.1 of<br>the device) | AB3              | AF3 | AF3 |
|                       |                          | A1                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | A2                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | G                  | GPIO250               | GPIO                             | I/O       |                       |                      |                                          |                                          |                  |     |     |
| 251                   | FR_B_TX_<br>GPIO251      | P                  | FR_B_TX               | FlexRay B transfer               | O         | FS                    | V <sub>DDE2</sub>    | —/Up<br>(—/— for Rev.1 of<br>the device) | —/Up<br>(—/— for Rev.1 of<br>the device) | Y6               | AD5 | AD5 |
|                       |                          | A1                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | A2                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | G                  | GPIO251               | GPIO                             | I/O       |                       |                      |                                          |                                          |                  |     |     |
| 252                   | FR_B_RX_<br>GPIO252      | P                  | FR_B_RX               | FlexRay B receive                | I         | FS                    | V <sub>DDE2</sub>    | —/Up<br>(—/— for Rev.1 of<br>the device) | —/Up<br>(—/— for Rev.1 of<br>the device) | AA5              | AE4 | AE4 |
|                       |                          | A1                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | A2                 | —                     | —                                | —         |                       |                      |                                          |                                          |                  |     |     |
|                       |                          | G                  | GPIO252               | GPIO                             | I/O       |                       |                      |                                          |                                          |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup>       | State after RESET <sup>8</sup>        | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------------|---------------------------------------|------------------|------|------|
|                       |                          |                    |                       |                               |           |                       |                      |                                       |                                       | 324              | 416  | 516  |
| 253                   | FR_B_TX_EN_<br>GPIO253   | P                  | FR_B_TX_EN            | FlexRay B transfer enable     | O         | FS                    | V <sub>DDE2</sub>    | —/Up<br>(—/— for Rev.1 of the device) | —/Up<br>(—/— for Rev.1 of the device) | AB5              | AF4  | AF4  |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | G                  | GPIO253               | GPIO                          | I/O       |                       |                      |                                       |                                       |                  |      |      |
| FlexCAN               |                          |                    |                       |                               |           |                       |                      |                                       |                                       |                  |      |      |
| 83                    | CNTXA_TXDA_<br>GPIO83    | P                  | CNTXA                 | FlexCAN A transmit            | O         | MH                    | V <sub>DDEH4</sub>   | —/Up                                  | —/Up                                  | AB17             | AF19 | AE19 |
|                       |                          | A1                 | TXDA                  | eSCI A transmit               | O         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | G                  | GPIO83                | GPIO                          | I/O       |                       |                      |                                       |                                       |                  |      |      |
| 84                    | CNRXA_RXDA_<br>GPIO84    | P                  | CNRXA                 | FlexCAN A receive             | I         | MH                    | V <sub>DDEH4</sub>   | —/Up                                  | —/Up                                  | AA18             | AE19 | AD19 |
|                       |                          | A1                 | RXDA                  | eSCI A receive                | I         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | G                  | GPIO84                | GPIO                          | I/O       |                       |                      |                                       |                                       |                  |      |      |
| 85                    | CNTXB_PCSC3_<br>GPIO85   | P                  | CNTXB                 | FlexCAN B transmit            | O         | MH                    | V <sub>DDEH4</sub>   | —/Up                                  | —/Up                                  | Y18              | AD19 | AC19 |
|                       |                          | A1                 | PCSC3                 | DSPI C peripheral chip select | O         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | G                  | GPIO85                | GPIO                          | I/O       |                       |                      |                                       |                                       |                  |      |      |
| 86                    | CNRXB_PCSC4_<br>GPIO86   | P                  | CNRXB                 | FlexCAN B receive             | I         | MH                    | V <sub>DDEH4</sub>   | —/Up                                  | —/Up                                  | W18              | AC19 | AA19 |
|                       |                          | A1                 | PCSC4                 | DSPI C peripheral chip select | O         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | G                  | GPIO86                | GPIO                          | I/O       |                       |                      |                                       |                                       |                  |      |      |
| 87                    | CNTXC_PCSD3_<br>GPIO87   | P                  | CNTXC                 | FlexCAN C transmit            | O         | MH                    | V <sub>DDEH4</sub>   | —/Up                                  | —/Up                                  | W16              | AF20 | AF20 |
|                       |                          | A1                 | PCSD3                 | DSPI D peripheral chip select | O         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                       |                                       |                  |      |      |
|                       |                          | G                  | GPIO87                | GPIO                          | I/O       |                       |                      |                                       |                                       |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 88                    | CNRXC_PCSD4_GPIO88       | P                  | CNRXC                 | FlexCAN C receive             | I         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | W17              | AE20 | AE20 |
|                       |                          | A1                 | PCSD4                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO88                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 246                   | CNTXD_GPIO246            | P                  | CNTXD                 | FlexCAN D transmit            | O         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AB21             | AD20 | AD20 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO246               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 247                   | CNRXD_GPIO247            | P                  | CNRXD                 | FlexCAN D receive             | I         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | Y19              | AC20 | AC20 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO247               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| eSCI                  |                          |                    |                       |                               |           |                       |                      |                                 |                                |                  |      |      |
| 89                    | TXDA_GPIO89              | P                  | TXDA                  | eSCI A transmit               | O         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | —                | M2   | K2   |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO89                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 90                    | RXDA_GPIO90              | P                  | RXDA                  | eSCI A receive                | I         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | —                | M3   | K3   |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO90                | GPIO                          | I         |                       |                      |                                 |                                |                  |      |      |
| 91                    | TXDB_PCSD1_GPIO91        | P                  | TXDB                  | eSCI B transmit               | O         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | —                | P1   | K1   |
|                       |                          | A1                 | PCSD1                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO91                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 92                    | RXDB_PCSD5_ GPIO92       | P                  | RXDB                  | eSCI B receive                | I         | MH                    | V <sub>DDEH1</sub>   | —/Up                            | —/Up                           | —                | N1   | L5   |
|                       |                          | A1                 | PCSD5                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO92                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 244                   | TXDC_ETRIG0_ GPIO244     | P                  | TXDC                  | eSCI C transmit               | O         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | —                | AF23 | AF23 |
|                       |                          | A1                 | ETRIG0                | eQADC trigger input           | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO244               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 245                   | RXDC_ GPIO245            | P                  | RXDC                  | eSCI C receive                | I         | MH                    | V <sub>DDEH5</sub>   | —/Up                            | —/Up                           | —                | AD22 | AD22 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO245               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| DSPI                  |                          |                    |                       |                               |           |                       |                      |                                 |                                |                  |      |      |
| 93                    | SCKA_PCSC1_ GPIO93       | P                  | SCKA                  | DSPI A clock                  | I/O       | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | Y7               | AD8  | AB8  |
|                       |                          | A1                 | PCSC1                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO93                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 94                    | SINA_PCSC2_ GPIO94       | P                  | SINA                  | DSPI A data input             | I         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AA7              | AF7  | AE7  |
|                       |                          | A1                 | PCSC2                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO94                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 95                    | SOUTA_PCSC5_ GPIO95      | P                  | SOUTA                 | DSPI A data output            | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AB7              | AD7  | AC7  |
|                       |                          | A1                 | PCSC5                 | DSPI C peripheral chip select | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO95                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 96                    | PCSA0_PCSD2_<br>GPIO96   | P                  | PCSA0                 | DSPI A peripheral chip select | I/O       | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AB6              | AE6 | AD6 |
|                       |                          | A1                 | PCSD2                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO96                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 97                    | PCSA1_<br>GPIO97         | P                  | PCSA1                 | DSPI A peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AC6 | AC6 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO97                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 98                    | PCSA2_<br>GPIO98         | P                  | PCSA2                 | DSPI A peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AC7 | AF6 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO98                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 99                    | PCSA3_<br>GPIO99         | P                  | PCSA3                 | DSPI A peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AE7 | AD7 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO99                | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 100                   | PCSA4_<br>GPIO100        | P                  | PCSA4                 | DSPI A peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AE5 | AE5 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO100               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |
| 101                   | PCSA5_ETRIG1_<br>GPIO101 | P                  | PCSA5                 | DSPI A peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AA6              | AD6 | AA8 |
|                       |                          | A1                 | ETRIG1                | eQADC trigger input           | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO101               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |      |
|-----------------------|--------------------------|--------------------|-----------------------|-------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|------|
|                       |                          |                    |                       |                               |           |                       |                      |                                 |                                | 324              | 416 | 516  |
| 102                   | SCKB_<br>GPIO102         | P                  | SCKB                  | DSPI B clock                  | I/O       | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | Y8               | AE8 | AC8  |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO102               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 103                   | SINB_<br>GPIO103         | P                  | SINB                  | DSPI B data input             | I         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AA8              | AE9 | AB9  |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO103               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 104                   | SOUTB_<br>GPIO104        | P                  | SOUTB                 | DSPI B data output            | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | AB8              | AF9 | AA10 |
|                       |                          | A1                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO104               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 105                   | PCSB0_PCSD2_<br>GPIO105  | P                  | PCSB0                 | DSPI B peripheral chip select | I/O       | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | Y9               | AD9 | AF8  |
|                       |                          | A1                 | PCSD2                 | DSPI D peripheral chip select | O         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO105               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 106                   | PCSB1_PCSD0_<br>GPIO106  | P                  | PCSB1                 | DSPI B peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AC9 | AE8  |
|                       |                          | A1                 | PCSD0                 | DSPI D peripheral chip select | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO106               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |
| 107                   | PCSB2_SOUTC_<br>GPIO107  | P                  | PCSB2                 | DSPI B peripheral chip select | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | W7               | AF8 | AD8  |
|                       |                          | A1                 | SOUTC                 | DSPI C data output            | O         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                             | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO107               | GPIO                          | I/O       |                       |                      |                                 |                                |                  |     |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>       | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                              | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------------|--------------------|-----------------------|-----------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                                |                    |                       |                                               |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 108                   | PCSB3_SINC_<br>GPIO108         | P                  | PCSB3                 | DSPI B peripheral chip select                 | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AD10 | AC9  |
|                       |                                | A1                 | SINC                  | DSPI C data input                             | I         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO108               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 109                   | PCSB4_SCKC_<br>GPIO109         | P                  | PCSB4                 | DSPI B peripheral chip select                 | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AC8  | AF7  |
|                       |                                | A1                 | SCKC                  | DSPI C clock                                  | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO109               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 110                   | PCSB5_PCSC0_<br>GPIO110        | P                  | PCSB5                 | DSPI B peripheral chip select                 | O         | MH                    | V <sub>DDEH3</sub>   | —/Up                            | —/Up                           | —                | AF6  | AE6  |
|                       |                                | A1                 | PCSC0                 | DSPI C peripheral chip select                 | I/O       |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO110               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 235                   | SCKC_SCK_C_LVDSP_<br>GPIO235   | P                  | SCKC                  | DSPI C clock                                  | I/O       | MH+<br>LVDS           | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AA19             | AD21 | AD21 |
|                       |                                | A1                 | SCK_C_LVDSP           | LVDS+ downstream signal positive output clock | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO235               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 236                   | SINC_SCK_C_LVDSM_<br>GPIO236   | P                  | SINC                  | DSPI C data input                             | I         | MH+<br>LVDS           | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AA20             | AE22 | AE22 |
|                       |                                | A1                 | SCK_C_LVDSM           | LVDS– downstream signal negative output clock | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO236               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |
| 237                   | SOUTC_SOUT_C_LVDSP_<br>GPIO237 | P                  | SOUTC                 | DSPI C data output                            | O         | MH+<br>LVDS           | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AB18             | AF21 | AF21 |
|                       |                                | A1                 | SOUT_C_LVDSP          | LVDS+ downstream signal positive output data  | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | A2                 | —                     | —                                             | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                                | G                  | GPIO237               | GPIO                                          | I/O       |                       |                      |                                 |                                |                  |      |      |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>   | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                             | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|----------------------------|--------------------|-----------------------|----------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                            |                    |                       |                                              |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 238                   | PCSC0_SOUT_C_LVDSM_GPIO238 | P                  | PCSC0                 | DSPI C peripheral chip select                | I/O       | MH+ LVDS              | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | AB19             | AE21 | AE21 |
|                       |                            | A1                 | SOUT_C_LVDSM          | LVDS– downstream signal negative output data | O         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO238               | GPIO                                         | I/O       |                       |                      |                                 |                                |                  |      |      |
| 239                   | PCSC1_GPIO239              | P                  | PCSC1                 | DSPI C peripheral chip select                | O         | MH                    | V <sub>DDEH4</sub>   | —/Up                            | —/Up                           | —                | AC22 | AC22 |
|                       |                            | A1                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO239               | GPIO                                         | I/O       |                       |                      |                                 |                                |                  |      |      |
| 240                   | PCSC2_GPIO240              | P                  | PCSC2                 | DSPI C peripheral chip select                | O         | MH                    | V <sub>DDEH5</sub>   | —/Up                            | —/Up                           | —                | AE23 | AE23 |
|                       |                            | A1                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO240               | GPIO                                         | I/O       |                       |                      |                                 |                                |                  |      |      |
| 241                   | PCSC3_GPIO241              | P                  | PCSC3                 | DSPI C peripheral chip select                | O         | MH                    | V <sub>DDEH5</sub>   | —/Up                            | —/Up                           | —                | AD23 | AD23 |
|                       |                            | A1                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO241               | GPIO                                         | I/O       |                       |                      |                                 |                                |                  |      |      |
| 242                   | PCSC4_GPIO242              | P                  | PCSC4                 | DSPI C peripheral chip select                | O         | MH                    | V <sub>DDEH5</sub>   | —/Up                            | —/Up                           | —                | AF24 | AF24 |
|                       |                            | A1                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO242               | GPIO                                         | I/O       |                       |                      |                                 |                                |                  |      |      |
| 243                   | PCSC5_GPIO243              | P                  | PCSC5                 | DSPI C peripheral chip select                | O         | MH                    | V <sub>DDEH5</sub>   | —/Up                            | —/Up                           | —                | AE24 | AE24 |
|                       |                            | A1                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | A2                 | —                     | —                                            | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                            | G                  | GPIO243               | GPIO                                         | I/O       |                       |                      |                                 |                                |                  |      |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>      | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during<br>RESET <sup>7</sup> | State<br>after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|-------------------------------|--------------------|-----------------------|-----------------------------------------------------------------|-----------|-----------------------|----------------------|------------------------------------|-----------------------------------|------------------|-----|-----|
|                       |                               |                    |                       |                                                                 |           |                       |                      |                                    |                                   | 324              | 416 | 516 |
| EBI                   |                               |                    |                       |                                                                 |           |                       |                      |                                    |                                   |                  |     |     |
| 256                   | D_CS0_<br>GPIO256             | P                  | D_CS0                 | EBI chip select 0                                               | O         | F                     | V <sub>DDE9</sub>    | —/Up                               | —/Up                              | —                | —   | AD9 |
|                       |                               | A1                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | A2                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | G                  | GPIO256               | GPIO                                                            | I/O       |                       |                      |                                    |                                   |                  |     |     |
| 257                   | D_CS2_D_ADD_DAT31_<br>GPIO257 | P                  | D_CS2                 | EBI chip select 2                                               | O         | F                     | V <sub>DDE8</sub>    | —/Up                               | —/Up                              | —                | —   | U1  |
|                       |                               | A1                 | D_ADD_DAT31           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | A2                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | G                  | GPIO257               | GPIO                                                            | I/O       |                       |                      |                                    |                                   |                  |     |     |
| 258                   | D_CS3_D_TEA_<br>GPIO258       | P                  | D_CS3                 | EBI chip select 3                                               | O         | F                     | V <sub>DDE8</sub>    | —/Up                               | —/Up                              | —                | —   | T6  |
|                       |                               | A1                 | D_TEA                 | EBI transfer error acknowledge                                  | I         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | A2                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | G                  | GPIO258               | GPIO                                                            | I/O       |                       |                      |                                    |                                   |                  |     |     |
| 259                   | D_ADD12_<br>GPIO259           | P                  | D_ADD12               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                               | —/Up                              | —                | —   | R1  |
|                       |                               | A1                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | A2                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | G                  | GPIO259               | GPIO                                                            | I/O       |                       |                      |                                    |                                   |                  |     |     |
| 260                   | D_ADD13_<br>GPIO260           | P                  | D_ADD13               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                               | —/Up                              | —                | —   | R2  |
|                       |                               | A1                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | A2                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | G                  | GPIO260               | GPIO                                                            | I/O       |                       |                      |                                    |                                   |                  |     |     |
| 261                   | D_ADD14_<br>GPIO261           | P                  | D_ADD14               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                               | —/Up                              | —                | —   | R3  |
|                       |                               | A1                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | A2                 | —                     | —                                                               | —         |                       |                      |                                    |                                   |                  |     |     |
|                       |                               | G                  | GPIO261               | GPIO                                                            | I/O       |                       |                      |                                    |                                   |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>        | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|---------------------------------|--------------------|-----------------------|-----------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                 |                    |                       |                                                                 |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 262                   | D_ADD15_<br>GPIO262             | P                  | D_ADD15               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | R4  |
|                       |                                 | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO262               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 263                   | D_ADD16_D_ADD_DAT16_<br>GPIO263 | P                  | D_ADD16               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | R5  |
|                       |                                 | A1                 | D_ADD_DAT16           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO263               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 264                   | D_ADD17_D_ADD_DAT17_<br>GPIO264 | P                  | D_ADD17               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T5  |
|                       |                                 | A1                 | D_ADD_DAT17           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO264               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 265                   | D_ADD18_D_ADD_DAT18_<br>GPIO265 | P                  | D_ADD18               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T2  |
|                       |                                 | A1                 | D_ADD_DAT18           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO265               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 266                   | D_ADD19_D_ADD_DAT19_<br>GPIO266 | P                  | D_ADD19               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T3  |
|                       |                                 | A1                 | D_ADD_DAT19           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO266               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 267                   | D_ADD20_D_ADD_DAT20_<br>GPIO267 | P                  | D_ADD20               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | T4  |
|                       |                                 | A1                 | D_ADD_DAT20           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                 | G                  | GPIO267               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>        | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |      |
|-----------------------|---------------------------------|--------------------|-----------------------|-----------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|------|
|                       |                                 |                    |                       |                                                                 |           |                       |                      |                                 |                                | 324              | 416 | 516  |
| 268                   | D_ADD21_D_ADD_DAT21_<br>GPIO268 | P                  | D_ADD21               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AB11 |
|                       |                                 | A1                 | D_ADD_DAT21           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | G                  | GPIO268               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |      |
| 269                   | D_ADD22_D_ADD_DAT22_<br>GPIO269 | P                  | D_ADD22               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AD10 |
|                       |                                 | A1                 | D_ADD_DAT22           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | G                  | GPIO269               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |      |
| 270                   | D_ADD23_D_ADD_DAT23_<br>GPIO270 | P                  | D_ADD23               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AE10 |
|                       |                                 | A1                 | D_ADD_DAT23           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | G                  | GPIO270               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |      |
| 271                   | D_ADD24_D_ADD_DAT24_<br>GPIO271 | P                  | D_ADD24               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AF10 |
|                       |                                 | A1                 | D_ADD_DAT24           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | G                  | GPIO271               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |      |
| 272                   | D_ADD25_D_ADD_DAT25_<br>GPIO272 | P                  | D_ADD25               | EBI address bus                                                 | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AD11 |
|                       |                                 | A1                 | D_ADD_DAT25           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                                 | G                  | GPIO272               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |      |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>    | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                             | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |      |
|-----------------------|-----------------------------|--------------------|-----------------------|--------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|------|
|                       |                             |                    |                       |                                                              |           |                       |                      |                                 |                                | 324              | 416 | 516  |
| 273                   | D_ADD26_D_ADD_DAT26_GPIO273 | P                  | D_ADD26               | EBI address bus                                              | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AE11 |
|                       |                             | A1                 | D_ADD_DAT26           | EBI data only in non-mux mode. Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                             | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                             | G                  | GPIO273               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |      |
| 274                   | D_ADD27_D_ADD_DAT27_GPIO274 | P                  | D_ADD27               | EBI address bus                                              | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AF11 |
|                       |                             | A1                 | D_ADD_DAT27           | EBI data only in non-mux mode. Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                             | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                             | G                  | GPIO274               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |      |
| 275                   | D_ADD28_D_ADD_DAT28_GPIO275 | P                  | D_ADD28               | EBI address bus                                              | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AD12 |
|                       |                             | A1                 | D_ADD_DAT28           | EBI data only in non-mux mode. Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                             | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                             | G                  | GPIO275               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |      |
| 276                   | D_ADD29_D_ADD_DAT29_GPIO276 | P                  | D_ADD29               | EBI address bus                                              | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AB12 |
|                       |                             | A1                 | D_ADD_DAT29           | EBI data only in non-mux mode. Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                             | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                             | G                  | GPIO276               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |      |
| 277                   | D_ADD30_D_ADD_DAT30_GPIO277 | P                  | D_ADD30               | EBI address bus                                              | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AE12 |
|                       |                             | A1                 | D_ADD_DAT30           | EBI data only in non-mux mode. Address and data in mux mode. | I/O       |                       |                      |                                 |                                |                  |     |      |
|                       |                             | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                             | G                  | GPIO277               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |      |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-----------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                                                 |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 278                   | D_ADD_DAT0_<br>GPIO278   | P                  | D_ADD_DAT0            | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | P25 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO278               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 279                   | D_ADD_DAT1_<br>GPIO279   | P                  | D_ADD_DAT1            | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | P26 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO279               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 280                   | D_ADD_DAT2_<br>GPIO280   | P                  | D_ADD_DAT2            | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | N24 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO280               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 281                   | D_ADD_DAT3_<br>GPIO281   | P                  | D_ADD_DAT3            | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | N25 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO281               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 282                   | D_ADD_DAT4_<br>GPIO282   | P                  | D_ADD_DAT4            | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | N26 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO282               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                             | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|--------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                                              |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 283                   | D_ADD_DAT5_ GPIO283      | P                  | D_ADD_DAT5            | EBI data only in non-mux mode. Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | M25 |
|                       |                          | A1                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO283               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 284                   | D_ADD_DAT6_ GPIO284      | P                  | D_ADD_DAT6            | EBI data only in non-mux mode. Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | N22 |
|                       |                          | A1                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO284               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 285                   | D_ADD_DAT7_ GPIO285      | P                  | D_ADD_DAT7            | EBI data only in non-mux mode. Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | M24 |
|                       |                          | A1                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO285               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 286                   | D_ADD_DAT8_ GPIO286      | P                  | D_ADD_DAT8            | EBI data only in non-mux mode. Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | M23 |
|                       |                          | A1                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO286               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |     |
| 287                   | D_ADD_DAT9_ GPIO287      | P                  | D_ADD_DAT9            | EBI data only in non-mux mode. Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | M22 |
|                       |                          | A1                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                            | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO287               | GPIO                                                         | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-----------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                                                 |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 288                   | D_ADD_DAT10_<br>GPIO288  | P                  | D_ADD_DAT10           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | L26 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO288               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 289                   | D_ADD_DAT11_<br>GPIO289  | P                  | D_ADD_DAT11           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | L25 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO289               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 290                   | D_ADD_DAT12_<br>GPIO290  | P                  | D_ADD_DAT12           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | L24 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO290               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 291                   | D_ADD_DAT13_<br>GPIO291  | P                  | D_ADD_DAT13           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | L23 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO291               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 292                   | D_ADD_DAT14_GPIO292      | P                  | D_ADD_DAT14           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | L22 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO292               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|-----------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                                                                 |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 293                   | D_ADD_DAT15_GPIO293      | P                  | D_ADD_DAT15           | EBI data only in non-mux mode.<br>Address and data in mux mode. | I/O       | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | K26 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO293               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 294                   | D_RD_WR_GPIO294          | P                  | D_RD_WR               | EBI read/write                                                  | O         | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | R26 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO294               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 295                   | D_WE0_GPIO295            | P                  | D_WE0                 | EBI write enable                                                | O         | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | N1  |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO295               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 296                   | D_WE1_GPIO296            | P                  | D_WE1                 | EBI write enable                                                | O         | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | P5  |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO296               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 297                   | D_OE_GPIO297             | P                  | D_OE                  | EBI output enable                                               | O         | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | P23 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO297               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |
| 298                   | D_TS_GPIO298             | P                  | D_TS                  | EBI transfer start                                              | O         | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AE9 |
|                       |                          | A1                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                                                               | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO298               | GPIO                                                            | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary           | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |      |
|-----------------------|--------------------------|--------------------|-----------------------|----------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|------|
|                       |                          |                    |                       |                            |           |                       |                      |                                 |                                | 324              | 416 | 516  |
| 299                   | D_ALE_GPIO299            | P                  | D_ALE                 | EBI Address Latch Enable   | O         | F                     | V <sub>DDE10</sub>   | —/Up                            | —/Up                           | —                | —   | P24  |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO299               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |      |
| 300                   | D_TA_GPIO300             | P                  | D_TA                  | EBI transfer acknowledge   | I/O       | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AF9  |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO300               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |      |
| 301                   | D_CS1_GPIO301            | P                  | D_CS1                 | EBI chip select            | O         | F                     | V <sub>DDE9</sub>    | —/Up                            | —/Up                           | —                | —   | AB10 |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO301               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |      |
| 302                   | D_BDIP_GPIO302           | P                  | D_BDIP                | EBI burst data in progress | O         | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | M2   |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO302               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |      |
| 303                   | D_WE2_GPIO303            | P                  | D_WE2                 | EBI write enable           | O         | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | N2   |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO303               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |      |
| 304                   | D_WE3_GPIO304            | P                  | D_WE3                 | EBI write enable           | O         | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | N3   |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |      |
|                       |                          | G                  | GPIO304               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |      |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary           | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------|--------------------|-----------------------|----------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                          |                    |                       |                            |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 305                   | D_ADD9_GPIO305           | P                  | D_ADD9                | EBI address bus            | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | P1  |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO305               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 306                   | D_ADD10_GPIO306          | P                  | D_ADD10               | EBI address bus            | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | P2  |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO306               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 307                   | D_ADD11_GPIO307          | P                  | D_ADD11               | EBI address bus            | I/O       | F                     | V <sub>DDE8</sub>    | —/Up                            | —/Up                           | —                | —   | P3  |
|                       |                          | A1                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO307               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| Reset and Clocks      |                          |                    |                       |                            |           |                       |                      |                                 |                                |                  |     |     |
| —                     | RESET                    | P                  | RESET                 | External reset input       | I         | MH                    | V <sub>DDEH1</sub>   | RESET/Up                        | RESET/Up                       | M2               | R2  | N5  |
| 230                   | RSTOUT                   | P                  | RSTOUT                | External reset output      | O         | MH                    | V <sub>DDEH1</sub>   | RSTOUT/Low                      | RSTOUT/High                    | A3               | A3  | A3  |
| 211                   | BOOTCFG0_IRQ2_GPIO211    | P                  | BOOTCFG0              | Boot configuration         | I         | MH                    | V <sub>DDEH1</sub>   | BOOTCFG/Down                    | BOOTCFG/Down                   | —                | —   | L4  |
|                       |                          | A1                 | IRQ2                  |                            | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO211               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |
| 212                   | BOOTCFG1_IRQ3_GPIO212    | P                  | BOOTCFG1              | Boot configuration         | I         | MH                    | V <sub>DDEH1</sub>   | BOOTCFG/Down                    | Input/Down                     | L1               | N2  | L3  |
|                       |                          | A1                 | IRQ3                  | External interrupt request | I         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | A2                 | —                     | —                          | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                          | G                  | GPIO212               | GPIO                       | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup>                                       | Signal Name <sup>2</sup>                                                       | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                                                      | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup>                | Package Location |      |      |
|-------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------|-----------------------|-------------------------------------------------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|-----------------------------------------------|------------------|------|------|
|                                                             |                                                                                |                    |                       |                                                                                                       |           |                       |                      |                                 |                                               | 324              | 416  | 516  |
| 213                                                         | WKPCFG_NMI_<br>GPIO213                                                         | P                  | WKPCFG                | Weak pull configuration input                                                                         | I         | MH                    | V <sub>DDEH1</sub>   | WKPCFG/Up                       | Input/Up                                      | —                | N3   | M5   |
|                                                             |                                                                                | A1                 | NMI                   | Critical interrupt to core <sup>11</sup>                                                              | I         |                       |                      |                                 |                                               |                  |      |      |
|                                                             |                                                                                | A2                 | —                     | —                                                                                                     | —         |                       |                      |                                 |                                               |                  |      |      |
|                                                             |                                                                                | G                  | GPIO213               | GPIO                                                                                                  | I         |                       |                      |                                 |                                               |                  |      |      |
| 208                                                         | PLLCFG0_IRQ4_<br>GPIO208                                                       | P                  | PLLCFG0               | FMPLL mode configuration input                                                                        | I         | MH                    | V <sub>DDEH1</sub>   | PLLCFG/Up                       | Input/Up                                      | M3               | R3   | M3   |
|                                                             |                                                                                | A1                 | IRQ4                  | External interrupt request                                                                            | I         |                       |                      |                                 |                                               |                  |      |      |
|                                                             |                                                                                | A2                 | —                     | —                                                                                                     | —         |                       |                      |                                 |                                               |                  |      |      |
|                                                             |                                                                                | G                  | GPIO208               | GPIO                                                                                                  | I/O       |                       |                      |                                 |                                               |                  |      |      |
| 209                                                         | PLLCFG1_IRQ5_<br>GPIO209                                                       | P                  | PLLCFG1               | FMPLL mode configuration input                                                                        | I         | MH                    | V <sub>DDEH1</sub>   | PLLCFG/Up                       | Input/Up<br>(for Rev2 of the<br>device: —/Up) | L2               | P2   | L1   |
|                                                             |                                                                                | A1                 | IRQ5                  | External interrupt request                                                                            | I         |                       |                      |                                 |                                               |                  |      |      |
|                                                             |                                                                                | A2                 | SOUTD                 | DSPI D data output                                                                                    | O         |                       |                      |                                 |                                               |                  |      |      |
|                                                             |                                                                                | G                  | GPIO209               | GPIO                                                                                                  | I/O       |                       |                      |                                 |                                               |                  |      |      |
| —                                                           | PLLCFG2                                                                        | P                  | PLLCFG2               | FMPLL mode configuration input                                                                        | I         | MH                    | V <sub>DDEH1</sub>   | PLLCFG/<br>Down                 | PLLCFG/<br>Down                               | L3               | P3   | L2   |
| —                                                           | XTAL                                                                           | P                  | XTAL                  | Crystal oscillator output                                                                             | O         | AE                    | V <sub>DD33</sub>    | XTAL                            | XTAL                                          | W22              | AC26 | AC26 |
| —                                                           | EXTAL                                                                          | P                  | EXTAL                 | Crystal oscillator input                                                                              | I         | AE                    | V <sub>DD33</sub>    | EXTAL                           | EXTAL                                         | V22              | AB26 | AB26 |
| 229                                                         | D_CLKOUT                                                                       | P                  | D_CLKOUT              | EBI system clock output                                                                               | O         | F                     | V <sub>DDE9</sub>    | CLKOUT/<br>Enabled              | CLKOUT/<br>Enabled                            | —                | —    | AF12 |
| 214                                                         | ENGCLK                                                                         | P                  | ENGCLK                | EBI engineering clock output<br>Note: EXTCLK (External clock input)<br>selected through SIU register) | O         | F                     | V <sub>DDE2</sub>    | ENGCLK/<br>Enabled              | ENGCLK/<br>Enabled                            | AA1              | AD1  | AD1  |
| JTAG and Nexus<br>(see footnote <sup>12</sup> about resets) |                                                                                |                    |                       |                                                                                                       |           |                       |                      |                                 |                                               |                  |      |      |
| —                                                           | EVTI                                                                           | <sub>13</sub>      | EVTI                  | Nexus event in                                                                                        | I         | F                     | V <sub>DDE2</sub>    | —/Up                            | EVTI/Up                                       | N4               | T4   | V1   |
| 227                                                         | EVTO<br>(the BAM uses this pin to<br>select if auto baud rate is on or<br>off) | <sub>13</sub>      | EVTO                  | Nexus event out                                                                                       | O         | F                     | V <sub>DDE2</sub>    | ABS/Up                          | EVTO/Hi                                       | P1               | U1   | V2   |
| 219                                                         | MCKO                                                                           | <sub>13</sub>      | MCKO                  | Nexus message clock out                                                                               | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | Disabled <sup>14</sup>                        | N2               | T2   | U4   |

**Table 43. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>                                                             | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary       | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------------------------------------------------------------------|--------------------|-----------------------|------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                                                                      |                    |                       |                        |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 220                   | MDO0_GPIO220<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO0 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | MDO0/Low                       | P3               | U3  | V3  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO220               | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 221                   | MDO1_GPIO221<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO1 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | P4               | U4  | W6  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO221               | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 222                   | MDO2_GPIO222<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO2 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | R1               | V1  | V4  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO222               | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 223                   | MDO3_GPIO223<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO3 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | R2               | V2  | V5  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO223               | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 75                    | MDO4_GPIO75<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO4 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | R3               | V3  | W1  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO75                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 76                    | MDO5_GPIO76<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO5 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | R4               | V4  | W2  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO76                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup>                                                             | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary       | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |     |     |
|-----------------------|--------------------------------------------------------------------------------------|--------------------|-----------------------|------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|-----|-----|
|                       |                                                                                      |                    |                       |                        |           |                       |                      |                                 |                                | 324              | 416 | 516 |
| 77                    | MDO6_GPIO77<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO6 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | T1               | W1  | W3  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO77                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 78                    | MDO7_GPIO78<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO7 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | T2               | W2  | Y1  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO78                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 79                    | MDO8_GPIO79<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO8 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | T3               | W3  | W5  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO79                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 80                    | MDO9_GPIO80<br>(GPIO function on this pin is only available on Rev.2 of the device)  | _13                | MDO9 <sup>15</sup>    | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | U1               | Y1  | Y2  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO80                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 81                    | MDO10_GPIO81<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO10 <sup>15</sup>   | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | U2               | Y2  | Y3  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO81                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |
| 82                    | MDO11_GPIO82<br>(GPIO function on this pin is only available on Rev.2 of the device) | _13                | MDO11 <sup>15</sup>   | Nexus message data out | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | U3               | Y3  | Y4  |
|                       |                                                                                      | A1                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | A2                 | —                     | —                      | —         |                       |                      |                                 |                                |                  |     |     |
|                       |                                                                                      | G                  | GPIO82                | GPIO                   | I/O       |                       |                      |                                 |                                |                  |     |     |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                        | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|-----------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                                         |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| 231                   | MDO12_GPIO231            | _13                | MDO12 <sup>15</sup>   | Nexus message data out                  | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | V1               | AA1  | Y5   |
|                       |                          | A1                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO231               | GPIO                                    | I/O       |                       |                      |                                 |                                |                  |      |      |
| 232                   | MDO13_GPIO232            | _13                | MDO13 <sup>15</sup>   | Nexus message data out                  | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | W2               | AA2  | AA1  |
|                       |                          | A1                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO232               | GPIO                                    | I/O       |                       |                      |                                 |                                |                  |      |      |
| 233                   | MDO14_GPIO233            | _13                | MDO14 <sup>15</sup>   | Nexus message data out                  | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | V3               | AA3  | AA2  |
|                       |                          | A1                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO233               | GPIO                                    | I/O       |                       |                      |                                 |                                |                  |      |      |
| 234                   | MDO15_GPIO234            | _13                | MDO15 <sup>15</sup>   | Nexus message data out                  | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | —/Down                         | U4               | Y4   | AA3  |
|                       |                          | A1                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | A2                 | —                     | —                                       | —         |                       |                      |                                 |                                |                  |      |      |
|                       |                          | G                  | GPIO234               | GPIO                                    | I/O       |                       |                      |                                 |                                |                  |      |      |
| 224                   | MSEO0                    | _13                | MSEO0 <sup>15</sup>   | Nexus message start/end out             | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | MSEO/HI                        | P2               | U2   | U6   |
| 225                   | MSEO1                    | _13                | MSEO1 <sup>15</sup>   | Nexus message start/end out             | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | MSEO/HI                        | N3               | T3   | U5   |
| 226                   | RDY                      | _13                | RDY                   | Nexus ready output                      | O         | F                     | V <sub>DDE2</sub>    | O/Low                           | RDY/HI                         | M4               | R4   | U3   |
| —                     | TCK                      | _13                | TCK                   | JTAG test clock input                   | I         | F                     | V <sub>DDE2</sub>    | TCK/Down                        | TCK/Down                       | Y1               | AB2  | AB2  |
| —                     | TDI                      | _13                | TDI                   | JTAG test data input                    | I         | F                     | V <sub>DDE2</sub>    | TDI/Up                          | TDI/Up                         | Y2               | AC2  | AC2  |
| 228                   | TDO                      | _13                | TDO                   | JTAG test data output                   | O         | F                     | V <sub>DDE2</sub>    | TDO/Up                          | TDO/Up                         | W1               | AB1  | AB1  |
| —                     | TMS                      | _13                | TMS                   | JTAG test mode select input             | I         | F                     | V <sub>DDE2</sub>    | TMS/Up                          | TMS/Up                         | W3               | AB3  | AB3  |
| —                     | JCOMP                    | _13                | JCOMP                 | JTAG TAP controller enable              | I         | F                     | V <sub>DDE2</sub>    | JCOMP/Down                      | JCOMP/Down                     | M1               | R1   | U2   |
| —                     | TEST                     | —                  | TEST                  | Test mode select (not for customer use) | I         | F                     | V <sub>DDEH1</sub>   | TEST/Down                       | TEST/Down                      | B4               | B4   | B4   |
| —                     | VDDSYN                   | —                  | VDDSYN                | Clock synthesizer power input           | I         | VDDE                  | V <sub>DDSYN</sub>   | VDDSYN                          | VDDSYN                         | Y22              | AD26 | AD26 |

Table 43. Signal Properties and Muxing Summary (continued)

| GPIO/PCR <sup>1</sup> | Signal Name <sup>2</sup> | P/A/G <sup>3</sup> | Function <sup>4</sup> | Function Summary                                                      | Direction | Pad Type <sup>5</sup> | Voltage <sup>6</sup> | State during RESET <sup>7</sup> | State after RESET <sup>8</sup> | Package Location |      |      |
|-----------------------|--------------------------|--------------------|-----------------------|-----------------------------------------------------------------------|-----------|-----------------------|----------------------|---------------------------------|--------------------------------|------------------|------|------|
|                       |                          |                    |                       |                                                                       |           |                       |                      |                                 |                                | 324              | 416  | 516  |
| —                     | VSSSYN                   | —                  | VSSSYN                | Clock synthesizer ground input                                        | I         | VSSE                  | V <sub>DDSYN</sub>   | VSSSYN                          | VSSSYN                         | U22              | AA26 | AA26 |
| —                     | VSTBY                    | —                  | VSTBY                 | SRAM standby power input                                              | I         | VHV                   | V <sub>DDEH1</sub>   | VSTBY                           | VSTBY                          | K4               | M4   | M4   |
| —                     | REGSEL                   | —                  | REGSEL                | Selects regulator mode (Linear/Switch mode)                           | I         | AE                    | V <sub>DDREG</sub>   | REGSEL                          | REGSEL                         | V20              | W23  | W23  |
| —                     | REGCTL                   | —                  | REGCTL                | Regulator controller output to base/gate of power transistor          | O         | AE                    | V <sub>DDREG</sub>   | REGCTL                          | REGCTL                         | T22              | Y26  | Y26  |
| —                     | VSSFL                    | —                  | VSSFL                 | Tie to V <sub>SS</sub>                                                | I         | VSS                   | V <sub>DDREG</sub>   | VSSFL                           | VSSFL                          | V21              | AB25 | AB25 |
| —                     | VDDREG                   | —                  | VDDREG                | Source voltage for on-chip regulators and Low voltage detect circuits | I         | VDDINT                | V <sub>DDREG</sub>   | VDDREG                          | VDDREG                         | U21              | AA25 | AA25 |

<sup>1</sup> The GPIO number is the same as the corresponding pad configuration register (SIU\_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

<sup>2</sup> The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

<sup>3</sup> P/A/G stands for Primary/Alternate/GPIO. This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

<sup>4</sup> Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU\_PCRn registers except where explicitly noted.

<sup>5</sup> MH = High voltage, medium speed

F = Fast speed

FS = Fast speed with slew

AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)

VHV = Very high voltage

<sup>6</sup> VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

<sup>7</sup> The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

<sup>8</sup> The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

<sup>9</sup> This signal name includes eTPU\_C functionality that this device does not have. This is for forward compatibility with devices that have an eTPU\_C.

<sup>10</sup> During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

<sup>11</sup> NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU\_IREER and SIU\_IFEER registers.

- <sup>12</sup> Nexus reset is different than system reset; MDO 1-11 are enabled when trace (RPM or FPM) is enabled, and MDO 12-15 when FPM trace is enabled. MSEO and MCKO are also dependent on trace (RPM or FPM) being enabled.
- <sup>13</sup> The Nexus pins don't have a "primary" function as they are not configured by the SIU. The pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of these pins once enabled.
- <sup>14</sup> MCKO is disabled from reset; it can be enabled from the tool (controlled by Nexus NPC\_PCR register).
- <sup>15</sup> Do not connect pin directly to a power supply or ground.

Table 45 lists the pin locations of the power and ground signals on the 324 TEPBGA package.

Table 44. 324-pin Power Supply Locations

VDD

|    |    |    |    |    |     |    |    |     |    |     |     |      |     |
|----|----|----|----|----|-----|----|----|-----|----|-----|-----|------|-----|
| A2 | B3 | C4 | D5 | K3 | V19 | W5 | W9 | W20 | Y4 | Y21 | AA3 | AA22 | AB2 |
|----|----|----|----|----|-----|----|----|-----|----|-----|-----|------|-----|

VDD33

|     |    |
|-----|----|
| W21 | V4 |
|-----|----|

VDDE2

|     |    |    |     |    |     |    |    |    |    |
|-----|----|----|-----|----|-----|----|----|----|----|
| AB4 | M9 | N1 | N10 | N9 | P10 | P9 | T4 | W6 | V2 |
|-----|----|----|-----|----|-----|----|----|----|----|

VDDEH1

|    |    |
|----|----|
| B1 | L4 |
|----|----|

VDDEH4

|      |    |
|------|----|
| AB20 | W8 |
|------|----|

VDDEH6

|     |     |
|-----|-----|
| N20 | T21 |
|-----|-----|

VDDEH7

|     |     |     |
|-----|-----|-----|
| C22 | H19 | L22 |
|-----|-----|-----|

VSS

|     |     |     |      |     |      |     |     |     |     |     |    |     |     |     |     |     |     |
|-----|-----|-----|------|-----|------|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|
| A1  | A22 | AA2 | AA21 | AB1 | AB22 | B2  | B21 | C20 | C3  | D19 | D4 | J10 | J11 | J12 | J13 | J14 | J9  |
| K10 | K11 | K12 | K13  | K14 | K9   | L10 | L11 | L12 | L13 | L14 | L9 | M10 | M11 | M12 | M13 | M14 | N11 |
| N12 | N13 | N14 | P11  | P12 | P13  | P14 | W19 | W4  | Y20 | Y3  |    |     |     |     |     |     |     |

Table 45 lists the pin locations of the power and ground signals on the 416 TEPBGA package.

**Table 45. 416-pin Power Supply Locations**

**VDD**

|    |    |    |    |    |     |      |     |      |      |     |      |     |      |
|----|----|----|----|----|-----|------|-----|------|------|-----|------|-----|------|
| A2 | B3 | C4 | D5 | N4 | AB4 | AB23 | AC3 | AC12 | AC24 | AD2 | AD25 | AE1 | AE26 |
|----|----|----|----|----|-----|------|-----|------|------|-----|------|-----|------|

**VDD33**

|    |     |      |
|----|-----|------|
| M1 | AA4 | AA23 |
|----|-----|------|

**VDDE2**

|     |     |     |     |     |    |     |     |     |     |     |     |    |     |     |     |
|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|
| N10 | P10 | P11 | R10 | R11 | T1 | T10 | T11 | T12 | U10 | U11 | U12 | W4 | AC1 | AC5 | AF2 |
|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|

**VDDEH1**

|    |    |
|----|----|
| B1 | P4 |
|----|----|

**VDDEH3**

|      |     |
|------|-----|
| AC10 | AF5 |
|------|-----|

**VDDEH4**

|      |      |
|------|------|
| AC11 | AF22 |
|------|------|

**VDDEH5**

|      |      |
|------|------|
| AC21 | AF25 |
|------|------|

**VDDEH6**

|     |      |
|-----|------|
| N23 | AC25 |
|-----|------|

**VDDEH7**

|     |     |     |
|-----|-----|-----|
| D24 | E23 | M26 |
|-----|-----|-----|

**VSS**

|     |     |     |     |     |     |     |     |      |     |      |     |      |     |      |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|-----|-----|
| A1  | A26 | B2  | B25 | C3  | C24 | D4  | D23 | K10  | K11 | K12  | K13 | K14  | K15 | K16  | K17 | L10 | L11 |
| L12 | L13 | L14 | L15 | L16 | L17 | M10 | M11 | M12  | M13 | M14  | M15 | M16  | M17 | N11  | N12 | N13 | N14 |
| N15 | N16 | N17 | P12 | P13 | P14 | P15 | P16 | P17  | R12 | R13  | R14 | R15  | R16 | R17  | T13 | T14 | T15 |
| T16 | T17 | U13 | U14 | U15 | U16 | U17 | AC4 | AC23 | AD3 | AD24 | AE2 | AE25 | AF1 | AF26 |     |     |     |

Table 46 lists the pin locations of the power and ground signals on the 516 TEPBGA package.

**Table 46. 516-pin Power Supply Locations**

**VDD**

|    |    |    |    |    |    |     |      |     |      |      |     |      |     |      |
|----|----|----|----|----|----|-----|------|-----|------|------|-----|------|-----|------|
| A2 | B3 | C4 | D5 | E6 | N4 | AB4 | AB23 | AC3 | AC12 | AC24 | AD2 | AD25 | AE1 | AE26 |
|----|----|----|----|----|----|-----|------|-----|------|------|-----|------|-----|------|

**VDD33**

|    |    |     |     |      |      |      |
|----|----|-----|-----|------|------|------|
| M1 | P6 | L21 | AA4 | AA11 | AA14 | AA23 |
|----|----|-----|-----|------|------|------|

**VDDE10**

|     |     |     |     |     |     |      |
|-----|-----|-----|-----|-----|-----|------|
| F16 | F17 | F19 | F21 | N21 | P21 | AA22 |
|-----|-----|-----|-----|-----|-----|------|

**VDDE2**

|     |     |     |     |     |    |     |     |     |     |     |     |    |     |     |     |
|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|
| N10 | P10 | P11 | R10 | R11 | T1 | T10 | T11 | T12 | U10 | U11 | U12 | W4 | AC1 | AC5 | AF2 |
|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|

**VDDE8**

|    |    |     |     |    |     |
|----|----|-----|-----|----|-----|
| F6 | F8 | F10 | F11 | N6 | AA5 |
|----|----|-----|-----|----|-----|

**VDDE9**

|      |     |     |      |      |      |      |
|------|-----|-----|------|------|------|------|
| AA13 | AB6 | AB7 | AB18 | AB19 | AB20 | AB21 |
|------|-----|-----|------|------|------|------|

**VDDEH1**

|    |    |
|----|----|
| B1 | P4 |
|----|----|

**VDDEH3**

|      |     |
|------|-----|
| AC10 | AF5 |
|------|-----|

**VDDEH4**

|      |      |
|------|------|
| AC11 | AF22 |
|------|------|

**VDDEH5**

|      |      |
|------|------|
| AC21 | AF25 |
|------|------|

**VDDEH6**

|     |      |
|-----|------|
| N23 | AC25 |
|-----|------|

**VDDEH7**

|     |     |     |
|-----|-----|-----|
| D24 | E23 | M26 |
|-----|-----|-----|

**VSS**

|     |     |     |     |     |     |     |     |     |      |     |      |     |      |     |      |     |      |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|
| A25 | B2  | B25 | B26 | C3  | C24 | D4  | D23 | E5  | E7   | E8  | E9   | E10 | E11  | E12 | E13  | E14 | E15  |
| E16 | E17 | E18 | E19 | E21 | E22 | F5  | F13 | F14 | K10  | K11 | K12  | K13 | K14  | K15 | K16  | K17 | L10  |
| L11 | L12 | L13 | L14 | L15 | L16 | L17 | M10 | M11 | M12  | M13 | M14  | M15 | M16  | M17 | N11  | N12 | N13  |
| N14 | N15 | N16 | N17 | P12 | P13 | P14 | P15 | P16 | P17  | R12 | R13  | R14 | R15  | R16 | R17  | T13 | T14  |
| T15 | T16 | T17 | U13 | U14 | U15 | U16 | U17 | AA6 | AA21 | AB5 | AB22 | AC4 | AC23 | AD3 | AD24 | AE2 | AE25 |

# Appendix B Revision History

Table 47 describes the changes made to this document between revisions.

**Table 47. Revision History**

| Revision<br>(Date) | Description of changes                                                                                                                                                                                                                                                                                                              |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2<br>(Sept 2008)   | Initial release, NDA Required.                                                                                                                                                                                                                                                                                                      |
| 3<br>(Nov 2009)    | <b>Changes between Rev.2 and Rev. 3:</b>                                                                                                                                                                                                                                                                                            |
|                    | Added 516-pin package figures.                                                                                                                                                                                                                                                                                                      |
|                    | Signals table: Updates throughout entire table.                                                                                                                                                                                                                                                                                     |
|                    | Updated <a href="#">Section 4.6, "Power Up/Down Sequencing"</a>                                                                                                                                                                                                                                                                     |
|                    | Updated features list.<br>Updated flash PFCPR1 settings table.<br>Fixed JTAG Test Clock Input Timing figure so the spec #'s in table matched figure.                                                                                                                                                                                |
|                    | Updated Orderable Part numbers table.                                                                                                                                                                                                                                                                                               |
|                    | Moved signals table to be an appendix.                                                                                                                                                                                                                                                                                              |
|                    | Added 324-pin package thermals.<br>Updated part numbers in orderable parts table (missing F: MPC5674F).                                                                                                                                                                                                                             |
|                    | FMPLL Electrical Spec table:<br>Spec #1 changed min values of 4 to 8<br>Removed last sentence of footnote 2<br>Added note "Upper tolerance of less than 1% is allowed on 40MHz crystal."                                                                                                                                            |
|                    | Oscillator Electrical Spec table:<br>Moved predivider op. frequency spec from this table to the FMPLL Electrical Spec table<br>Removed footnote #3 (since VDDE9 is an external supply and has no relation to the oscillator, PMC, or PLL).                                                                                          |
|                    | Added maximum solder temperature to Absolute Max Ratings table.                                                                                                                                                                                                                                                                     |
|                    | PMC Operating Conditions table:<br>Removed JTemp row.<br>Changed VDDR to VDDREG (naming consistency)<br>Changed VDD12 to VDD (naming consistency)                                                                                                                                                                                   |
|                    | PMC Electrical Spec table:<br>Added VDDREG to this parameter "Trimmed bandgap reference voltage / voltage dependence ( $V_{DDREG}$ )"<br>Changed VDDSTEP to LVDSTEP12 (naming consistency)                                                                                                                                          |
|                    | Added two conditons to the opening statements of <a href="#">Section 4.6, "Power Up/Down Sequencing."</a>                                                                                                                                                                                                                           |
|                    | DC Electrical Specifications table:<br>spec #9 (Fast I/O Input High Voltage)<br>spec #10 (Fast I/O Input Low Voltage)<br>spec #24 (Operating Current 1.2 V Supplies; IDD)<br>spec #25 (Operating Current 3.3 V Supplies; IDDSYN)<br>spec #32 (Analog Input Current, Channel Off; IINACT_A)<br>footnote #12 ("IOH_S = {11.6} mA...") |

Table 47. Revision History (continued)

| Revision<br>(Date) | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3<br>(cont.)       | eQADC Conversion Specifications table:<br>Spec #7, 8: both +/-3, no dependency on frequency<br>Spec #15, 16: added "(with calibration)" to both                                                                                                                                                                                                                                                                                                                                                                                                             |
|                    | Flash Program and Erase Specifications table:<br>Added footnote 4 to spec #2.<br>Updated all initial max value times.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                    | Updated entire AC Specifications: Clocking section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                    | Pad AC Specifications table: updated Medium pad specs<br>Derated Pad AC Specifications table: updated all specs                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                    | Updated entire <a href="#">Section 4.6, "Power Up/Down Sequencing."</a>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                    | Updated Absolute Maximum Ratings (AMR) specs 1–11, 15, 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                    | Changed name of IDDC to IREGCTL since it is the REGCTL max drive current.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|                    | Added two EMC Radiated Emissions Operating Behaviors tables and removed "EMI Testing Specifications" table.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                    | PMC Electrical Specifications table:<br>1b: Changed 1% to 2%<br>1c: Changed 150 to 300 ppm/C<br>2b: added footnote<br>2c: Changed from "Trimming step VDD" to "Trimming step VDD12OUT"                                                                                                                                                                                                                                                                                                                                                                      |
|                    | DC Electrical Specifications table:<br>6: Updated min value and added keep-out range                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|                    | Standby RAM Regulator Electrical Specifications table:<br>Added brownout spec                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                    | PMC electrical spec table, added new specs: SMPS regulator output resistance, SPMS regulator clock frequency, SMPS regulator overshoot at start-up, SMPS max output current, and voltage variation on current step.                                                                                                                                                                                                                                                                                                                                         |
|                    | Added LVD VDDA specs to the PMC electrical spec table.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                    | Removed specs for VDDF and VFLASH since those supplies are shorted with others in the package.                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4<br>(Aug 2010)    | <b>Changes between Rev.3 and Rev.4:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                    | Table "Derated Pad AC Specifications", Spec #1: Changed 20ns to 200ns.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                    | Added "324-ball TEPBGA Pin Assignments" section and mechanical drawings.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                    | Appendix A (Signals):<br>Added "(the BAM uses this pin to select if auto baud rate is on or off)" to the EVTO pin description.<br>Added 324 pinout column.<br>Changed footnote from "NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU DIRER register." to "NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers."<br>Updated eQADC signals to show that eQADC A and B each have dedicated channels (ANx0-23) and shared channels (AN24-39). |

Table 47. Revision History (continued)

| Revision<br>(Date) | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4<br>(cont)        | "Temperature Sensor Electrical Specifications" table: Changed spec #2 to have one temperature range (-40 - 150 C) and changed spec value from $\pm 1.0$ to $\pm 10.0$ C.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|                    | "eQADC Conversion Specifications (Operating)" table: Changed spec #13 (non-disruptive injection current) values from $\pm 1$ to $\pm 3$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                    | "IPCLKDIV Settings" table, removed footnote "eMIOS and DMA are not considered peripherals here."                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5<br>(Feb-2011)    | <p>Note 4 in Maximum Ratings updated from 2.0 V to 1.65 V.</p> <p>Changed I/O Supply Voltage spec in DC Electrical specs, Spec 2, from 1.62 V min to 3.0 V min.</p> <p>Changed the APC=RWSC value in line 1 of PFCPR1 Settings vs. Frequency of Operation table from 0b011 to 0b100</p> <p>Changed note 1 for Pad AC Specifications table from Vdde = 1.62 V to 1.98 V to read Vdde = 3.0 V to 3.6 V</p> <p>Changed note 6 for Signal Properties and Muxing Summary table by removing the voltage range 1.8 V - 3.3 V to have 3.3 V instead of the range.</p> <p>Spec 2 in Table 9 "ESD Ratings" the spec for "ESD for Charged Device Model (CDM)" changed to 250 V (other) from 500 V (other)</p> <p>Removed voltage ranges 1.62-1.98 V and 2.25-2.75 V from spec 28 in Table 14</p> |
| 6<br>(Feb-2011)    | Same content as for Rev. 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 7<br>(Mar-2011)    | Added entry for Rev. 6 and Rev. 7 to this table to fix a revision-numbering issue.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 8<br>(Jun-2011)    | <p>Added the following footnotes to the "Signal Properties and Muxing Summary" table:</p> <ul style="list-style-type: none"> <li>Footnote 10, for the ANA[0:7] signals, "During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device."</li> <li>Footnote 15, for MDO[0:15] and MSEO[0:1] signals, "Do not connect pin directly to a power supply or ground."</li> </ul>                                                                                                                                                                                                                                                              |
|                    | <p>Changed min and max values of ID 1 "Nominal bandgap reference voltage" in Table 11 (PMC Electrical Specifications) to 0.608 V min and 0.632 V max.</p> <p>Changed min and max values of Spec 2 "ADC Bandgap" in Table 23 (ADC Band Gap Reference/LVI Electrical Specifications) to 1.171 V min and 1.269 V max.</p> <p>Changed Spec 3 of Table 26 (Flash EEPROM Module Life) from 'Minimum Data Retention at 25 °C ambient temperature' to 'Minimum Data Retention at 85 °C ambient temperature'</p>                                                                                                                                                                                                                                                                               |
|                    | <p>Added Spec 41, 42, 43 and 44 to the "DC Electrical Specifications" table</p> <p>Added Note 25 to the "DC Electrical Specifications" table for Spec 41, 42 and 43</p> <p>Added Note 26 to the "DC Electrical Specifications" for Spec 44</p> <p>Added Spec 17 to the "eQADC Conversion Specifications (Operating)" table.</p> <p>Added Spec 18 to the "eQADC Conversion Specifications (Operating)" table.</p> <p>Added Note 15 to the "eQADC Conversion Specifications (Operating)" table for Spec 17 and 18.</p>                                                                                                                                                                                                                                                                  |
|                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

Table 47. Revision History (continued)

| Revision<br>(Date) | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8<br>(Jun-2011)    | <p>Removed spec 3 from Table 27 "PFCPR1 Settings vs Frequency of Operation"</p> <p>Updated spec 2a (Untrimmed VRC 1.2V) in Table 11 "PMC Electrical Specifications" to a max value of <math>V_{DD12OUT} + 17\%</math>.</p> <p>Updated item 26 (Operating Current VDDA Supply) in table 14 "Electrical Specifications" from 30 mA to 40 mA.</p> <p>Updated Note 11 for Table 14 (Electrical Specifications) to read <math>IOH\_F = \{16,32,47,77\}</math> mA and <math>IOL\_F = \{24,48,71,115\}</math> mA for <math>\{00,01,10,11\}</math> drive mode with <math>VDDE = 3.0</math> V.</p> <p>Updated ID 9 in Table 11 (PMC Electrical Specifications) to</p> <p><math>V_{REG} = 4.5</math> V, max DC output current with a max of 80 mA</p> <p><math>V_{REG} = 4.25</math> V, max DC output current, crank condition with a max of 40 mA</p> <p>Updated Table 17 (DSPI LVDS Pad Specification) with the following:</p> <ul style="list-style-type: none"> <li>Spec 1 typical value updated from 40 MHz to 50 MHz</li> <li>Spec 2 added SRC conditions and associated values: <ul style="list-style-type: none"> <li>SRC=0b00 or SRC=0b11 Min 150 mV Max 400 mV</li> <li>SRC=0b01 Min 90 mV Max 320 mV</li> <li>SRC=0b10 Min 160 mV Max 480 mV</li> </ul> </li> <li>Spec 3 <ul style="list-style-type: none"> <li>Min value from 1.075 V to 1.06 V</li> <li>Max value from 1.325 V to 1.39 V</li> </ul> </li> <li>Added Spec 5, 6 and 7</li> </ul> <p>Updated table 17 "DSPI LVDS pad specification" to include Temperature with a min value of -40 C and max of 150 C</p> <p>Updated Spec 5 of Table 18, "FMPLL Electrical Specifications" to &lt; 400 us as the Max vaule.</p> <p>Added the sentence "Violating the VCO min/max range may prevent the system from exiting reset." to the end of Footnote 16 of Table 18, "FMPLL Electrical Specifications"</p> <p>Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", Crystal Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz.</p> <p>Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", External Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz.</p> <p>Removed Note 9, 'Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1', from Table 18, "FMPLL Electrical Specifications".</p> <p>Updated ID 16 in Table 11, "PMC Electrical Specifications", SMPS regulator clock frequency (after reset) 2.4MHz Max</p> <p>Updated Table 16 "Flash EEPROM Module Life", spec 3, 'Blocks with 10,001–100,000 P/E cycles' to 5 Years.</p> <p>Added Typ column to Table 25, "Flash Program and Erase Specifications"</p> <p>Updated Table 3, "Absolute Maximum Ratings" with the following:</p> <ul style="list-style-type: none"> <li>Spec 1, '1.2 V Core Supply Voltage', to a Max of 2.0 V</li> <li>Spec 3, 'Clock Synthesizer Voltage', to a Max of 5.3 V</li> <li>Spec 4, 'I/O Supply Voltage' to a Max of 5.3 V</li> <li>Spec 5, 'Analog Supply Voltage' to a Max of 5.3 V</li> <li>Note 2 to read, "2.0 V for 10 hours cumulative time, 1.32 V +10% for time remaining."</li> <li>Note 3, "... 5.0 V + 10% ..." to "... 5.25 V + 10 % ..."</li> <li>Note 5, "... 3.3 V + 10% ..." to "... 3.60 V + 10 % ..."</li> </ul> <p>Updated Spec 2 (ESD for Charged Device Model (CDM)) of Table 9, "ESD Ratings", to 500 V</p> <p>Updated Table 27, "PFCPR1 Settings vs. Frequency of Operation", Spec 3, APC = RWSC column to 0b100.</p> <p>Updated Spec 26, "Operating Current 5.0 V Supplies @ <math>f_{sys} = 264</math> MHz" for <math>I_{DDA}</math> to 50 mA, in Table 14, "DC electrical specifications".</p> |

Table 47. Revision History (continued)

| Revision<br>(Date) | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9                  | <p>Updated <a href="#">Table 1, "Orderable Part Numbers"</a> with actual available parts. Added new part number SPC5673FF3MVY2 ,Package description 516 PBGA, w/EBI, Pb-free.Speed is 200 MHz nom and max.—Removed note attached to “Orderable Part Numbers” and “Freescale Part Number”.</p> <p>Updated footnotes of <a href="#">Table 3, "Absolute Maximum Ratings"</a> to:</p> <ul style="list-style-type: none"> <li>• 2.0 V for 10 hours cumulative time, 1.2V +10% for time remaining.</li> <li>• 6.4 V for 10 hours cumulative time, 5.0V +10% for time remaining.</li> <li>• 5.3 V for 10 hours cumulative time, 3.3V +10% for time remaining.</li> </ul> <p>Updated <a href="#">Table 6, "Thermal Characteristics, 324-pin Package"</a> to show MPC5674F thermal characteristics.</p> <p>In <a href="#">Table 10, "PMC Operating conditions"</a>, updated the parameter “Supply voltage VDD 1.2V nominal” to “Core supply voltage”.</p> <p>In <a href="#">Table 11, "PMC Electrical Specifications"</a>, updated the following rows:</p> <ul style="list-style-type: none"> <li>• Parameter “Nominal VRC regulated 1.2V output VDD” updated column “Typ” to 1.27 V.</li> <li>• The minimum and maximum value of “Untrimmed VRC 1.2V output variation before band gap trim (unloaded)” updated to “-14%” and “+10%”, respectively.</li> <li>• The minimum and maximum value of “Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max 1A)” updated to “-10%” and “+5%”, respectively.</li> </ul> <p>In <a href="#">Table 12, "Power Sequence Pin States for MH and AE pads"</a>, updated the row (VDD33 = low, VDDE = high), parameter “MH+LVDS Pads” to “Outputs disabled”.</p> <p>In <a href="#">Table 13, "Power Sequence Pin States for F and FS pads"</a>, updated the rows (VDD = low, VDD33 = low, VDDE = high) and (VDD = high, VDD33 = low, VDDE = high), parameter “F and FS pad” to “Outputs Disabled”.</p> <p>In <a href="#">Table 14, "DC Electrical Specifications"</a>, updated the spec 'Operating Current 1.2 V Supplies @ <math>f_{SYS} = 264</math> MHz' with 'V<sub>DD</sub> @ 1.32 V' Max value to 850 mA from 1.0 A, and deleted corresponding footnote stating that the previous information was preliminary.</p> <p>Updated current (mA) values in <a href="#">Table 15, "V<sub>DDE</sub>/V<sub>DDEH</sub> I/O Pad Average DC Current"</a> from Spec 5 to 13:</p> <ul style="list-style-type: none"> <li>• Spec 5 Current (mA) from 6.5 to 7.4</li> <li>• Spec 6 Current (mA) from 9.4 to 10.5</li> <li>• Spec 7 Current (mA) from 10.8 to 12.3</li> <li>• Spec 8 Current (mA) from 33.3 to 35.2</li> <li>• Spec 9 Current (mA) from 12.0 to 12.7</li> <li>• Spec 10 Current (mA) from 6.2 to 6.7</li> <li>• Spec 11 Current (mA) from 4.0 to 4.2</li> <li>• Spec 12 Current (mA) from 2.4 to 2.6</li> <li>• Spec 13 Current (mA) from 8.9 to 9.</li> </ul> <p>In <a href="#">Table 35, "Nexus Debug Port Timing"</a>, updated the footnote of parameter “tCYC” to “See Notes on tcyc in Table 27”. Removed references to “Section I/O Pad VDD33 Current Specifications” .</p> |
| 10                 | <p>Updated <a href="#">Figure 1, "MPC5674F Orderable Part Number Description"</a> with changes in “Revision of Silicon” and “Fab Revision ID”.</p> <p>Updated <a href="#">Table 1, "Orderable Part Numbers"</a> with changes in Part numbers and Package Description.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 10.1               | <p>In <a href="#">Figure 1, "MPC5674F Orderable Part Number Description"</a>, replaced “Revision of Silicon for TSMC is 0 for now. In future, it will be revision 1” with “0 = Rev 0 (TSMC14)”.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

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