SUD50P04-13L-GE3

Vishay Siliconix

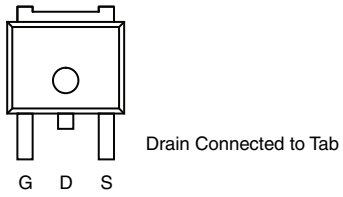
P-Channel 40 V (D-S) MOSFET

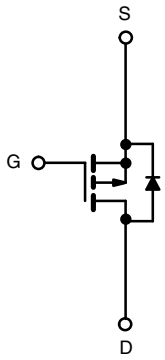
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 40	0.013 at V_{GS} = - 10 V	- 55.7[c]
	0.022 at V_{GS} = - 4.5 V	- 44.4

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE





Ordering Information: SUD50P04-13L-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current[b]	T_C = 25 °C	I_D	- 55.7[c]	
	T_C = 100 °C		- 35.2	
Pulsed Drain Current		I_{DM}	- 100	
Continuous Source Current (Diode Conduction)		I_S	- 52[c]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 40	
Avalanche Energy		E_{AS}	80	mJ
Maximum Power Dissipation[b]	T_C = 25 °C	P_D	78[b]	W
	T_A = 25 °C		3[a]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	15	18	°C/W
	Steady State		40	50	
Maximum Junction-to-Case (Drain)		R_{thJC}	1.3	1.8	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. See SOA curve for voltage derating.
c. Calculated based on maximum allowed junction temperature. Package limitation current is 50 A.

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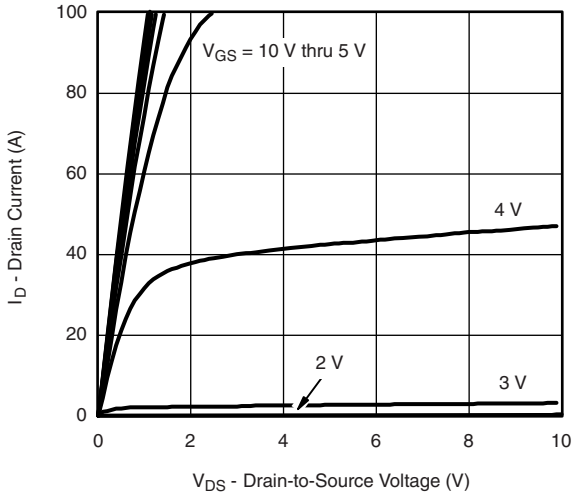
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 40			V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1.0		- 3.0	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 40 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 40 V, V_{GS} = 0 V, T_J = 125 °C			- 50	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ - 5 V, V_{GS} = - 10 V	- 50			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 30 A		0.0105	0.013	Ω
		V_{GS} = - 10 V, I_D = - 30 A, T_J = 125 °C			0.020	
		V_{GS} = - 4.5 V, I_D = - 20 A		0.017	0.022	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 30 A	15			S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 25 V, V_{GS} = 0 V, f = 1 MHz		3120		pF
Output Capacitance	C_{oss}			440		
Reverse Transfer Capacitance	C_{rss}			320		
Gate Resistance	R_g	f = 1 MHz		4.3		Ω
Total Gate Charge[c]	Q_g	V_{DS} = - 20 V, V_{GS} = - 10 V, I_D = - 50 A		63	95	nC
Gate-Source Charge[c]	Q_{gs}			13		
Gate-Drain Charge[c]	Q_{gd}			16		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 20 V, R_L = 0.4 Ω I_D ≅ - 50 A, V_{GEN} = - 10 V, R_g = 2.5 Ω		15	25	ns
Rise Time[c]	t_r			18	30	
Turn-Off Delay Time[c]	$t_{d(off)}$			60	90	
Fall Time[c]	t_f			47	70	
Drain-Source Body Diode Characteristics						
Pulse Current	I_{SM}				- 100	
Forward Voltage[a]	V_{SD}	I_F = - 50 A, V_{GS} = 0 V		- 1.0	- 1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 50 A, dI/dt = 100 A/µs		36	55	ns

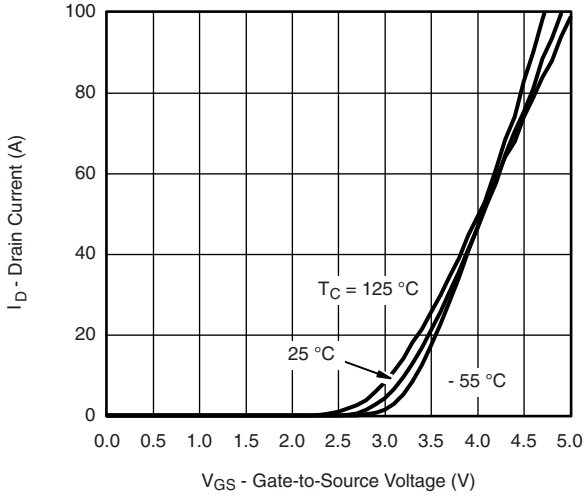
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

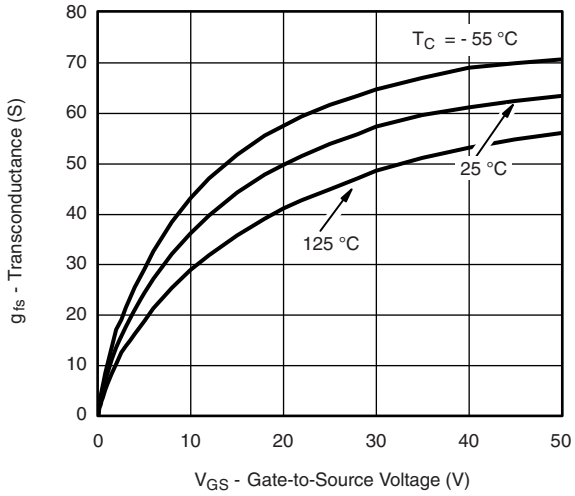
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



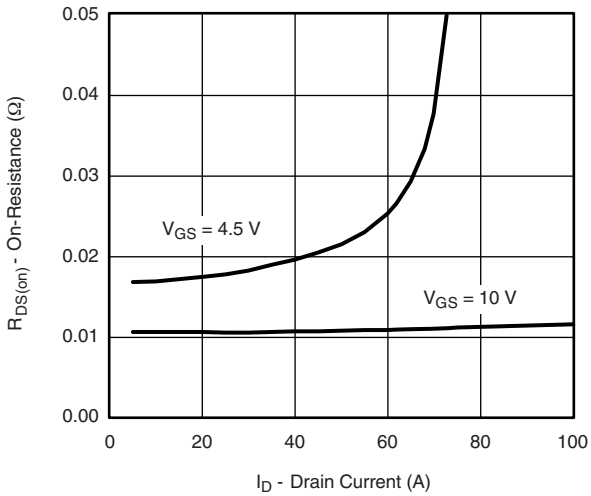
Output Characteristics



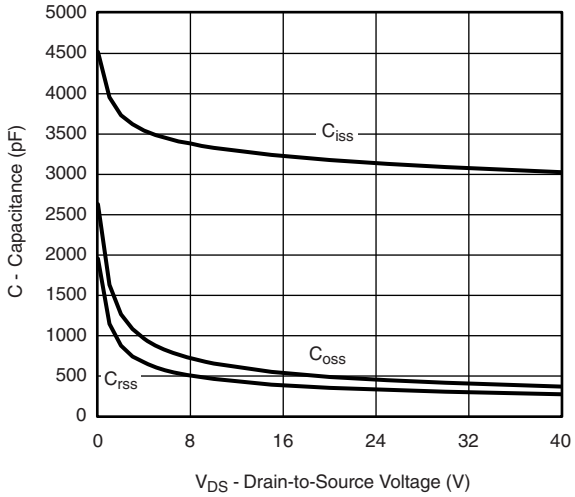
Transfer Characteristics



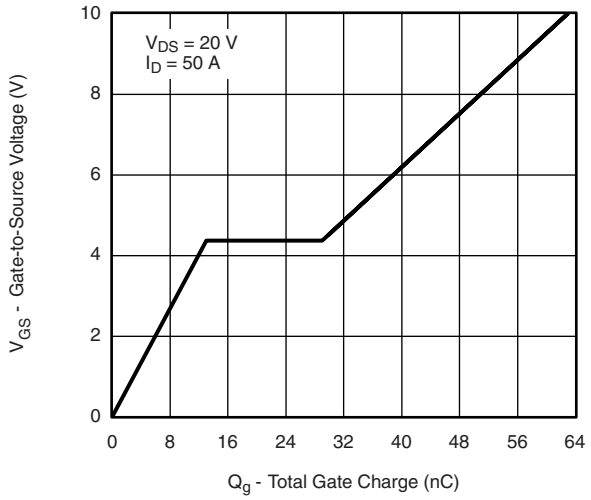
Transconductance



On-Resistance vs. Drain Current



Capacitance



Gate Charge

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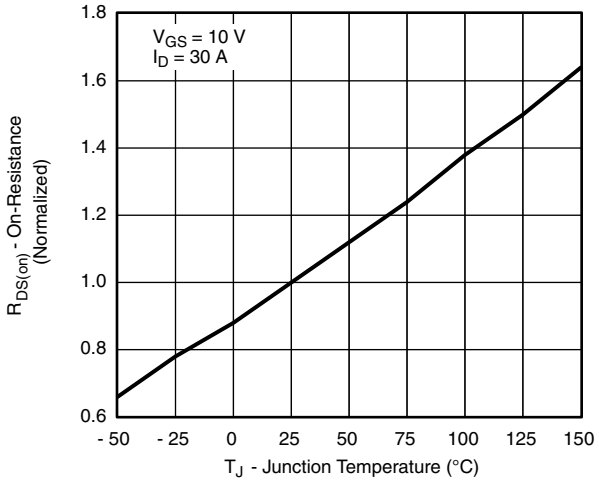
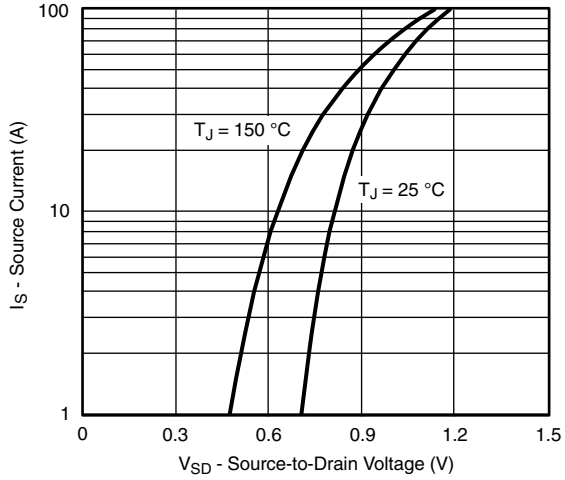
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

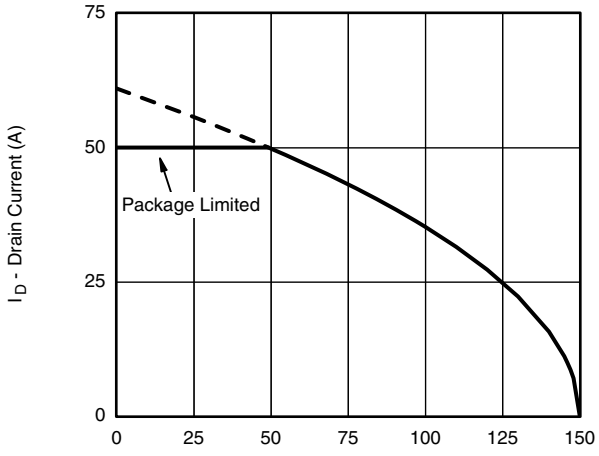


On-Resistance vs. Junction Temperature

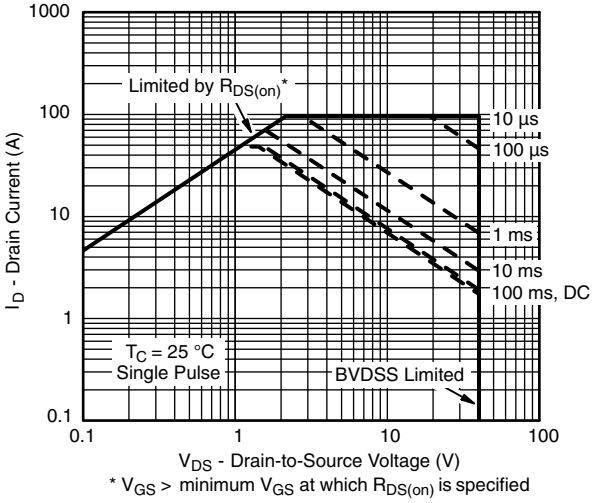


Source-Drain Diode Forward Voltage

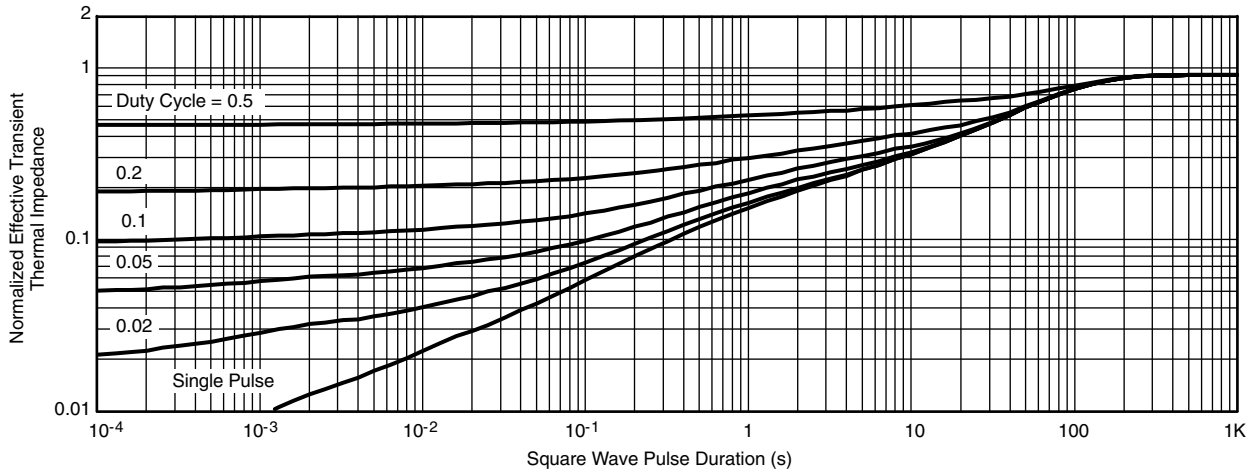
THERMAL RATINGS



Maximum Avalanche Drain Current vs. Case Temperature

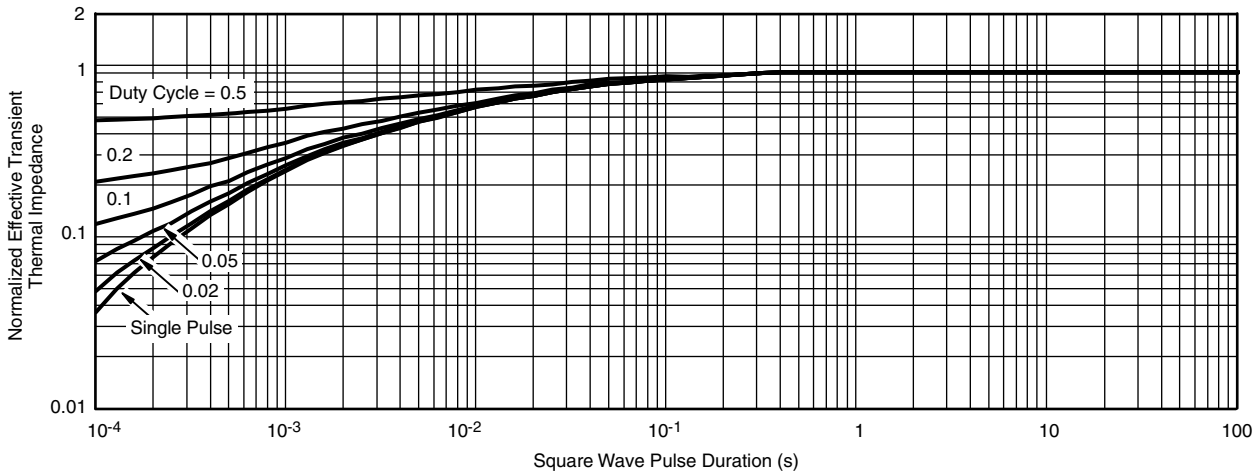


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

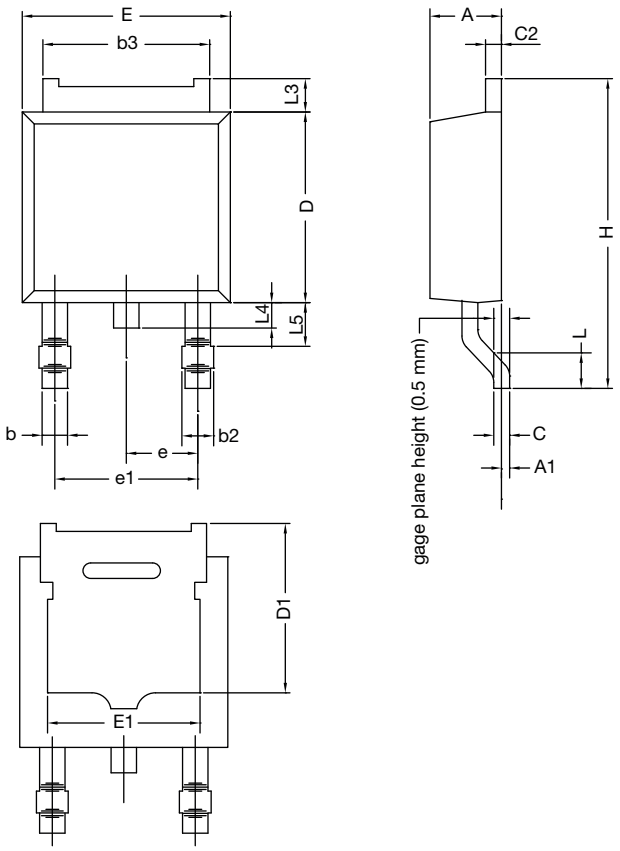
THERMAL RATINGS



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67069.

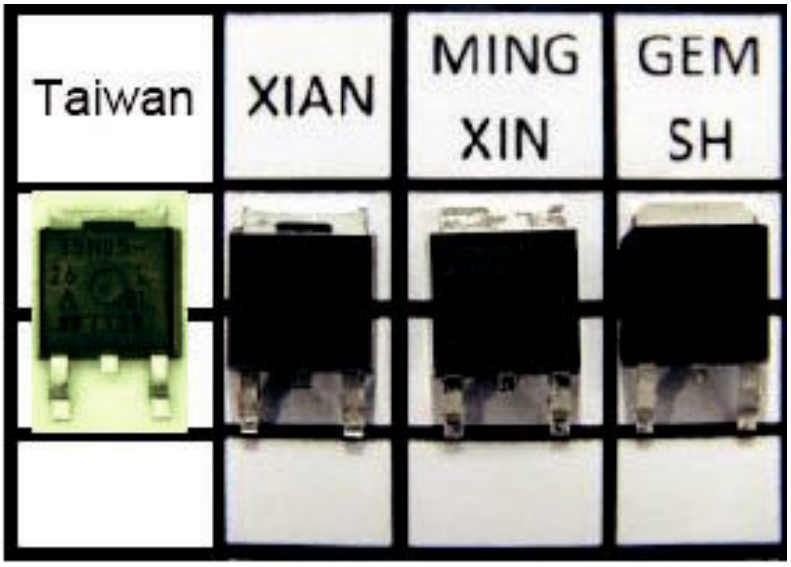
TO-252AA Case Outline



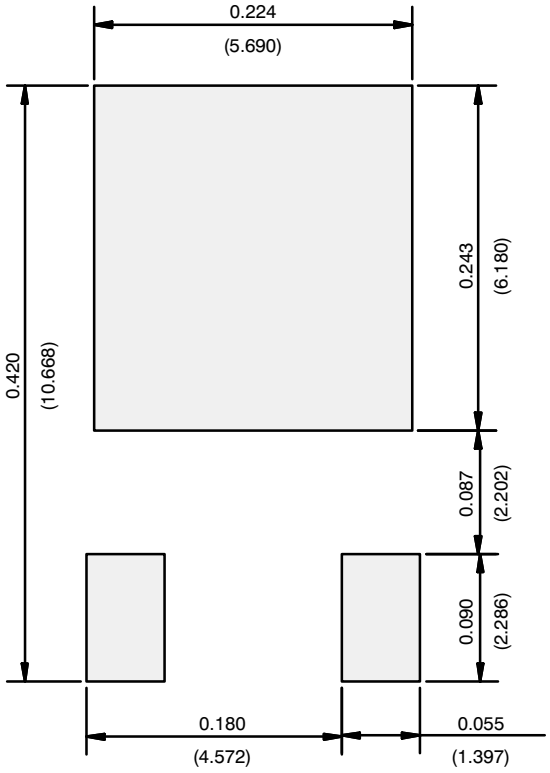
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0359-Rev. O, 03-Jun-13 DWG: 5347				

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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