DIFFERENTIAL DATA AND CLOCK D FLIP-FLOP

FEATURES

- **365ps propagation delay**
- **2.0GHz toggle frequency**
- **Internal 75KΩ input pull-down resistors**
- **Available in 8-pin SOIC package**

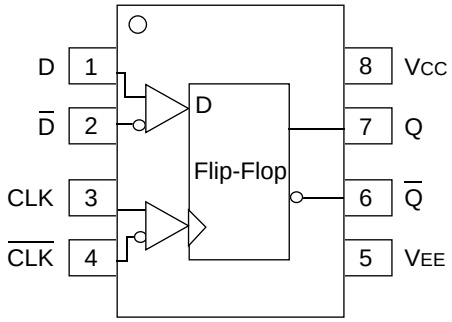
DESCRIPTION

The SY10/100EL52 are differential data, differential clock D flip-flops. These devices are functionally equivalent to the E452 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E452, the EL52 is ideally suited for those applications which require the ultimate in AC performance.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs also allow the EL52 to be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that, under open input conditions (pulled down to V_{EE}), the outputs of the device will remain stable.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D	Data Input
CLK	Clock Input
Q	Data Output

TRUTH TABLE[1]

D	CLK	Q
L	Z	L
H	Z	H

NOTE:

1. Z = LOW-to-HIGH transition.

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DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current 10EL	—	21	25	17	21	25	17	21	25	17	21	25	mA
	100EL	—	21	25	17	21	25	17	21	25	19	24	29	
V_{EE}	Power Supply Voltage 10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	1.8	2.5	—	2.2	2.8	—	2.2	2.8	—	2.2	2.8	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK	235	335	515	275	365	465	275	365	465	320	410	510	ps
t_S	Set-up Time	125	0	—	125	0	—	125	0	—	125	0	—	ps
t_H	Hold Time	150	50	—	150	50	—	150	50	—	150	50	—	ps
t_{PW}	Minimum Pulse Width	400	—	—	400	—	—	400	—	—	400	—	—	ps
V_{PP}	Minimum Input Swing[1]	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range[2]													V
	D (10EL)	–0.4	—	–1.6	–0.4	—	–1.6	–0.4	—	–1.6	–0.4	—	–1.6	
	D (100EL)	–0.4	—	–1.2	–0.4	—	–1.2	–0.4	—	–1.2	–0.4	—	–1.2	
	CLK (10EL)	–0.6	—	(3)	–0.6	—	(3)	–0.6	—	(3)	–0.6	—	(3)	
	CLK (100EL)	–0.8	—	(3)	–0.8	—	(3)	–0.8	—	(3)	–0.8	—	(3)	
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Minimum input swing for which AC parameters are guaranteed.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V.
3. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL52ZC	Z8-1	Commercial
SY10EL52ZCTR	Z8-1	Commercial
SY100EL52ZC	Z8-1	Commercial
SY100EL52ZCTR	Z8-1	Commercial

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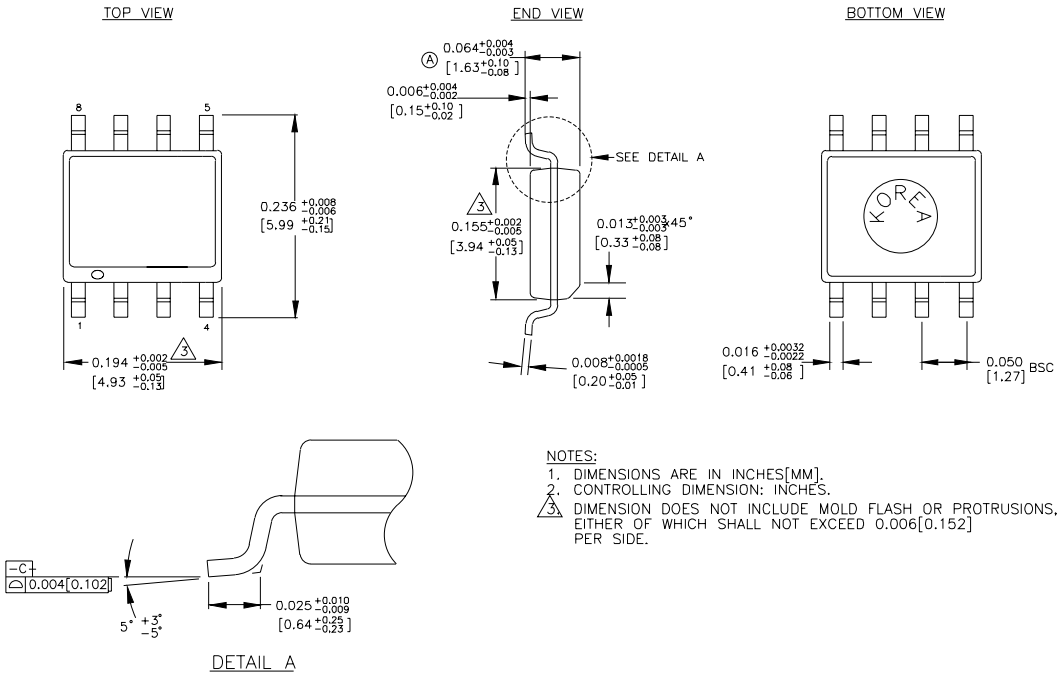
8 LEAD SOIC .150" WIDE (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

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