

TCK2292xG, TCK2297xG

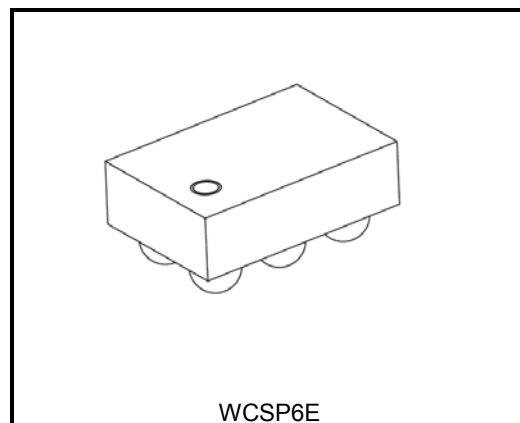
2A, 25mΩ Load Switch IC with Slew Rate Control Driver

The TCK2292xG and TCK2297xG are load switch ICs for power management with slew rate control driver featuring wide input voltage operation from 1.1 to 5.5 V. Switch ON resistance is only 25 mΩ typical at 5.0 V, -0.5 A load condition and these feature a slew rate control driver. TCK2292xG has output auto-discharge function. Output current type is available on 2 A.

This device is available in 0.4 mm pitch ultra small package WCSP6E (0.8 mm x 1.2 mm, t: 0.59 mm (max)). Thus this device is ideal for portable applications that require high-density board assembly such as cellular phone.

Feature

- Wide input voltage operation: $V_{IN} = 1.1$ to 5.5 V
- Low ON resistance:
 $R_{ON} = 25\text{ m}\Omega$ (typ.) at $V_{IN} = 5.0\text{ V}$, $I_{OUT} = -0.5\text{ A}$
 $R_{ON} = 31\text{ m}\Omega$ (typ.) at $V_{IN} = 3.3\text{ V}$, $I_{OUT} = -0.5\text{ A}$
 $R_{ON} = 52\text{ m}\Omega$ (typ.) at $V_{IN} = 1.8\text{ V}$, $I_{OUT} = -0.5\text{ A}$
 $R_{ON} = 104\text{ m}\Omega$ (typ.) at $V_{IN} = 1.2\text{ V}$, $I_{OUT} = -0.5\text{ A}$
- Low Quiescent Current: $I_Q = 0.1\text{ }\mu\text{A}$ (typ.) at $I_{OUT} = 0\text{ mA}$ (TCK22921G, TCK22971G)
- Slew Rate Control circuit
- Output auto-discharge (Option)
- Reverse current blocking
- Pull down connection between Control and GND (Option)
- Ultra small package: WCSP6E (0.8mm x 1.2mm, t: 0.59mm(max))



Weight: 1 mg (typ.)

Start of commercial production
2016-06

Function Table

Part number	Function					Device Marking
	Rise time @VIN=5V	Reverse current blocking (SW OFF state)	Output auto-discharge	Control pin polarity	Control pin connection	
TCK22921G	4.5 μ s	Built in	Built in	Active High	Pull down	1R
TCK22922G	666 μ s	Built in	Built in	Active High	Pull down	2R
TCK22923G	1364 μ s	Built in	Built in	Active High	Pull down	3R
TCK22925G	3380 μ s	Built in	Built in	Active High	Pull down	4R
TCK22971G	4.5 μ s	Built in	N/A	Active High	Pull down	5R
TCK22972G	666 μ s	Built in	N/A	Active High	Pull down	6R
TCK22973G	1364 μ s	Built in	N/A	Active High	Pull down	7R
TCK22974G	3380 μ s	Built in	N/A	Active High	Pull down	8R
TCK22975G	666 μ s	Built in	N/A	Active Low	Open	9R

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating		Unit
Input voltage	V _{IN}	-0.3 to 6.0		V
Control voltage	V _{CT}	-0.3 to 6.0		V
Output voltage	V _{OUT}	-0.3 to 6.0		V
Output current	I _{OUT}	DC	2.0	A
		Pulse	3.0 (Note1)	A
Power dissipation	P _D	800 (Note 2)		mW
Operating temperature range	T _{opr}	-40 to 85		°C
Junction teperature	T _j	150		°C
Storage temperature	T _{stg}	-55 to 150		°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: 100 μs pulse, 2% duty cycle

Note2: Rating at mounting on a board

Board material: Glass epoxy (FR4)

Board dimension: 40mm x 40mm (both sides of board), t=1.6mm

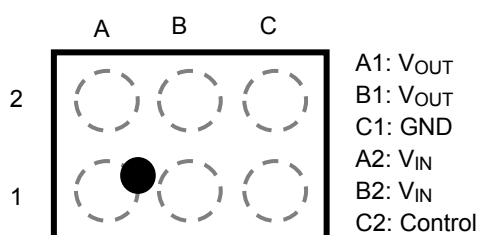
Metal pattern ratio: a surface approximately 50%, the reverse side approximately 50%

Through hole: diameter 0.5mm x 28

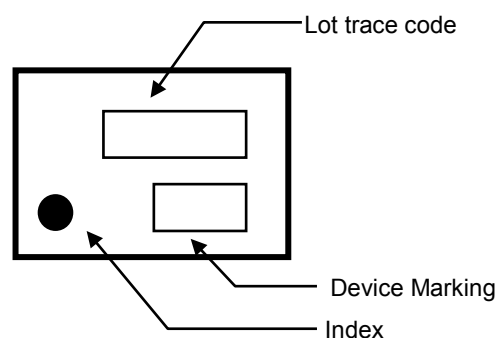
Operating conditions

Characteristics	Symbol	Condition	Min	Max	Unit
Input voltage	V _{IN}	—	1.1	5.5	V
Output voltage	V _{OUT}	—		V _{IN}	V
Output current	I _{OUT}	1.4V < V _{IN}		2.0	A
Control High-level input voltage	V _{IH}	1.2V < V _{IN} ≤ 5.5 V	1.0	—	V
		1.1V ≤ V _{IN} ≤ 1.2 V	0.9	—	
Control Low-level input voltage	V _{IL}	—	—	0.4	V

Pin Assignment(Top view)



Top marking



The diagram illustrates a CMOS inverter with an integrated slew rate control mechanism. The input signal V_{IN} is connected to the gate of the PMOS transistor Q_1 and also passes through a "Reverse Current Blocking" block. The "Control" input is connected to the gate of the NMOS transistor Q_2^* and also branches off to a "Pulldown*" block and a buffer. The buffer's output is connected to the "Control Logic" block. The "Control Logic" block receives feedback from the output V_{OUT} and provides control signals to the gates of both Q_1 and Q_2^* , as well as to the "Slew Rate Control Driver". The "Slew Rate Control Driver" is an inverter that controls the gate of Q_1 . The output of the inverter is V_{OUT} , which is also connected to the drain of Q_1 and the source of Q_2^* . A resistor is connected between V_{OUT} and the drain of Q_2^* . The "Pulldown*" block is connected to the input line and to ground (GND). A note at the bottom right states "*:Option", indicating that the pull-down transistor and resistor are optional components.

		TCK22921G TCK22922G TCK22923G TCK22925G	TCK22971G TCK22972G TCK22973G TCK22974G	TCK22975G
Control “High”	Output Q ₁	ON	ON	OFF
	Discharge Q ₂	OFF	—	—
	Reverse current blocking	Inactive	Inactive	Active
Control “Low”	Output Q ₁	OFF	OFF	ON
	Discharge Q ₂	ON	—	—
	Reverse current blocking	Active	Active	Inactive

Electrical Characteristics
DC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Quiescent current (ON state)	IQ	IOUT = 0 mA (Note 3)	VIN = 1.8 V	—	0.1	—	—	—	μA
			VIN = 3.3 V	—	0.1	—	—	—	μA
			VIN = 5.5 V	—	0.1	—	—	0.5	μA
Quiescent current (ON state)	IQ	IOUT = 0 mA	VIN = 1.8 V	—	1.2	—	—	—	μA
			VIN = 3.3 V	—	1.3	—	—	—	μA
			VIN = 5.5 V	—	1.4	—	—	2.5	μA
Quiescent current (OFF state)	IQ(OFF)	VIN = 5.5 V, VOUT = OPEN, (Note 4)		—	0.07	—	—	0.4	μA
Switch leakage current(OFF state)	ISD(OFF)	VIN = 5.5 V, VOUT = GND, current through from VIN to VOUT. (Note 5)		—	0.02	—	—	2	μA
Reverse blocking current	IRB	VOUT = 5.0 V, VIN = 0 V		—	0.01	—	—	2	μA
On resistance	RON	IOUT = -0.5A	VIN = 5.0 V	—	25	—	—	43	mΩ
			VIN = 3.3 V	—	31	—	—	53	
			VIN = 1.8 V	—	52	—	—	83	
			VIN = 1.2 V	—	104	—	—	185	
			VIN = 1.1 V	—	136	—	—	—	
Output discharge on resistance	RSD	— (Note 6)		—	100	—	—	—	Ω

Note 3: Only applies to the TCK22921G and TCK22971G

Note 4: Except OFF-state switch current

Note 5: Only applies to the TCK22971G, TCK22972G, TCK22973G, TCK22974G and TCK22975G

Note 6: Only applies to the TCK22921G, TCK22922G, TCK22923G, and TCK22925G

AC Characteristics (Ta = 25°C)

V_{IN} = 5.0 V

Characteristics	Symbol	Test Condition(Figure 1)		Min	Typ.	Max	Unit
V _{OUT} rise time	t _r	R _L =5Ω , C _L =1.0μF	TCK22921G	—	4.5	—	μs
			TCK22971G	—	—	—	
			TCK22922G	—	666	—	
			TCK22972G	—	—	—	
			TCK22975G	—	—	—	
			TCK22923G	—	1364	—	
V _{OUT} fall time	t _f	R _L =5Ω , C _L =1.0μF	TCK22923G	—	—	—	μs
			TCK22973G	—	—	—	
Turn on delay	t _{ON}	R _L =5Ω , C _L =1.0μF	TCK22925G	—	3380	—	μs
			TCK22974G	—	—	—	
			TCK22921G	—	3	—	
			TCK22971G	—	—	—	
			TCK22922G	—	380	—	
			TCK22972G	—	—	—	
Turn off delay	t _{OFF}	R _L =5Ω , C _L =1.0μF	TCK22975G	—	750	—	μs
			TCK22923G	—	—	—	
			TCK22973G	—	2000	—	μs
			TCK22925G	—	—	—	
			TCK22974G	—	—	—	μs
			TCK22921G	—	—	—	

AC Waveform

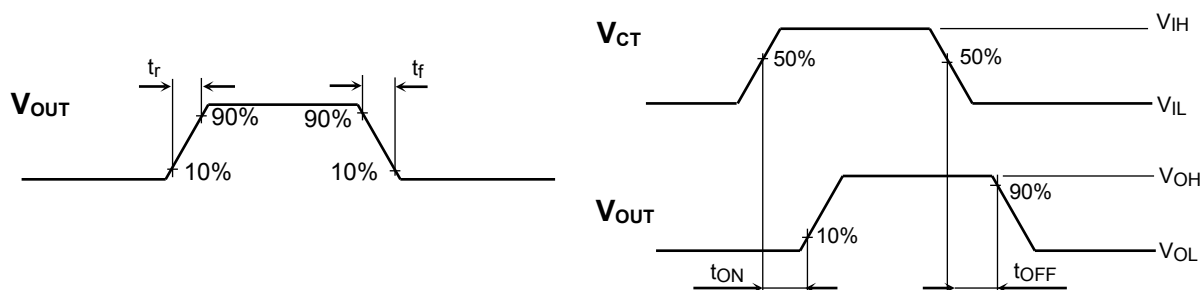


Figure 1 t_r, t_f, t_{ON}, t_{OFF} Waveforms(Active High)

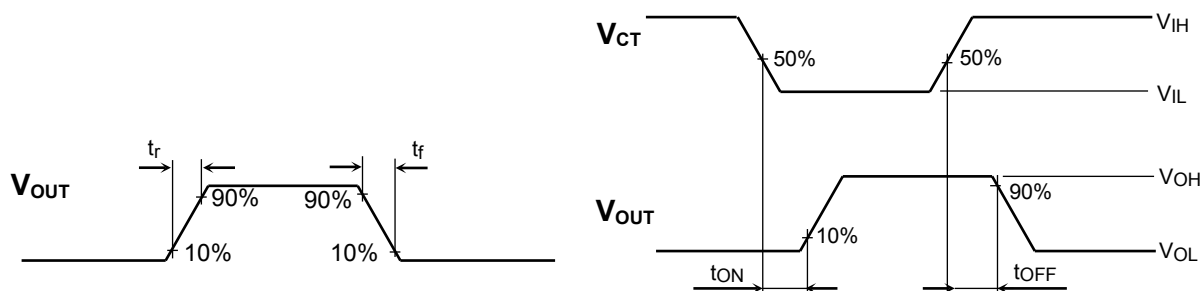
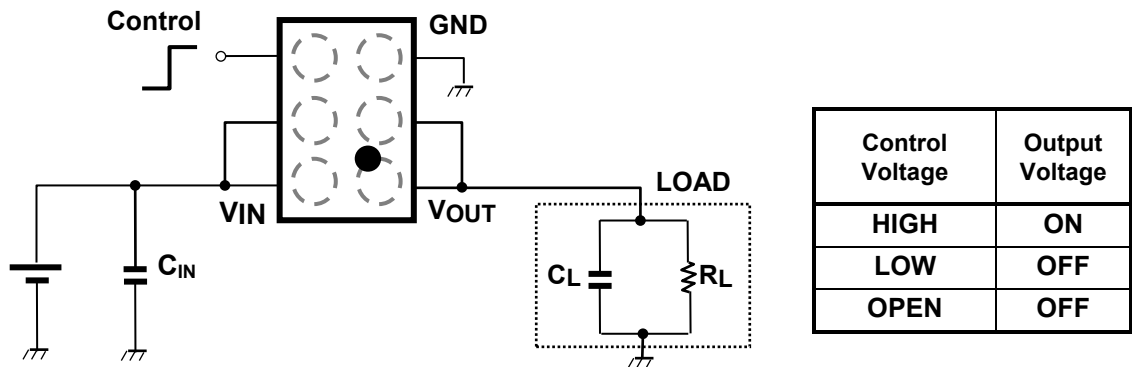


Figure 2 t_r, t_f, t_{ON}, t_{OFF} Waveforms(Active Low)

Application Note

1. Application circuit example (top view)

The figure below shows the recommended configuration



1) Input and Output capacitor

An input capacitor (C_{IN}) and an output capacitor (C_{OUT}) are highly recommended for the stable operation. And it is effective to reduce voltage overshoot or undershoot due to sharp changes in output current and also for improved stability of the power supply. When used, place C_{IN} and C_{OUT} more than $1.0\mu F$ as close to V_{IN} pin to improve stability of the power supply.

2) Control pin

The Control pin controls both the pass-through p-ch MOSFET and the discharge n-ch MOSFET (only for TCK2292xG), operated by the control voltage and Schmitt trigger. Also, pull down resistance equivalent to a few $M\Omega$ is connected between Control and GND, thus the load switch IC is in OFF state even when Control pin is OPEN. (except TCK22975G). Products that Control pin is an open connection, please use be sure to fix the potential of the Control pin to High or Low.

2. Reverse current blocking

This device has a built-in Reverse current blocking (SW OFF state) circuit to block reverse current from VOUT to VIN when output n-ch MOSEFT turned off and input voltage is 0V.

3. Instructions and directions for use

This device has a built-in several functions, but these does not assure for the suppression of uprising device operation. In use of these products, please read through and understand dissipation idea for absolute maximum ratings from the above mention or our 'Semiconductor Reliability Handbook'. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommend inserting failsafe system into the design.

4. Power Dissipation

Power dissipation is measured on the board condition shown below.

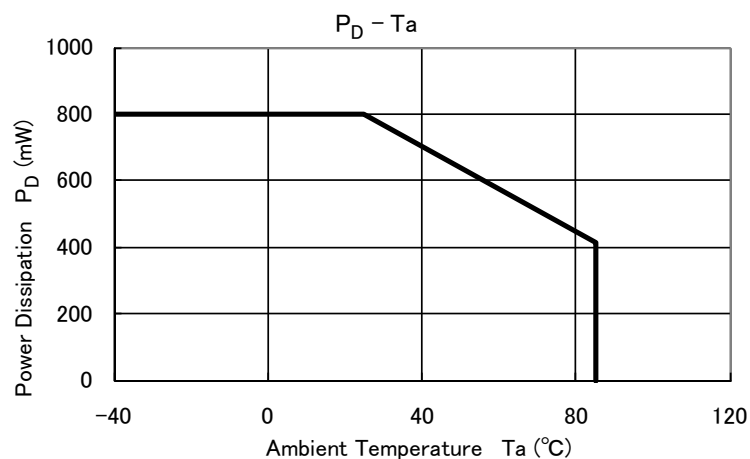
[The Board Condition]

Board material: Glass epoxy (FR4)

Board dimension: 40mm x 40mm (both sides of board), t=1.6mm

Metal pattern ratio: a surface approximately 50%, the reverse side approximately 50%

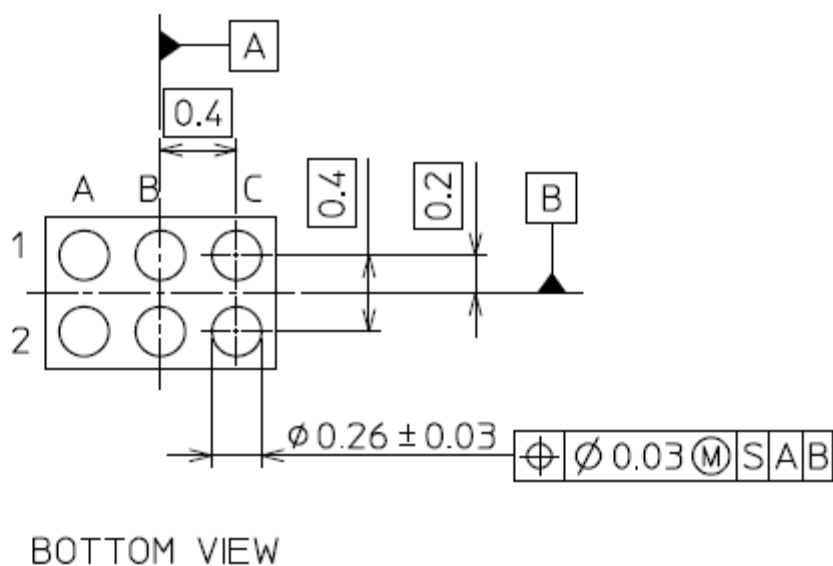
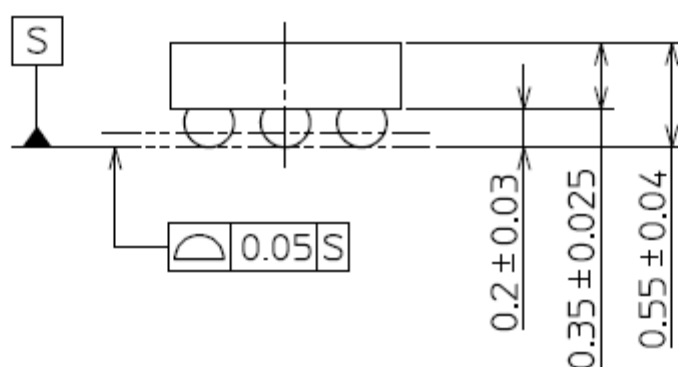
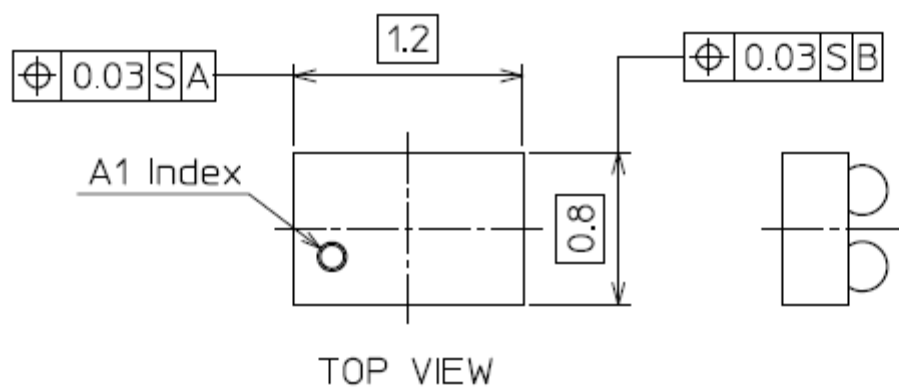
Through hole: diameter 0.5mm x 28



Please allow sufficient margin when designing a board pattern to fit the expected power dissipation. Also take into consideration the ambient temperature, input voltage, output current etc. and applying the appropriate derating for allowable power dissipation during operation.

Package dimension

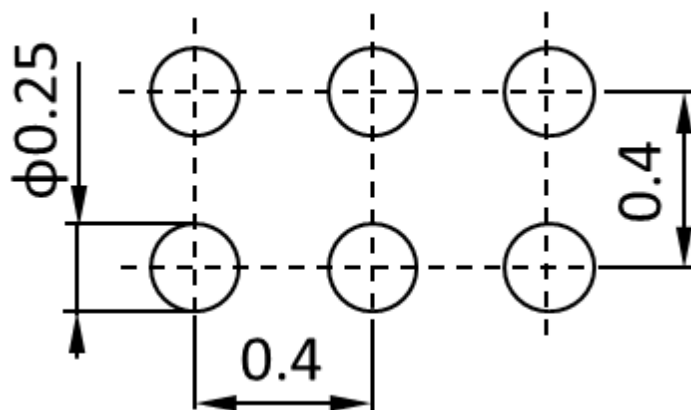
Unit: mm



Weight: 1 mg (typ.)

Land pattern dimensions (for reference only)

Unit: mm



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